

How to do Co-Layout between SOT-563 Package and SOT-236 Package



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ABSTRACT

Co-layout is more and more required in Buck converters applications due to the advantage of design flexibility. This application note focuses on how to co-lay between TPS56x242/7 with SOT-563 package and TPS56x201/8 with SOT-236 package. First, the pin-out is compared. Next, the schematic design and layout consideration are introduced. Finally, a co-layout design example is given and this application design is verified based on experiments.

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1 Introduction

The TPS56x242/7 is a single, adaptive on-time, D-CAP3™ control mode, synchronous buck converter that requires a very low external component count. The D-CAP3 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. TPS56x20x star parts series including: TPS561201/8, TPS562201/8, TPS563201/8, TPS564201/8, and TPS565201/8 which have been widely used in DTV, STB, surveillance, networking home terminal, and so on. Co-layout is more and more required in Buck converters applications due to the advantage of design flexibility. This application report mainly discusses how to do co-layout between TPS56x242/7 and TPS56x201/8.

2 Comparison of Pin-out

Figure 2-1 shows TPS56x242/7 pin-out with SOT-563 package which has been optimized. It integrates BST pin and add AGND for pin 4. Figure 2-2 shows TPS56x201/8 pin-out with SOT-236 package which is different from TPS56x242/7. Both packages and pin locations are different for these two families. VBST pin of TPS56x201/8 is used to supply input for the high-side NFET gate driver circuit. AGND pin of TPS56x242/7 is the ground of internal analog circuitry.

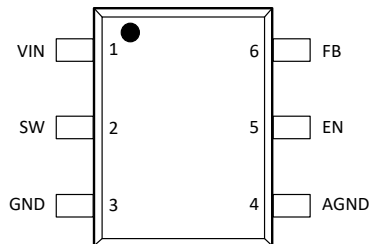


Figure 2-1. TPS56x242/7 Pin-out

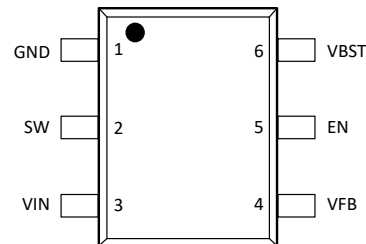


Figure 2-2. TPS56x201/8 Pin-out

Table 2-1. Pin Functions

Name	Pin NO.		Description
	TPS56x242/7	TPS56x201/8	
VIN	1	3	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	2	Switch node pin. Connect the output inductor to this pin.
GND	3	1	GND pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit.
FB	6	4	Converter feedback input. Connect to the output voltage with a feedback resistor divider.
EN	5	5	Enable input control. Driving EN high enables the converter.
VBST	NA	6	Supply input for the high-side NFET gate driver circuit. Connect 0.1- μ F capacitor between VBST and SW pins.
AGND	4	NA	Ground of the internal analog circuitry. Connect AGND to the GND plane.

3 Schematic Diagram

Since packages and pin locations are different for TPS56x242/7 and TPS56x201/8, the compatible schematic is designed to achieve co-layer. Figure 3-1 shows the co-layer schematic. There are several differences for the BOM. Table 3-1 shows solder information for different part.

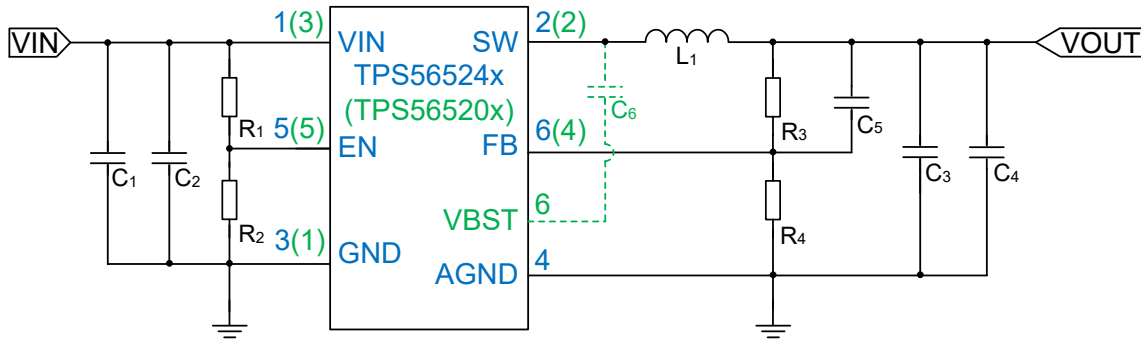


Figure 3-1. Schematic Diagram to Achieve Co-layer

Table 3-1. Solder Information for Different Part

Part Number	Description
TPS56x242/7	C ₆ needs to be floating. EN pin max voltage is 6 V.
TPS56x201/8	C ₆ needs to be soldered. EN pin max voltage is 19 V.

4 Layout Consideration

TPS56x242/7 is SOT-563 package which is 1.60 mm × 1.60 mm and TPS56x201/8 is SOT-236 package which is 1.60 mm × 2.90 mm. Figure 4-1 shows TPS56x242/7 package and Figure 4-2 shows TPS56x201/8 package. From the package, the body size of TPS56x201/8 is bigger than TPS56x242/7. When doing co-layout, the relative positions between SOT-236 device and SOT-563 devices needs to be considered and comply with manufacturer's rules. Figure 4-3 shows the piggyback solution for these two devices. It can make sure that the input capacitors of both devices are placed as close to the VIN pin to minimize trace impedance.

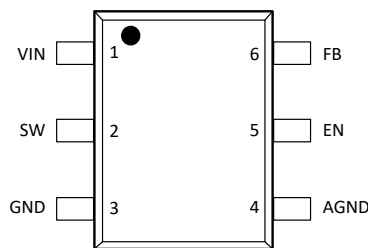


Figure 4-1. TPS56x242/7 Package

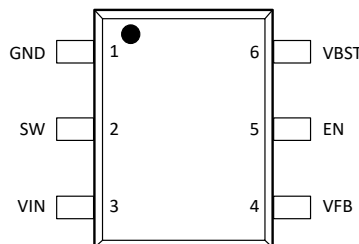


Figure 4-2. TPS56x201/8 Package

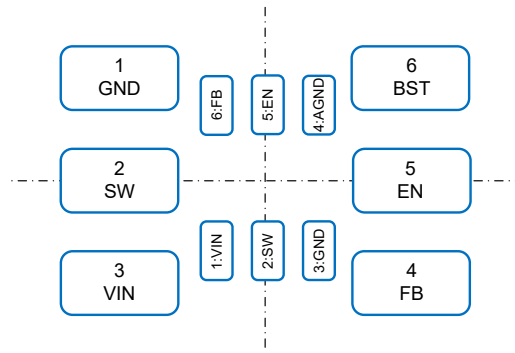


Figure 4-3. Piggyback Solution for TPS56x201/8 and TPS56x242/7

The recommend co-layout solution is shown in [Figure 4-4](#). The input capacitor is placed as close as possible to VIN pin. Voltage feedback loop is placed away from the high-voltage switching trace and has ground shield. The trace of the FB node is as small as possible to avoid noise coupling. When soldered with TPS565201, the switching trace is short and wide enough. When soldered with TPS565242, the switching trace goes through from the top layer to the bottom layer then back to the top layer with the connecting inductor. Please keep in mind that do not allow switching current to flow under the device.

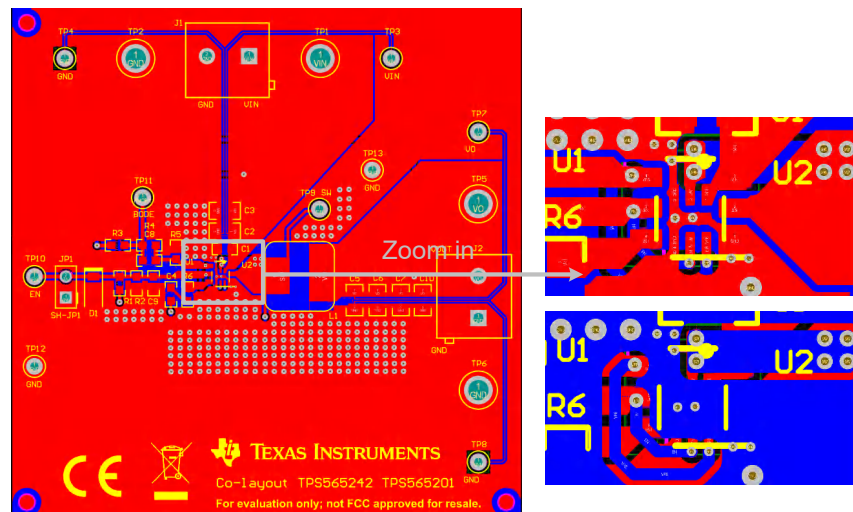


Figure 4-4. Co-layout EVM

5 Experimental Verification

This topic gives experimental verification of co-layout. The BOM of the co-layout board is the same as TI EVM board.

Figure 5-1 and Figure 5-2 show the board layout for the co-layout design.

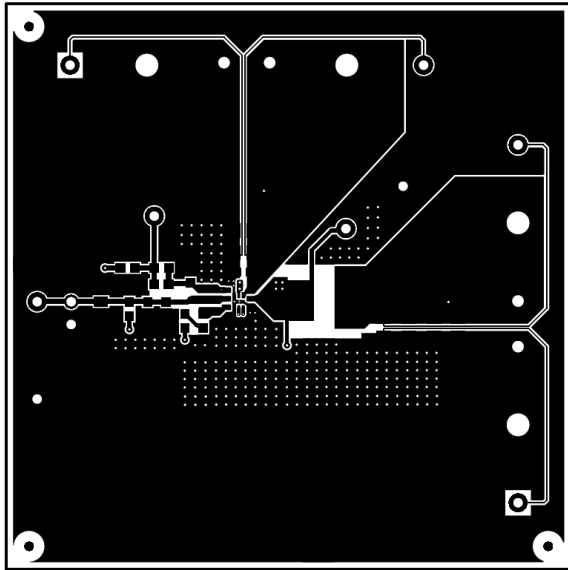


Figure 5-1. Co-layout Design Top Layer

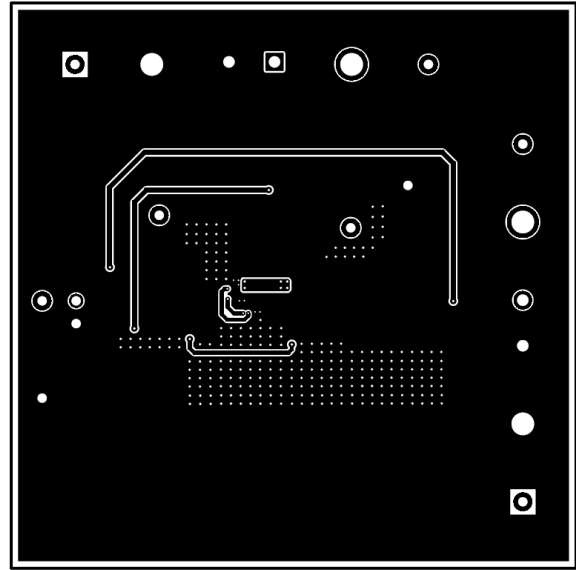


Figure 5-2. Co-layout Design Bottom Layer

Figure 5-3 and Figure 5-4 shows the output voltage ripple of EVM board and co-layout board with TPS565242. Figure 5-5 and Figure 5-6 shows the output voltage ripple of EVM board and co-layout board with TPS565201. The results show that co-layout board with both TPS565201 and TPS565242 can work well.

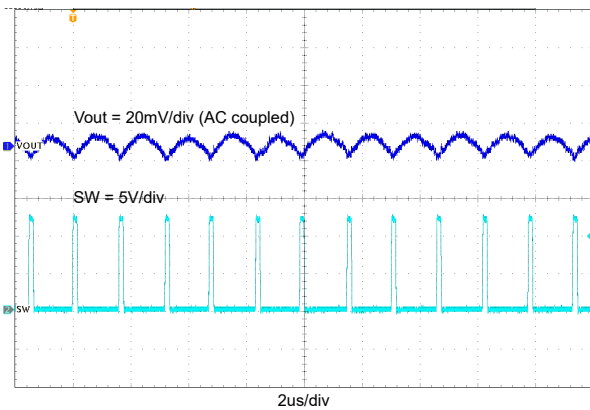


Figure 5-3. EVM Board with TPS565242 Output Ripple, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

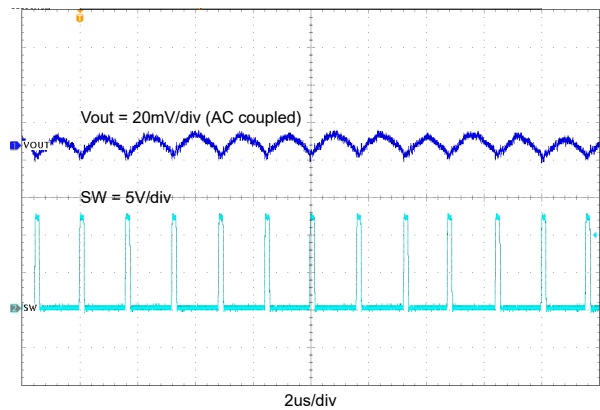


Figure 5-4. Co-layout Board with TPS565242 Output Ripple, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

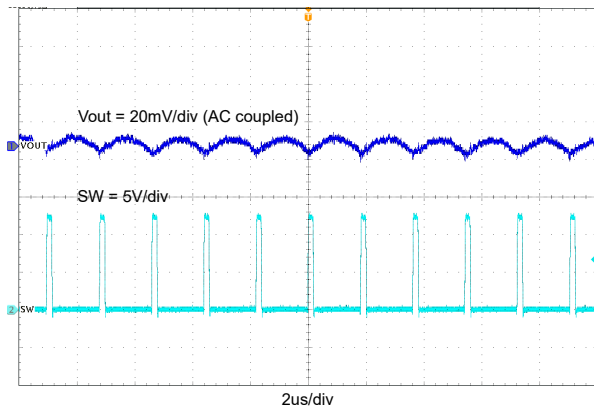


Figure 5-5. EVM Board with TPS565201 Output Ripple, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

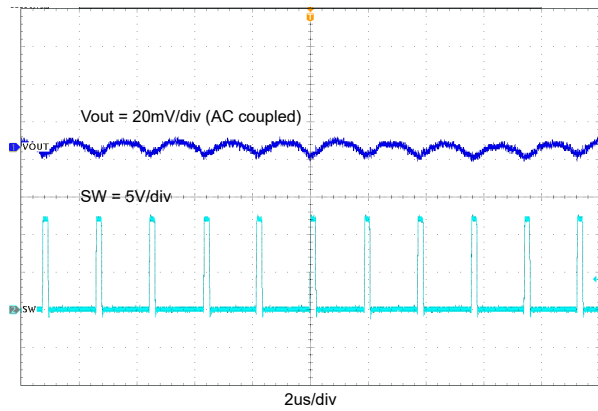


Figure 5-6. Co-layout Board with TPS565201 Output Ripple, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

Efficiency comparison between EVM and co-layout board which are tested at 1.05 V_{out} and 5 V_{out} are shown in [Table 5-1](#). From the efficiency results, it shows that the efficiency of co-layout board is slightly lower than EVM board.

Table 5-1. Efficiency Comparison between EVM and Co-layout Board, $V_{IN} = 12\text{ V}$, $I_{OUT} = 5\text{ A}$

	V_{out} (V)	Efficiency	V_{out} (V)	Efficiency
TPS565242 EVM board	1.05	84.2%	5	94.8%
TPS565242 Co-lay board	1.05	83.5%	5	94.4%
TPS565201 EVM board	1.05	77.3%	5	92.3%
TPS565201 Co-lay board	1.05	77.0%	5	92.2%

Switching spike voltage comparison between EVM and co-layout board which are tested at 1.05 V_{out} are shown in [Table 5-2](#). From the switching spike results, it shows that co-layout board is slightly worse than EVM board.

Table 5-2. Switching Spike Comparison between EVM and Colay Board

	V_{in} (V)	V_{out} (V)	I_{out} (A)	Switching spike voltage (V)
TPS565242 EVM board	12	1.05	5	12.0
TPS565242 Co-lay board	12	1.05	5	12.4
TPS565201 EVM board	12	1.05	5	13.2
TPS565201 Co-lay board	12	1.05	5	14.7

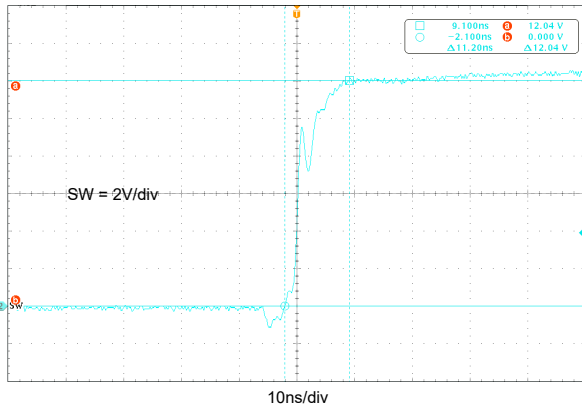


Figure 5-7. EVM Board with TPS565242 Switching Spike, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

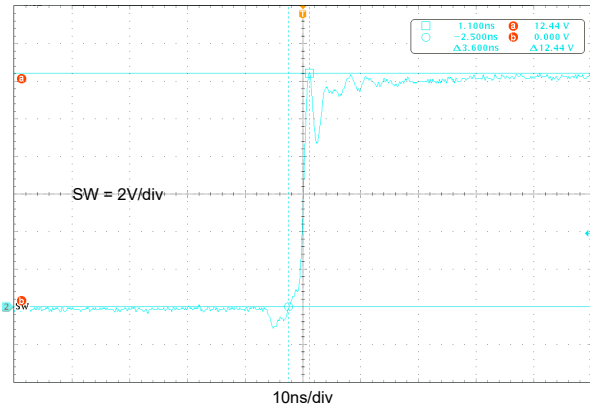


Figure 5-8. Co-layout Board with TPS565242 Switching Spike, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

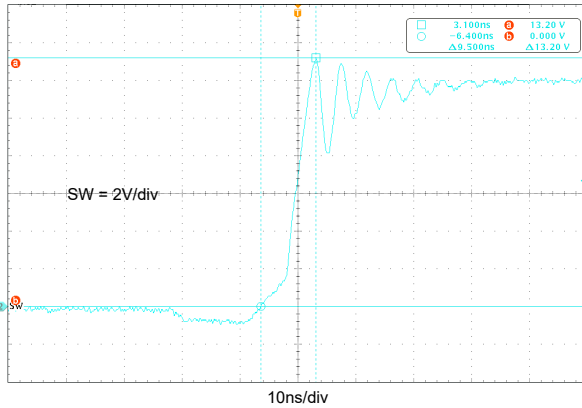


Figure 5-9. EVM Board with TPS565201 Switching Spike, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

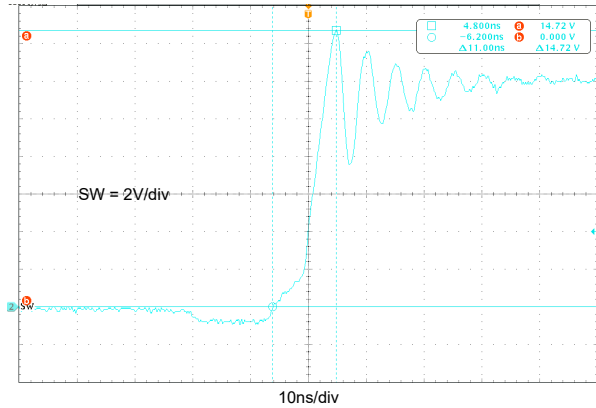


Figure 5-10. Co-layout Board with TPS565201 Switching Spike, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, $I_{OUT} = 5\text{ A}$

Figure 5-11 and Figure 5-12 shows the co-layout board with TPS565242 transient response with 0.1 A to 2.5 A and 1.25 A to 3.75 A. The current steps slew rate is set as 0.8 A/us.

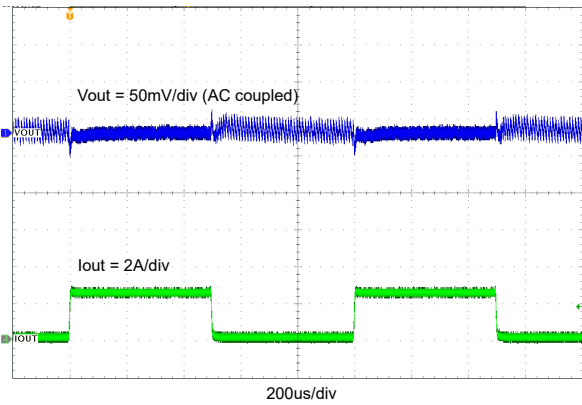


Figure 5-11. Co-layout Board with TPS565242 Transient Response, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, 0.1 A - 2.5 A

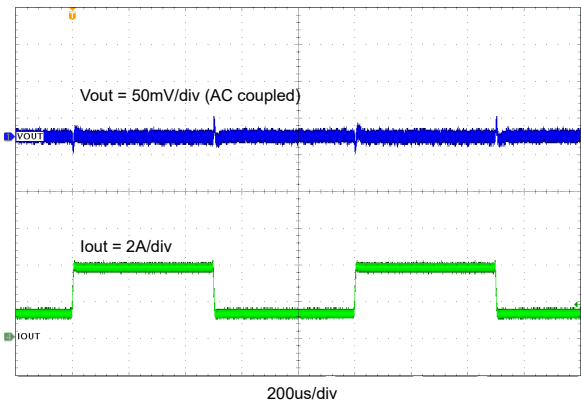


Figure 5-12. Co-layout Board with TPS565242 Transient Response, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, 1.25 A - 3.75 A

Figure 5-11 and Figure 5-12 shows the co-layout board with TPS565201 transient response with 0.1 A to 2.5 A and 1.25 A to 3.75 A. The current steps slew rate is set as 0.8 A/us.

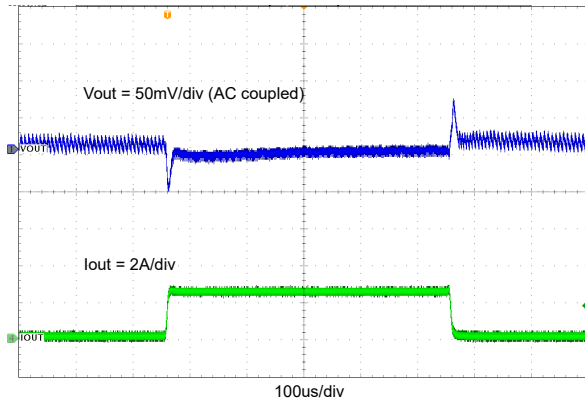


Figure 5-13. Co-layout Board with TPS565201 Transient Response, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, 0.1 A - 2.5 A

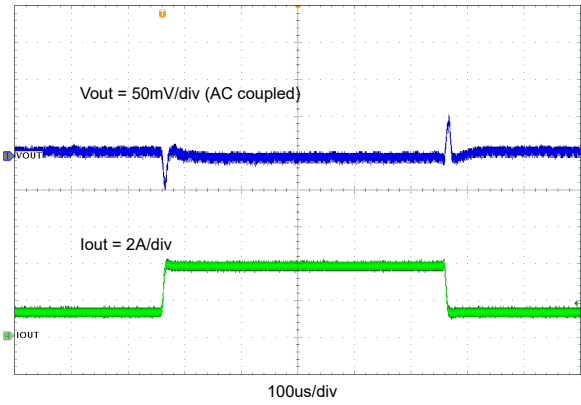


Figure 5-14. Co-layout Board with TPS565201 Transient Response, $V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$, 1.25 A - 3.75 A

6 Summary

This application note introduces how to co-layout between TPS56x242/7 with SOT-563 package and TPS56x201/8 with SOT-236 package. Pin-out is compared and layout recommendations are given. Finally, the application note shows the experiment verification results of the co-layout design. From the test results, both TPS56x242/7 and TPS56x201/8 can work well with co-layout board.

7 References

- Texas Instruments, [TPS56524x 3-V to 16-V Input Voltage, 5-A Synchronous Buck Converter in SOT-563 Package](#) data sheet.
- Texas Instruments, [TPS56424x 3-V to 16-V Input Voltage, 4-A Synchronous Buck Converter in SOT-563 Package](#) data sheet.
- Texas Instruments, [TPS565201 4.5-V to 17-V Input, 5-A Synchronous Step-Down Voltage Regulator](#) data sheet.
- Texas Instruments, [TPS564201 4.5-V to 17-V Input, 4-A Synchronous Step-Down Voltage Regulator](#) data sheet.

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