Application Note

Cell Balancing With BQ7690x Battery Monitors

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ABSTRACT

The BQ7690x (which includes the BQ76905 and BQ76907) is a highly accurate and low power battery monitor and protector family with a host-operated cell balancing feature. This document describes how to use the cell-balancing function, how to increase the balancing current using external circuitry (FETs and BJTs), and systems considerations for the host-controlled balancing algorithm.

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Trademarks

1 Introduction

Battery cells are typically matched during the manufacturing of battery packs. Over time, an imbalance in the state of charge may develop between cells and reduce the overall capacity of the pack. Having a battery monitor with the capability of cell balancing allows longer battery life for the pack.

The BQ7690x supports passive cell balancing by bypassing the current of selected cells during charging or at rest, using the integrated or external bypass switches. For external bypass switches, the user could select between FET or BJT transistors. Balancing must be initiated and controlled manually from a host processor.

While balancing is active, there will be a current flowing into the cell input pins. In order to measure accurately, cell balancing needs to be disabled temporary while measuring the individual cells. Therefore, the timing for measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. The internal balancing FETs are disabled temporarily during each ADSCAN while the cell voltages and shared slot are being measured while cell balancing is active on a cell.

2 Cell Balancing Circuit Considerations

Cell balancing of a particular cell consists of enabling an integrated FET switch across the cell. The balancing current is determined by value of the input filter resistors selected when using internal balancing. Field Effect Transitors (FETs) or Bipolar Junction Transistors (BJT) can be used to increase the balance current in applications where the internal balancing current may not be sufficient.

Internal balancing, external balancing with N-channel FETs, and external balancing with BJTs are discussed in this section. Considerations for power dissipation and timing is also discussed.

2.1 Internal Cell-Balancing Circuit Design

When one of the internal balance FETs is enabled, the internal FET will pull the pins for that cell together drawing current through the input resistors for that cell. The recommended minimum value of the input filter resistors when using internal balancing is 20Ω. This value maximizes the balance current while keeping it well within the absolute maximum cell balancing current over the internal FET $R_{DS(ON)}$ range. The maximum recommended value for the input filter resistors is 1kΩ.

The typical internal cell balancing resistance ($R_{DS(ON)}$ for the internal FET) is 80Ω. For a typical lithium ion cell with a full charge voltage of 4.2V, this results in a balancing current of approximately 35mA. This is the DC current assuming the switch was continuously on; therefore, the average balancing current will be lower. The duty cycle is determined by a multiple factors which are discussed in more detail in Section 4.

$$I\_Balance = \frac{V_{CELL}}{(2 \times R_n + R_{CB})} = \frac{4.2}{(2 \times 20 + 80)} \quad = 35mA \tag{1}$$

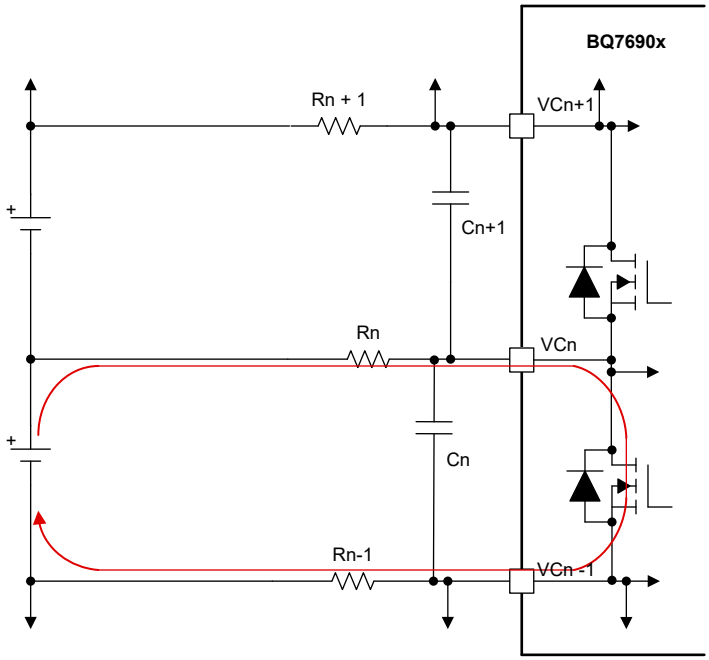

Figure 2-1. Application Circuit for Internal Balancing

For many applications, the internal balancing current for the device is sufficient and additional external components are not required. However, one must consider the power dissipation and the resulting impact on the device temperature. For example, 35mA into 80Ω results in about 0.098W (almost 100-mW). The junction to ambient thermal resistance (θ-JA) for the device is 47.2 °C/W. If 5-cells are balancing at the same time, this can result in a junction temperature rise of approximately 23 °C.

There are different alternatives to mitigate excessive power dissipation. The host can limit the maximum number of cells allowed to balance simultaneously, refer to How to Limit Maximum Balancing Cells. Another alliterative is to increase the cell input resistors, in order to reduce the balancing current and improve power dissipation.

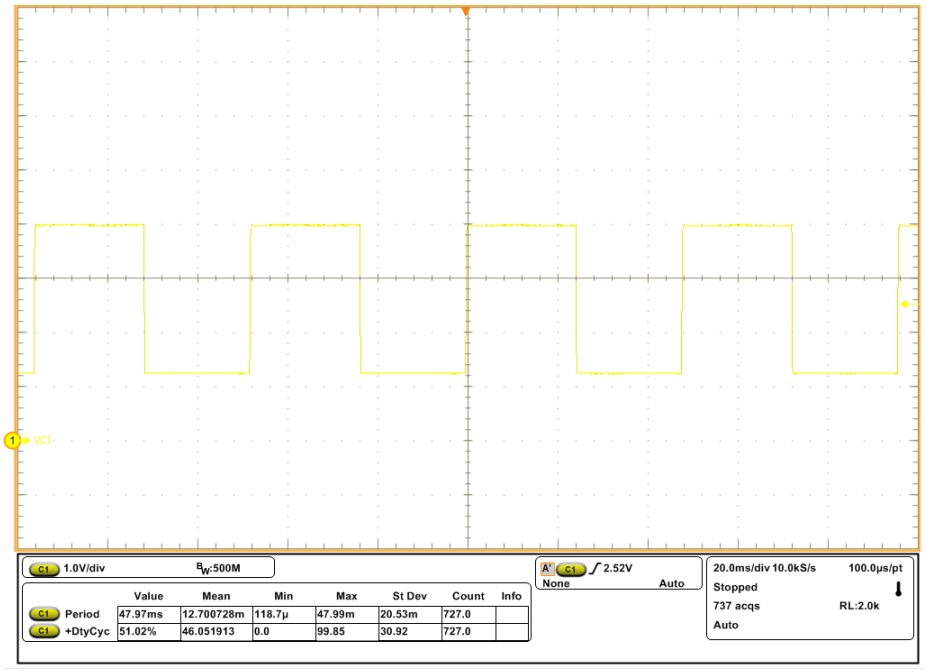

Figure 2-2. Internal Cell Balancing on Cell 1 (VC1)

Note

In Figure 2-2, the ON time of the duty cycle represents the active measurement time. While the low cycle represents the cell balancing time.

2.2 External Cell-Balancing Circuit Design Using N-Channel FETs

For applications that need higher cell balancing current, external FETs are often used. When using external FETs, the cell input resistors can be increased to the maximum recommended value of 1kΩ. Increasing the resistor size will help to provide enough voltage across the gate of the FET. In Figure 2-3, as the internal FET is turned on inside the device, the current flowing through R_{n-1} provides the V_{GS} for the external FET.

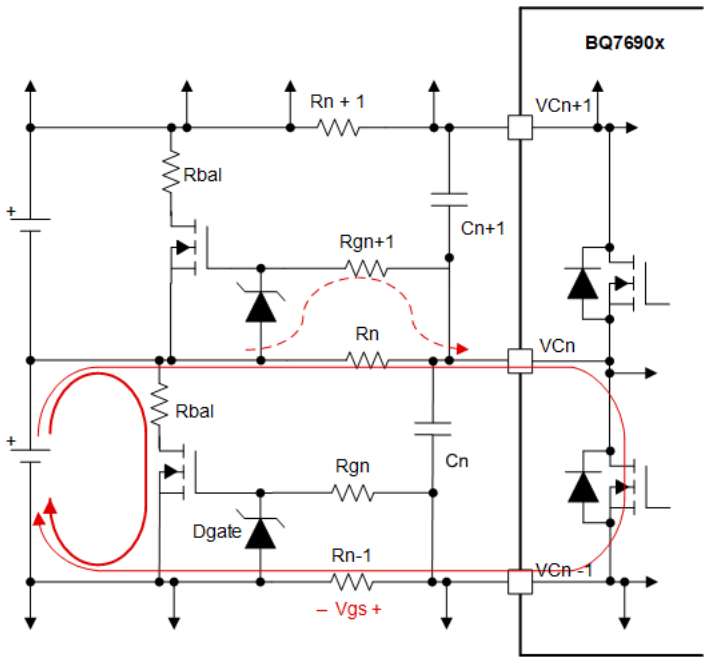

Figure 2-3. Balancing Circuit Using External N-channel FETs

Care must be taken to select an external FET with a low R_{DSON} defined at low V_{GS}. For example, say the minimum cell balance voltage is 3.9V. The external FET can have an R_{DSON} defined at or below 3.9V x 100 / (100 + 100 + 80) = 1.39V.

A Zener diode is needed to protect the external FET gate from pack transients. For example, in the event of a short across the pack in a 7-cell battery, Cell 7 would have approximately 28V across R_n during the event and the opposite transient at the release of the short circuit. The gate voltage can be connected through a resistor to limit the current when the diode conducts. (During normal operation the Zener will not conduct).

For Figure 2-3, the circuit was designed with an R_n of 100Ω and R_{gn} of 1kΩ. The R_{bal} resistor is set to 50Ω for a balance current of approximately 77mA through the external FET at 4V. At this cell voltage, an additional approximately 15mA of current flows through the internal FET of the device for a total balancing current of close to 92mA. An N-channel MOSFET was selected with an R_{DSON} defined for low V_{GS} down to 1.4V.

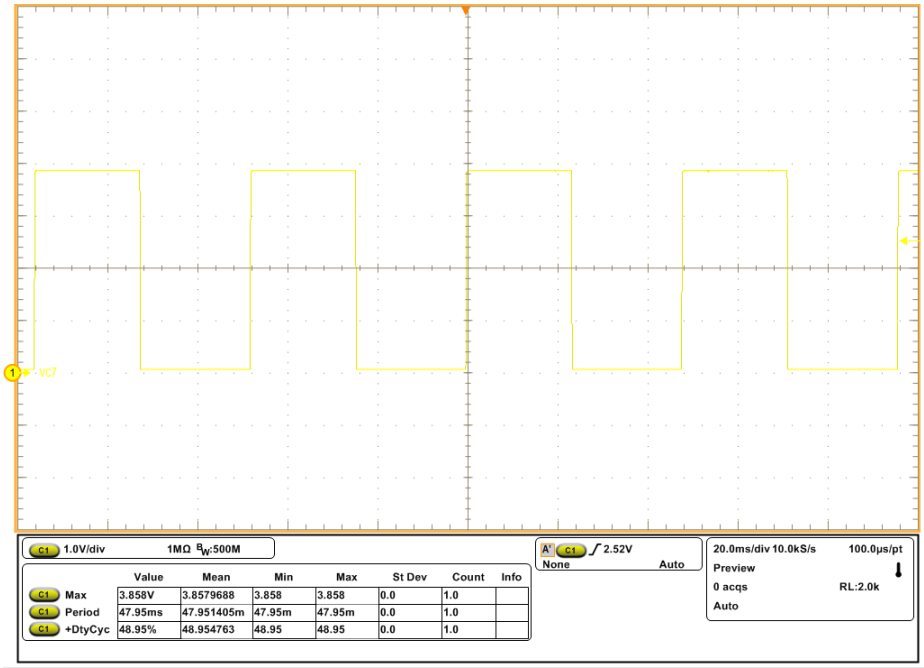

Figure 2-4. BQ76907 Cell Balancing With N-Channel FETs, Cell 7 (VC7) Rbal_voltage Approximately = 3.86V

Note

In Figure 2-4, the ON time of the duty cycle represents the voltage across the Rbal resistor while balancing cell 7 (VC7). While the low cycle represents the voltage across Rbal resistor when balancing is OFF.

2.3 External Cell-Balancing Circuit Design Using BJTs

External FETs are suited for applications with typical 4.2V lithium ion cells since balancing is most commonly done at higher voltages during charge. For applications that need higher balancing current than the internal balancing can provide but also need to balance at lower cell voltages, external BJTs may be considered. The balancing current for an external BJT can be controlled by selecting the appropriate balance resistor (R_{bal}) and base resistor (R_{bn}). In Figure 2-5, as the internal FET is turned on inside the device, the current flowing through R_{bn} puts the NPN transistor into saturation.

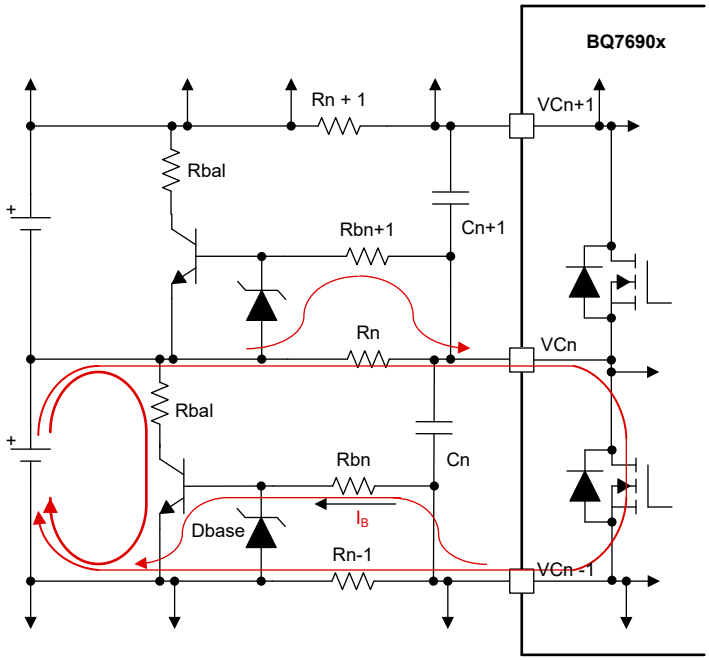

Figure 2-5. Balancing Circuit Using External BJTs

A Zener diode is also used in this circuit to protect from pack transients similar to the FET circuits. A standard diode is also suitable to use instead of a Zener when using BJTs because it is the forward voltage of the Zener that protects the transistor. The base-emitter diode (or emitter-base diode for a PNP) will conduct in the reverse direction which will prevent the Zener from conducting.

Note

The Zener diode might not be needed since the BJT comes with a built-in diode.

In Figure 2-6, the circuit was designed with an R_n of 100Ω and R_{gn} of 240Ω. The R_{bal} resistor is set to 50Ω for a balance current of approximately 74mA through the BJT at 4V. At this cell voltage, an additional approximately 15mA of current flows through the internal FET of the device for a total balancing current of close to 89mA. An NPN transistor was selected with hFE of 30 at IC = 100 mA.

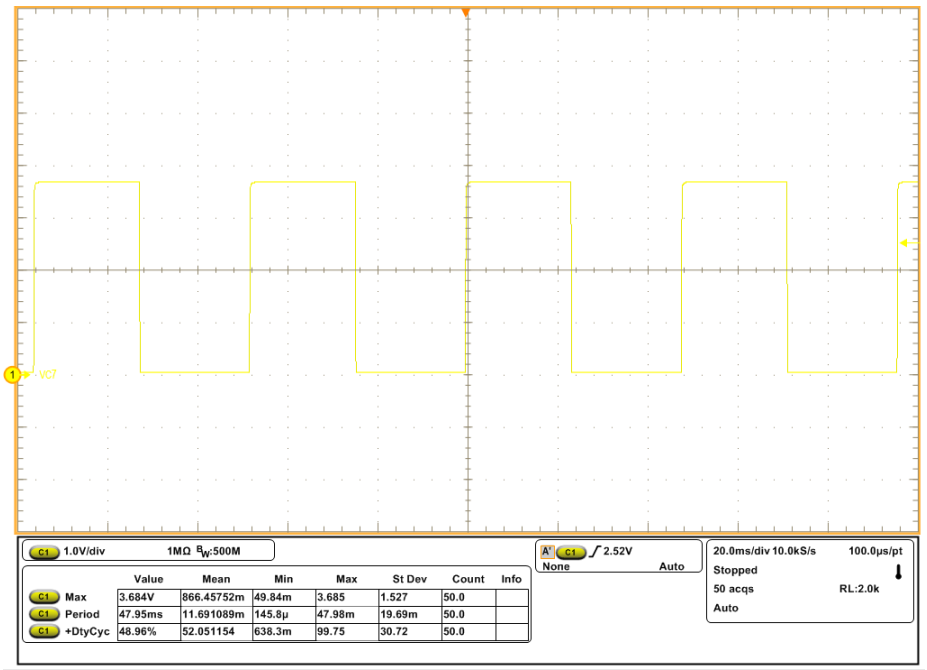

Figure 2-6. BQ76907 Cell Balancing With NPN BJT, Cell 7 (VC7) Rbal_voltage Approximately = 3.68V

Note

In Figure 2-6, the positive duty cycle represents the voltage across the Rbal resistor while balancing cell 7 (VC7). While the negative duty cycle represents the voltage across Rbal resistor when balancing is OFF.

3 Considerations for a Host-Balancing Algorithm

CAUTION

Improper setting of the cell-balancing control bits can damage the IC.

Host-controlled balancing can be controlled using specific subcommands sent by the host, these subcommands are also accessible in SEALED mode, to avoid the need for the pack to be unsealed in operation in order to initiate balancing. If host-controlled balancing will not be used, access to these subcommands can be disabled by setting the ***Balancing Configuration[CB_NO_CMD]*** configuration bit. The subcommand used by the host to control cell balancing is described in Table 3-1.

Table 3-1. Host-Controlled Cell Balancing Subcommand

Subcommand	Description
0x0083 CB_ACTIVE_CELLS()	When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x00 to turn balancing off.

Note

When writing to the host-controlled balancing commands, it is necessary to write the checksum and length to registers 0x60/0x61 for the values to be written successfully. Refer to the BQ76907 Technical Reference Manual or BQ7690x Software Development Guide for information on writing the checksum and length.

Adjacent, as well as non-adjacent cells can be balanced. Balancing is controlled using the *0x0083 CB_ACTIVE_CELLS()* subcommand sent by the host. When balancing is initiated using this subcommand, the device starts a timer and will begin balancing the specified cells for up to 20 seconds. The timer is reset if a new balancing subcommand is issued. This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ7690x, so that balancing cannot continue indefinitely. The host can

write 0x00 to the subcommand to disable balancing. When this subcommand is read, it reports a bit mask of which cells are being actively balanced.

The device will disable balancing if the ADC measurement of a thermistor (if the TS pin is configured for thermistor measurement) is above ***Settings:Cell Balancing:Min Temp Threshold*** (the threshold for the minimum temperature) or below ***Settings:Cell Balancing:Max Temp Threshold*** (the threshold for the maximum temperature) or the internal die temperature of the device exceeds a programmable threshold set by ***Settings:Cell Balancing:Max Internal Temp***.

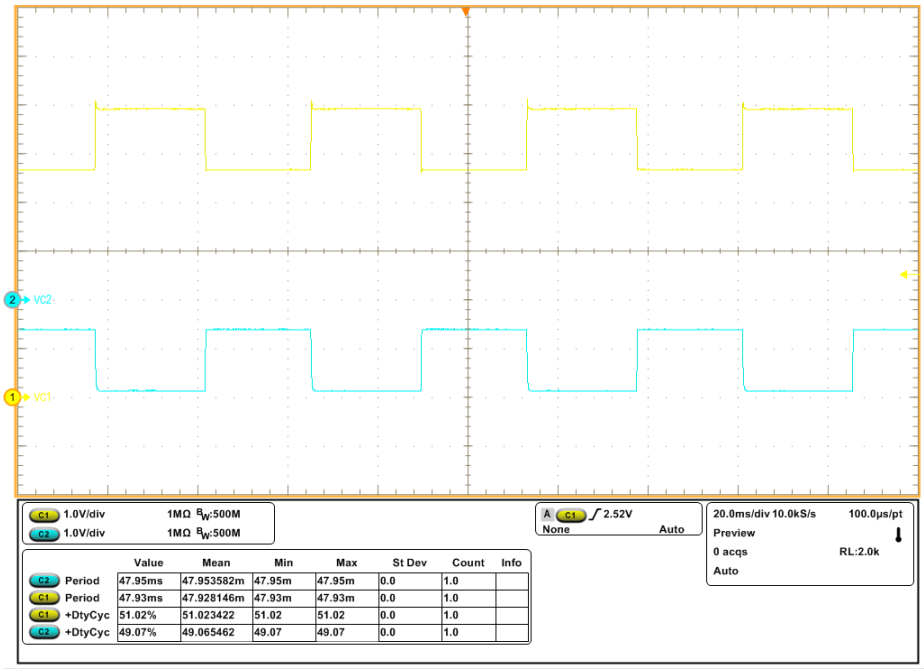

Figure 3-1. Adjacent Cell Balancing, Cell 1 (VC1) yellow, Cell 2 (VC2) blue.

Note

Note on Adjacent Cell Balancing: Care needs to be taken when using host-controlled balancing to ensure the power dissipation is at safe levels. Adjacent cell balancing can only be used in special cases after careful consideration. Care must be taken to not exceed the abs max 50mA cell balancing current limit or the abs max VC0 input voltage limit.

How to Limit Maximum Balancing Cells

To avoid excessive power dissipation when cell balancing, the host can limit the maximum number of cells allowed to balance simultaneously. To achieve this, the host will need to specify the cells that are allowed to be balanced by writing to the CB ACTIVE CELLS register.

CB ACTIVE CELLS Register Field Descriptions

Bit	Field	Description
7–0	CBCELLS_7–CBCELLS_0	Cell balancing active cells: When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x00 to turn balancing off. Bit 7 corresponds to the seventh active cell Bit 6 corresponds to the sixth active cell Bit 5 corresponds to the fifth active cell Bit 4 corresponds to the fourth active cell Bit 3 corresponds to the third active cell Bit 2 corresponds to the second active cell Bit 1 corresponds to the first active cell (will be connected between VC1 and VC0) Bit 0 is reserved, read/write 0 to this bit

Figure 3-2. CB ACTIVE CELLs Register

For instance, you can perform the following sequence to allow for cell 5 and cell 7 for balancing.

1. Write to the *0x0083 CB_ACTIVE_CELLS()* followed by the specified cell.
   a. W:10 3E 83 00 A0
2. Write the checksum and length.
   a. W:10 60 DC 05
3. (Optional) Read after writing to ensure the specified cells are being balanced.
   a. R:10 40 2

Note

Writing to RAM registers is explained in the BQ7690x Software Development Guide.

4 Timing Information

Due to the current that flows into the cell input pins on the BQ7690x while balancing is active, cell voltage measurements cannot be made without disabling balancing temporarily. Therefore, the timing for measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. While balancing of any cell is active, the balancing FETs are disabled temporarily during each ADSCAN while the cell voltages are being measured, as well as during the Shared Slot measurement. In order to meet the need for regular measurements while cell balancing is underway, the ***Settings:Configuration:Power Config[CB_LOOP_SLOW[1:0]]*** configuration bits modify the cell voltage measurement timing when cell balancing is active, to increase the average balancing current. This modification involves replacing the measurements in selected ADSCANs with idle slots of the same width, to allow balancing to remain active a higher percentage of the time.

Table 4-1. Cell Balancing Loop Slow-Down Settings

CB_LOOP_SLOW_1	CB_LOOP_SLOW_0	Description
0	0	Measurements are skipped in one of every two ADSCANs.
0	1	Measurements are skipped in three of every four ADSCANs.
1	0	Measurements are skipped in seven of every eight ADSCANs.
1	1	Measurements are skipped in 15 of every 16 ADSCANs.

Note

The LOOP_SLOW and CB_LOOP_SLOW settings operate independently. The LOOP_SLOW setting determines the speed of the regular measurement loop while balancing is not active. The CB_LOOP_SLOW setting determines the speed of the regular measurement loop only while balancing is active (the two settings do not combine together during balancing).

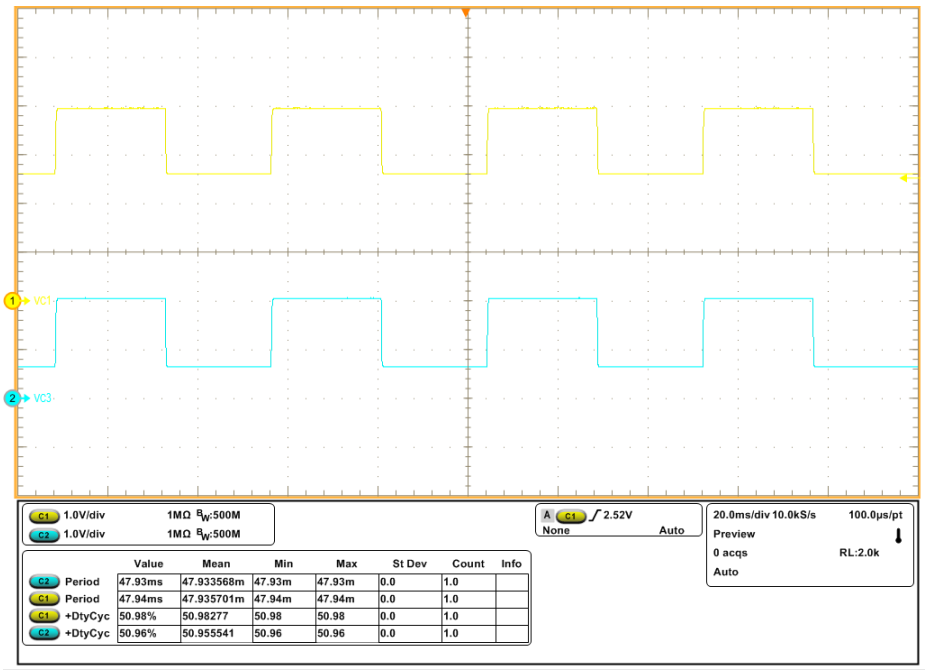

Figure 4-1. Internal Cell Balancing With CB_LOOP_SLOW = 0x00, Cell 1 (VC1) yellow, Cell 3 (VC3) blue

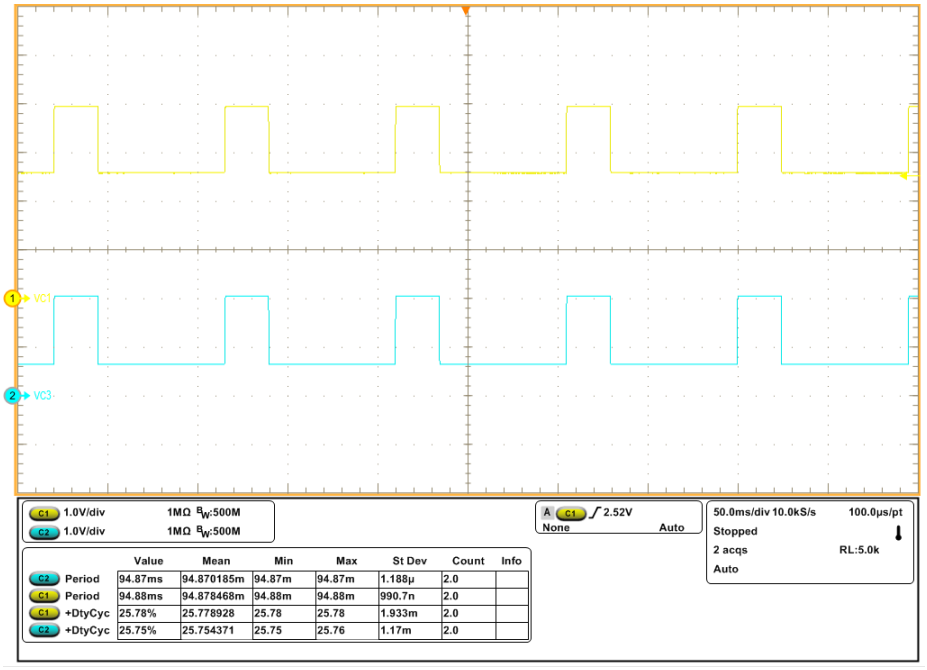

Figure 4-2. Internal Cell Balancing With CB_LOOP_SLOW = 0x01, Cell 1 (VC1) yellow, Cell 3 (VC3) blue

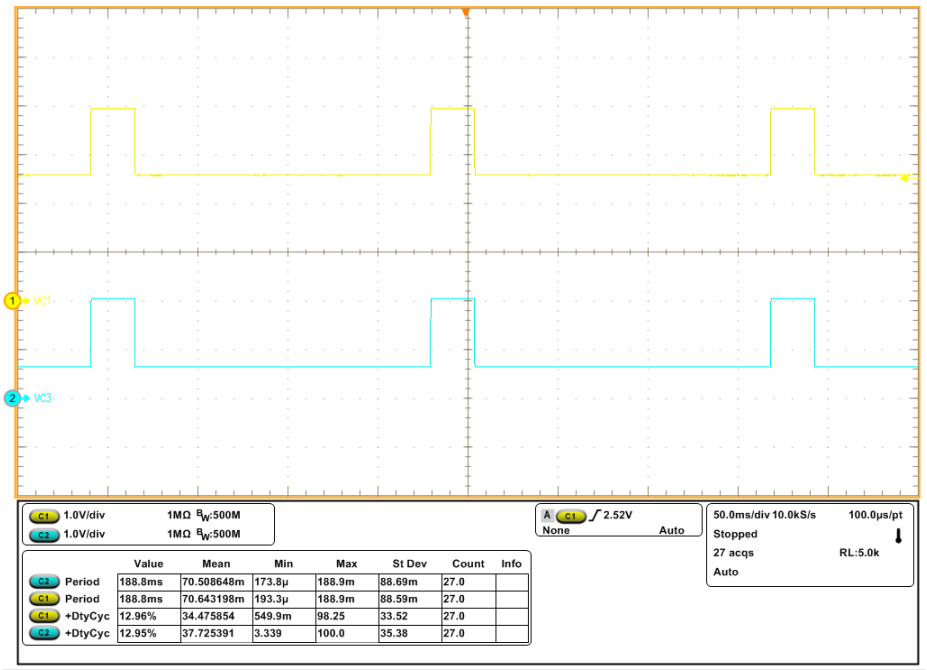

Figure 4-3. Internal Cell Balancing With CB_LOOP_SLOW = 0x10, Cell 1 (VC1) yellow, Cell 3 (VC3) blue

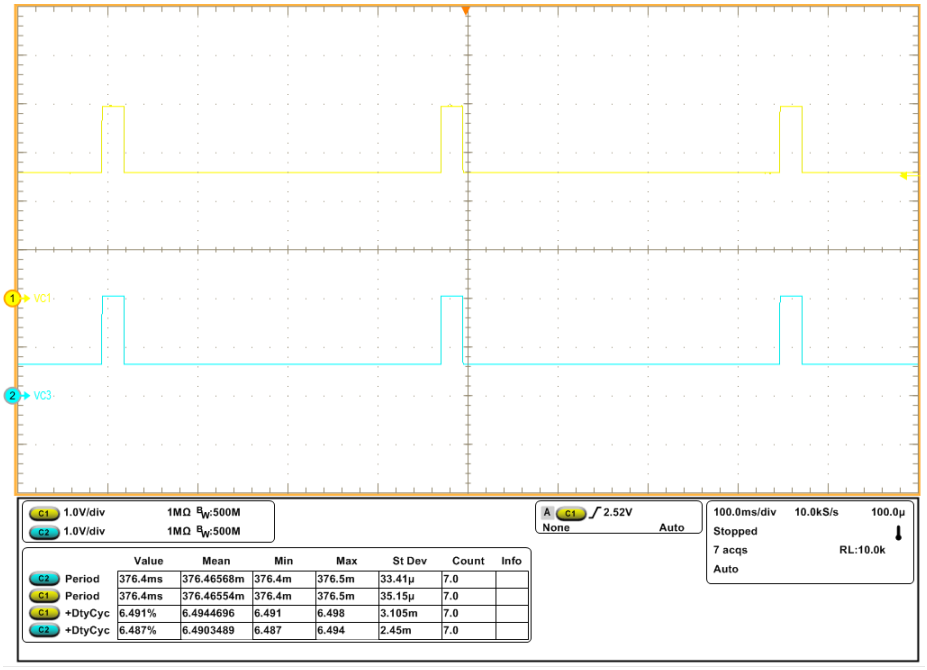

Figure 4-4. Internal Cell Balancing With CB_LOOP_SLOW = 0x11, Cell 1 (VC1) yellow, Cell 3 (VC3) blue

Note

In the previous four figures, the positive duty cycle represents the active measurement time. While the negative duty cycle represents the cell balancing time.

At the time cell balancing is disabled (either indefinitely or periodically to allow regular cell voltage measurements), there will be a voltage transient generated that can affect several nearby cell input pins, due to the resistor and capacitor network at those pins. If a cell measurement occurs too quickly after cell balancing has been disabled, the accuracy of the cell voltage measurement can be impacted. In order to address this potential issue, the device includes a programmable delay implemented each time cell balancing is disabled

before any cell voltage measurements are taken. This delay is set by ***Settings:Cell Balancing:Balancing Configuration[CBDLY2:0]*** from zero to 64 ms. It should be noted that this delay will increase the time between successive active measurement loops.

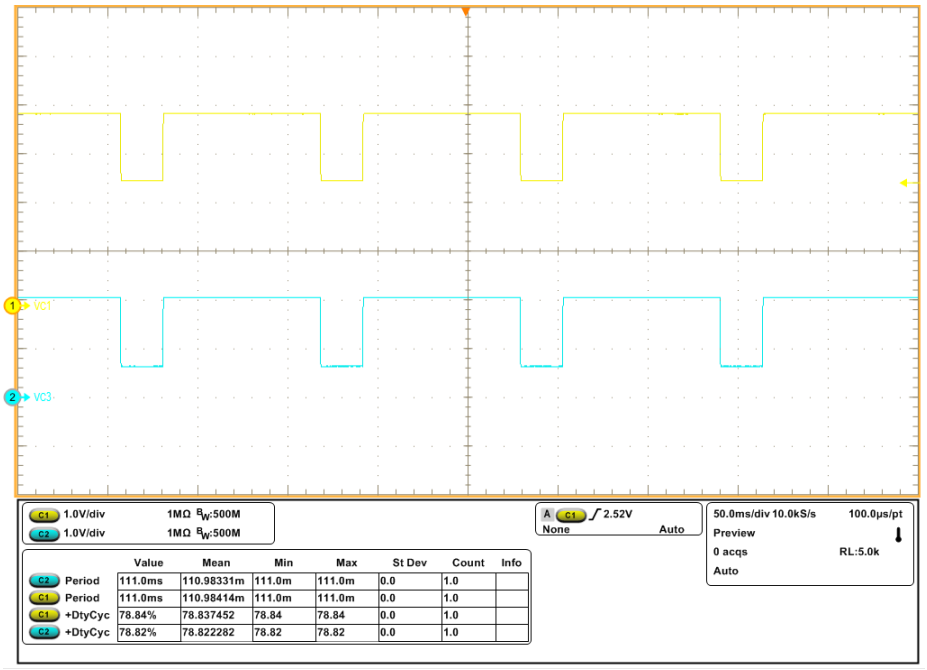

Figure 4-5. Cell Balancing With CB_LOOP_SLOW = 0x00 And Settings:Cell Balancing:Balancing Configuration[CBDLY2:0] = 0x07 (64 ms delay), Cell 1 (VC1) yellow, Cell 3 (VC3) blue

Note

Notice how the active measurement time is increased by approximately 64ms with respect to Figure 4-1. This allows the user to read very accurate voltage measurements values.

5 Debugging Common Issues With Cell Balancing

5.1 Using a Resistor Divider as a Cell Simulator

When testing the cell balancing feature with a power supply and resistor divider to simulate cells, this can often trigger the over-voltage protection which can be observed in the ***Safety Alert A*** register. This is because the resistor divider can pull on the voltages of the other cell inputs when cell balancing starts on one of the cells. This causes the voltages to become unstable, which triggers the over-voltage condition. Any time an over-voltage condition occurs, cell balancing is immediately disabled.

The best way to test the cell balancing feature is with real cells. If real cells are not available, another option is to use a resistor divider with a second power supply connected across one of the cells. For example, if the main supply and resistor divider are set to provide 3.9V on each cell input, a second supply set to 3.9V can be connected across one of the cell inputs.

5.2 Cell Balancing Troubleshooting

1. ***Why does cell balancing stop after a few seconds?***
   The balancing automatically stops after 20 seconds. It is the user responsibility to resend the 0x0083 command.
2. ***Why do I need to send the Cell Balancing command multiple times when using the Commdand Sequence tab in BQStudio?***
   Make sure the ***Auto Refresh*** and the ***Scan*** icons are OFF so that the EV2400 does not keep talking to the device while balancing.
3. ***Why my multimeter reports a lower balancing current and lower voltage when balancing?***
   The multimeter reports an average value because it cannot keep up with the measurement frequency. A scope must be used to be able to capture these measurements.
4. ***Why is the cell balancing not working after sending 0x0083 subcommand?***
   A checksum and length must be sent. Please see the following example.
   Cell 1 (VC1) Cell Balancing command
   - W: 10 3E 83 00 02 (writes to cell 1)
   - W: 10 60 7A 05 (checksum and length)
   - R: 10 40 2 (reads active balancing cells)
5. ***Where can I probe to see cell balancing happening at a particular cell?***
   You can be probing at the VCx pins if using internal balancing. If using external balancing circuitry, it is recommended to probe at the external balancing resistor to see if the FET or BJT is ON.
6. ***How can I calculate the maximum allowed dissipated power through the internal balancing FETs?***
   $P = (I_{max})^2 \times R_{DS(ON)}$

   Where I_{max} is the maximum cell balancing current at each cell (50 mA)

   Where the typical internal cell balancing resistance ($R_{DS(ON)}$ for the internal FET) is 80Ω

6 Summary

The BQ7690x (which includes the BQ76905 and BQ76907) includes a host-operated cell balancing feature, which allows to extend the battery life of your multi-cell battery pack. Applications needs willl determine the best alternative to incorporate cell balancing in your system design. This document describe how cell balacing works on the BQ7690x, how to increase the balancing current by using external FETs, and systems consideration for the balancing algorithm. In addition, it incorporate tests results using the BQ76907 to showcase the cell balancing functionality, alongiside common issues and troubleshooting techniques for cell balancing. This document is a guide on how to use the BQ7690x cell balancing functionality for your application.

7 References

- Texas Instruments, *BQ76907 2-s to 7-s High Accuracy Battery Monitor and Protector for Li-Ion, LiPolymer, and LiFePO4 Battery Packs)*, data sheet.
- Texas Instruments, *BQ76905 2-s to 5-s High Accuracy Battery Monitor and Protector for Li-Ion, LiPolymer, and LiFePO4 Battery Packs)*, data sheet.
- Texas Instruments, *BQ76907*, technical reference manual.
- Texas Instruments, *BQ76905*, technical reference manual.
- Texas Instruments, *Battery Management Studio (BQStudio) Software*.
- Texas Instruments, *BQ7690x Software Development Guide*, user's guide.
- Texas Instruments, *BQ76907*, product page.
- Texas Instruments, *BQ76905*, product page.

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