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TPS382x Microprocessor Supervisory Circuits with Watchdog Function

in SOT-23 Package

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TPS382x Microprocessor Supervisory Circuits With Watchdog Function in SOT-23 Package

ABSTRACT

This application report introduces micropower supply voltage supervisors (SVS), discusses their benefits, and describes design methods and precautions for their use.

1 Introduction

This application report supplements and uses information in the TPS3823/3824 data sheet and other supply voltage supervisor (SVS) application information published by Texas Instruments. These can be found on the internet in the semiconductor pages at:

http://www.ti.com/sc/docs/msp/power/default.htm

The TPS382x family of micropower SVSs provides circuit initialization and supervision, primarily in microprocessor-based applications, where partial/complete power loss and processor code dead loops can cause system malfunction.

2 Package Information

Figures 1 and 2 show the package configurations for the TPS3823 and TPS3824, respectively. Table 1 describes the I/O pin and signal characteristics.

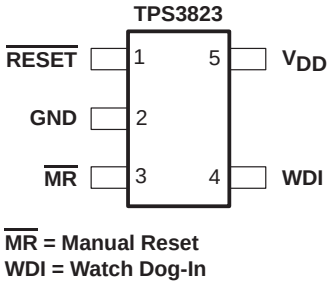

Figure 1. TPS3823 Package Pinout

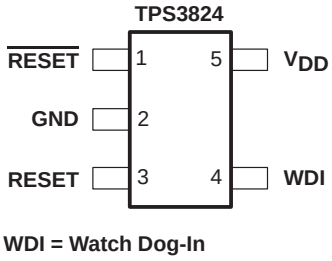

Figure 2. TPS3824 Package Pinout

Table 1. Pin Description

TPS3823	TPS3824	NAME	FUNCTION
1	1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ output (active low). This pulses low for a typical minimum of 200 ms when triggered, and stays low when V_{DD} is below the reset threshold or $\overline{\text{MR}}$ is low. It stays low for 200 ms after any of the following events: $\overline{\text{MR}}$ returns from low to high, V_{DD} rises above the reset threshold, or the watchdog causes a reset.
2	2	GND	Ground pin. Zero-volt reference for all signals.
3	N/A	$\overline{\text{MR}}$	Manual reset input (active low). A low level causes the $\overline{\text{RESET}}$ output to become active. Reset stays active while $\overline{\text{MR}}$ is low and for 200 ms after $\overline{\text{MR}}$ returns high. This input has an internal 52-kΩ pull-up resistor and can be driven from CMOS logic or a switch to ground. Connect to V_{DD} or leave open if unused.
N/A	3	RESET	RESET output (active high).
4	4	WDI	Watchdog input. If a WDI transition does not occur within a watchdog timeout period a reset is triggered. The timer is cleared by a rising or falling transition at the WDI input or an active $\overline{\text{RESET}}$ output.
5	5	V_{DD}	The supply voltage pin.

3 Power Supply Problems

Power supply problems such as spikes, surges, and brownout (a slowly falling supply voltage) can lead to system failures if a simplistic power-on-reset scheme (for example, an RC network) is used. Noise spikes on the supply can cause unwanted full or partial resets, and brownout can give rise to indeterminate system states if normal power is restored from a partial supply failure. Not all reset schemes work the same.

Two Texas Instruments publications (Literature numbers SLVAE03 and SLVAE04) give detailed discussions of these problems and describe the uses of SVS devices in general, and the TL77xx and TLC77xx series in particular.

The new family of TPS382x devices from Texas Instruments includes adequate hysteresis and reset logic delays to prevent the reset output from toggling. Reset toggling can occur when additional system power is drawn after the reset logic is cleared and the processor restarts, causing a drop in V_{DD} that triggers another reset. This happens most often when the processor initialization sequence turns on a display or other significant load.

The hysteresis parameters of similar SVS devices offered by other manufacturers can vary widely. In general it is better to have more hysteresis.

Since testing software-driven systems in all possible machine states can be time-consuming and costly, another means of ensuring that the system does not enter a dead loop (or infinite loop) is desirable.

The watchdog timer minimizes the likelihood of problems in an otherwise well-designed system by requiring the CPU to regularly reset the watchdog timer to zero in the course of its normal tasks. Experience suggests that a timeout period of between one and two seconds is acceptable.

If the CPU enters a dead loop, timer resets cease, and the timer causes a system reset to occur. The CPU then re-initializes, and resumes normal operation.

The integrated SVS prevents the problems described above while providing very low power consumption to the battery-powered (or battery-backup) systems that are in greatest need of an SVS.

The SVS provides the Vdd voltage sensing and delay logic, the watchdog timer logic, a manual reset input, and (optionally) complementary logic outputs.

4 Block diagram

Figure 3 shows the simplified block diagram of the TPS382x.

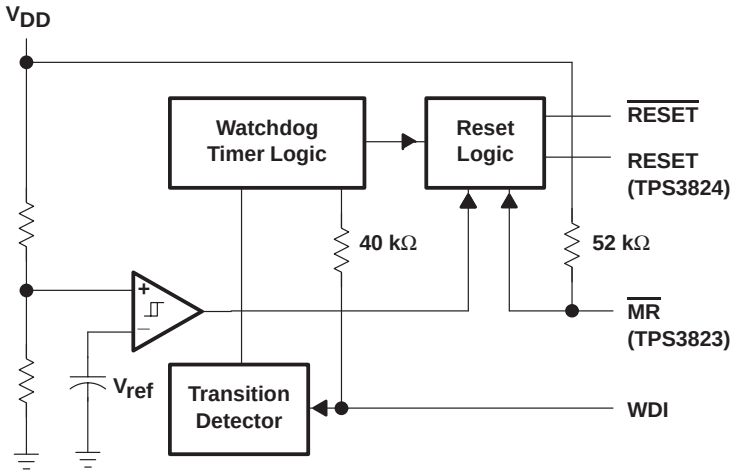

Figure 3. Simplified Block Diagram

5 TPS3823 and TPS3824 Power-on Reset

During power on the reset logic becomes active and asserts RESET when the supply voltage (V_{DD}) exceeds 1.1 V.

As long as the supply voltage remains below the positive-going threshold voltage (V_{IT+}), the reset logic remains triggered. V_{IT+} is the higher threshold of the V_{DD} sensing comparator.

This comparator hysteresis varies according to theTPS382x part type being used.

V_{IT+} can be calculated: $V_{IT+} = V_{IT-} + V_{hys}$

V_{IT-} and V_{hys} are both specified in the data sheet.

Once V_{DD} has risen above this reset threshold voltage, an internal timer starts. The timer logic then waits for 200 ms typically before the RESET output(s) return to the inactive state. This is to ensure that the V_{DD} supply has reached a usable value for long enough to ensure a clean system reset. The time delay masks out spikes in the power rail.

If V_{DD} drops below the negative-going threshold voltage V_{IT-}, the reset logic output immediately becomes active and resets the processor.

The TPS3823 has a manual reset input ($\overline{MR}$) on pin 3 in lieu of the RESET active high output of the TPS3824. This is more suitable for systems needing a manual or system-controlled reset function.

There is no $\overline{MR}$ input on the TPS3824 due to package pin count restrictions. However the choice of two reset outputs with both active-high and active-low logic increases its applicability in mixed reset level systems.

6 External Components

No external components are required for this family of SVS devices. All have fixed sense threshold voltages (V_{IT-} and V_{IT+}) set by an internal voltage divider combined with the voltage comparator hysteresis. This improves noise immunity and reduces the chance of false triggering.

Manual reset input $\overline{MR}$ activates the reset output logic to force a manual reset or an external reset from another system element.

7 Reset Logic

Either one or two (complementary) reset outputs are provided depending on part type. The single TPS3823 output is active low ($\overline{\text{RESET}}$). The TPS3824 provides active high and active low reset outputs.

Active low is inherently more reliable than active high in power-fail situations because the changing supply voltage can change the logic-high levels recognized by the other circuitry. System ground is the active low signal reference, and is unlikely to change significantly in most systems.

8 Manual Reset

Manual reset is provided only on the TPS3823. An external event pulling $\overline{MR}$ low activates the reset logic which triggers the $\overline{RESET}$ output as described above.

Figure 4 shows the relative timing. The duration of t_{pHL} is much shorter than t_d; it is measured in microseconds rather than milliseconds.

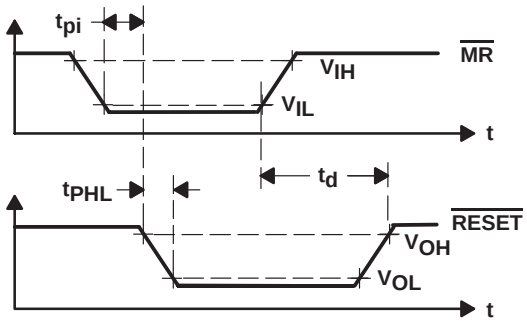

Figure 4. Timing Diagram of Manual Reset Input and $\overline{RESET}$ Output

9 V_{DD} Undervoltage

If V_{DD} falls below the levels specified in Tables 2 and 3 below, the voltage divider, comparator, and internal reference voltage detect this event and activate the reset logic.

Figure 5 shows the relationship between V_{DD} and the active low $\overline{\text{RESET}}$ output.

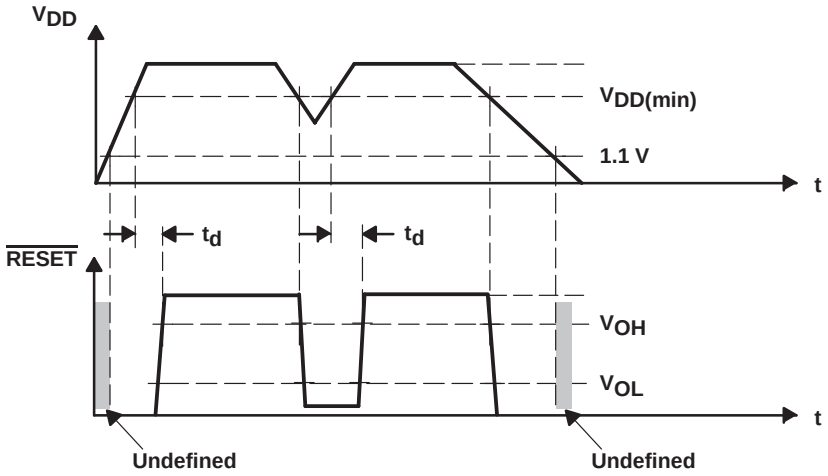

Figure 5. Timing Diagram of V_{DD} and $\overline{\text{RESET}}$ Output

When V_{DD} falls below the threshold value for the required time, a reset is produced. When V_{DD} falls below the minimum value of 1.1 V, the state of the reset output becomes undefined, since there is inadequate voltage for correct operation. Table 2 lists the nominal threshold voltages and markings for the available devices.

Table 2. Nominal Threshold Voltages and Marking

DEVICE NAME	THRESHOLD VOLTAGE	Marking
TPS3823–25DBV	2.25 V	PAPI
TPS3823–30DBV	2.63 V	PAQI
TPS3823–33DBV	2.93 V	PARI
TPS3823–50DBV	4.55 V	PASI
TPS3824–25DBV	2.25 V	PATI
TPS3824–30DBV	2.63 V	PAUI
TPS3824–33DBV	2.93 V	PAVI
TPS3824–50DBV	4.55 V	PAWI

Table 3 lists the minimum and maximum values over the working temperature range of the TPS 382x.

Table 3. Threshold Voltage Over Working Temperature Range

DEVICE NAME	TEST CONDITION	MIN	TYP	MAX	UNITS
TPS382x–25	T_A = –40°C to 85°C	2.20	2.25	2.30	V
TPS382x–30		2.57	2.63	2.69	V
TPS382x–33		2.86	2.93	3.00	V
TPS382x–50		4.46	4.55	4.64	V

The published data sheet figures are definitive, and should be used for design purposes. The figures above are provided for illustration only.

10 Watchdog Description

The TPS382x devices include a watchdog timer that must be reset periodically when it is enabled. A positive or negative transition at the WDI input triggers the reset. When the processor system fails to reset the watchdog within the nominal time out interval of 1.6 seconds, the reset output logic becomes active for typically 200 milliseconds. The watchdog timer is then re-initialized. Figure 6 shows the watchdog timing.

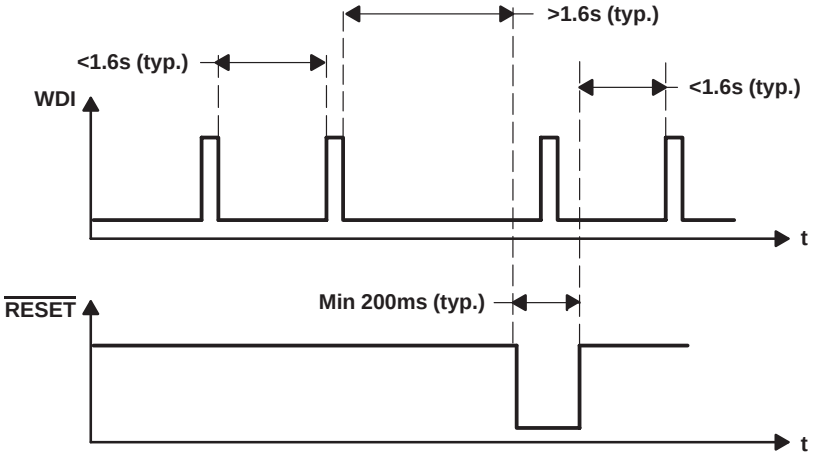

Figure 6. Functionality of the Watchdog

Disconnecting watchdog input WDI (leaving it floating), effectively deactivates the watchdog logic, because it resets itself through an internal 40-kΩ resistor before timing out; therefore, it can never activate the reset logic so long as WDI is not pulled high or low.

If WDI is pulled high or low, the transition detector zeroes the watchdog timer, and starts to count up from zero. When time-out occurs without another WDI transition, the reset logic is activated and a system reset occurs. The timeout period is approximately 1.6 seconds

Either a rising or falling edge produces a logic pulse that zeros the watchdog timer. This reduces the potential software overhead since only one transition is needed.

Watchdog input WDI may be driven by a 3-state output so that the auto–reset and active watchdog modes may be selected under system control.

The high-impedance state of the 3-state output places the watchdog in the auto-reset mode. The watchdog auto-reset will function normally provided that the leakage current from the 3-state output does not override the internal 40-kΩ resistor.

To estimate the effect of 3-state output leakage, consider the logic threshold levels of the WDI pin:

- The minimum high level input threshold is $0.7 \times V_{DD}$.
- The maximum low level input threshold is $0.3 \times V_{DD}$.

So any current in the internal 40-kΩ WDI resistor that gives rise to a voltage exceeding $0.3 \times V_{DD}$ to occur may cause the auto-reset to fail, in the worst case.

The 40-kΩ resistor value is typical, and should be used with care. The calculation below indicates the impact of 3-state leakage.

Using 40 kΩ and V_{DD} = 5 V the 3-state leakage that will produce 0.3 x V_{DD} is:

$$\frac{0.3 \times 5V}{40\ k\Omega} = 0.0375\ mA$$

When allowing for variation in the resistor value, likely drive level variations from the auto-reset logic, and the effects of capacitance, time, and temperature, it is recommended that no more than 10 μA leakage from a 3-state output be specified. The capacitive load on the WDI pin should not exceed 200 pF.

The watchdog input WDI is unusual in that it has an internal connection to the auto-reset logic through a 40-kΩ resistor. Therefore the input current varies depending on the state of the auto-reset logic.

When the auto-reset logic is high, the WDI pin sources current through the 40-kΩ resistor. When this logic is low, the resistor sinks current.

Hence the data sheet specifies WDI I_H average as 120 μA when WDI = V_{DD} as a time average, dc = 88%.

Similarly the I_L value for WDI = 0.3 V_{DD} is specified as –15 μA at 12%.

The duty cycle of the 3-bit WDI auto-reset timer keeps the output level low for the first 7/8 of the cycle and high for the remaining 1/8 of the cycle.

Holding the WDI pin high therefore draws current through the 40-kΩ resistor for the greater part of the watchdog cycle. To minimize the current drawn, it is best to leave the WDI input low for the majority of the cycle. Figure 7 shows the timing relationships for the internal and external watchdog signals.

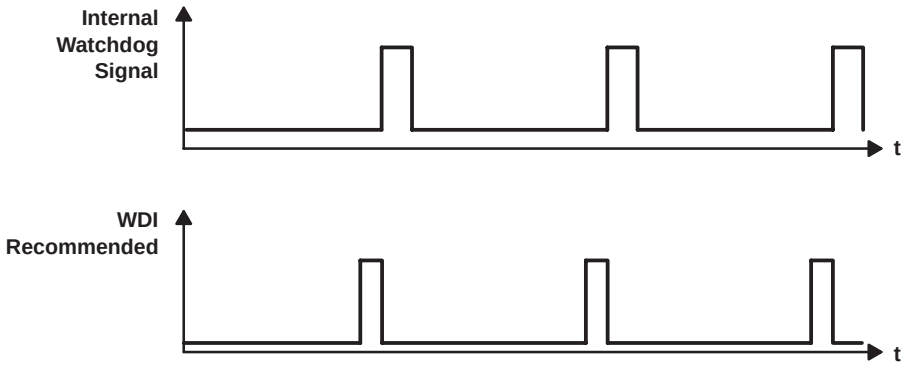

Figure 7. Timing of the Internal and External Watchdog Signal

11 Resetting a Microcontroller

In a simple system the watchdog may not be needed, and WDI can safely be left floating. This causes the watchdog to auto-reset through the 40-kΩ resistor before the reset logic outputs are enabled.

Figure 8 shows the V_{DD} voltage supervision functions within a microprocessor system. No external components are needed for the TPS3823 to provide these functions, and there is no software investment or additional software testing. Compared to a conventional manual reset with pull-up, this low-cost subsystem provides equal control over false resets and undervoltage problems.

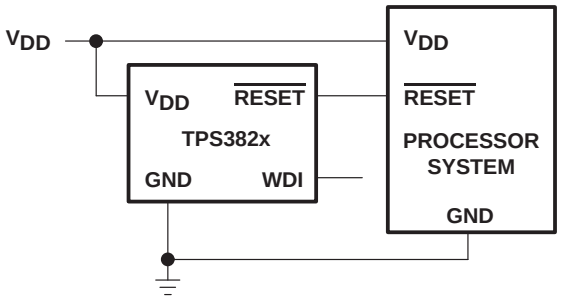

Figure 8. TPS382x Application

Figure 9 looks similar to Figure 8, but it represents a radically different system approach. Connecting WDI to a processor output (O/P) enables the WDI watchdog input. If the processor fails to toggle O/P from high to low or low to high within 1.6 seconds after each preceding toggle, the TPS382x activates its reset logic and resets the processor.

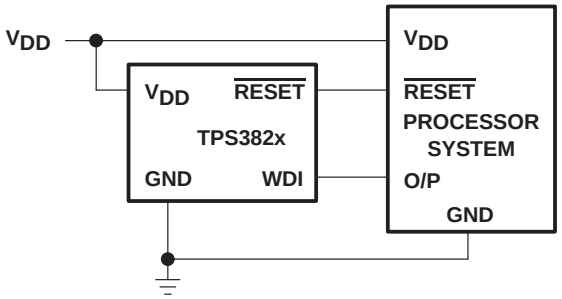

Figure 9. TPS382x System using WDI

This requires an investment in software development and testing, but it ensures a system reset if a dead loop in the main code fails to trigger the watchdog on time. Then the re-initialized processor can attempt to clear the problem.

Dead loops can occur through faulty coding (all loops should be positively terminated), but potential dead loops can occur in the increasingly complex software tasks that are routinely undertaken today.

Induced noise in a system can cause an address or instruction to be misread; the processor then makes a jump into unknown territory, tries to execute data as code, and ends in a loop.

In either case the watchdog will cause a reset to occur, and the processor can recover.

Figure 10 shows the TPS3823 with a manual reset input, $\overline{MR}$, that includes an internal pullup resistor. The $\overline{MR}$ input can be used with an external pushbutton to provide a manually-controlled reset, or it can be driven by an external logic level.

This allows an external device or system to control the reset function through the TPS3823.

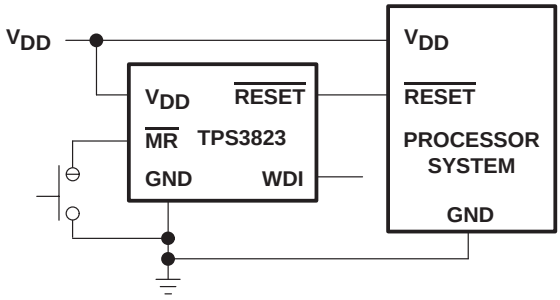

Figure 10. TPS3823 System

12 TPS3824

Figure 11 shows the TPS3824 in a system where a processor peripheral needs a reset signal that is active high.

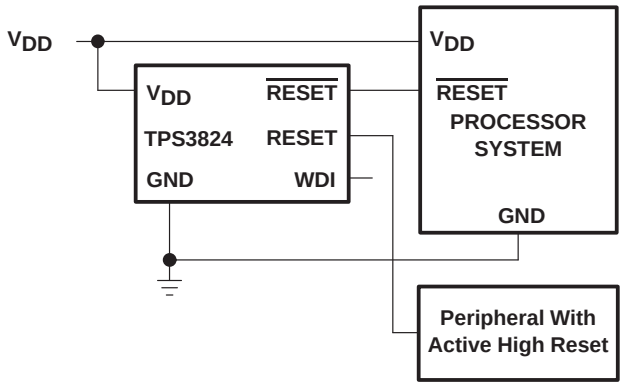

Figure 11. TPS3824 System

13 Layout Rules

Figure 12 shows the standard CMOS structure of the TPS382x. The devices are not unusually sensitive to induced noise, but it is still useful to consider the implications of noise on this critical part of the system.

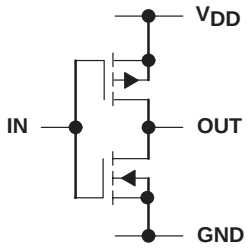

Figure 12. CMOS I/O Structure

In general it is best to keep noisy signals (clock signals, data or address buses) away from critical areas. If this cannot be done, then it is best for the noisier PCB tracks to cross any sensitive input tracks at right angles. Avoid extended parallel runs.

A 100-nF decoupling capacitor is recommended between V_{DD} and ground to further reduce the effect of power supply noise spikes.

Using $\overline{\text{RESET}}$ rather than RESET for critical (noisy) PCB areas is preferable to take advantage of the better potential noise immunity of the active low signal.

It is advisable to check for induced noise spikes on both the WDI (if used) and $\overline{\text{MR}}$ inputs. A false $\overline{\text{MR}}$ will reset the system, which will be immediately obvious, but a consistently false WDI signal will not become evident until there is a software dead loop or similar fault event and the watchdog fails to reboot the system.

It is important therefore, to check that the watchdog works reliably in the presence of the working environmental system noise. Many systems, which work well on the bench can have problems in the field when, for example, an inductive load is connected to a control system.

Despite the high (40-kΩ) input impedance of the floating WDI, it is unlikely to present a problem, since it is in this case perpetually self-resetting. Any induced noise that might cause additional watchdog counter resets to zero should not alter the $\overline{\text{MR}}$ or V_{DD} undervoltage triggers for the reset logic.

14 Summary

The TPS3823/3824 family of supply voltage supervisors addresses the problems of system initialization, power brownout, noisy power feed and software dead loops.

It does this by means of a V_{DD} sensing comparator with hysteresis, reset delay logic and a watchdog timer that is edge triggered. A manual reset input is available on the TPS3823, and both active-high and active-low reset on the TPS3824.

A range of parts is offered with threshold voltages suitable for nominal supply voltages between 2.5V and 5.0V. They are supplied in the 5-pin SOT23-5 package for minimum footprint on the application PCB.

No external components are required for full functionality.

15 References:

TPS3823/3824 data sheet, SLVS165, Texas Instruments.

TL77xx applications information, SLVAE04, Texas Instruments

TLC77xx applications information, SLVAE03, Texas Instruments

These are available for download from:

http://www–s.ti.com/sc/docs/psheets/pids2.htm