

Fundamental Theory of PMOS Low-Dropout Voltage Regulators

ABSTRACT

Most linear modern linear regulators use a PMOS architecture. This document covers the key characteristics of a PMOS LDO and the theory behind these linear regulators.

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1 Fundamentals

A voltage regulator is a constant voltage source that adjusts its internal resistance to any occurring changes of load resistance to provide a constant voltage at the regulator output.

The internal resistance of a constant voltage source (Figure 1) must be significantly smaller than the external load resistor ($R_{IN} \ll R_{LOAD}$) to ensure a constant output voltage over a certain range of load changes.

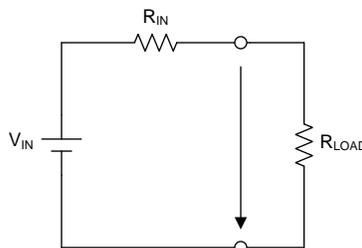


Figure 1. Constant-Voltage Source

The output voltage of a voltage source is calculated as Equation 1:

$$V_{OUT} = V_{IN} \times \frac{1}{1 + \frac{R_{IN}}{R_{LOAD}}} \tag{1}$$

Under a no-load condition ($R_{LOAD} = \infty$), the maximum output voltage possible is equal to the input voltage ($V_{OUT-MAX} = V_{IN}$). As the load increases, the output voltage drops from its maximum value and introduces an output-voltage error E_{VO} . This error E_{VO} is defined as the percentage difference between V_{OUT} under no-load condition ($V_{OUT-MAX}$), and V_{OUT} under load condition ($V_{OUT-LOAD}$), as described by Equation 2.

$$E_{VO} = \frac{V_{OUT-MAX} - V_{OUT-LOAD}}{V_{OUT-MAX}} \tag{2}$$

When replacing $V_{OUT-MAX}$ with V_{IN} and substituting $V_{OUT-LOAD}$ with the value in Equation 1, the voltage error is expressed through the resistor ratio of R_{IN} to R_{LOAD} , as given by Equation 3:

$$E_{VO} = \frac{R_{IN}}{R_{IN} + R_{LOAD}} \tag{3}$$

A plot of the voltage error over a series of R_{LOAD} -to- R_{IN} ratios confirms that the output voltage error E_{VO} increases with decreasing load resistance R_{LOAD} , as shown in Figure 2.

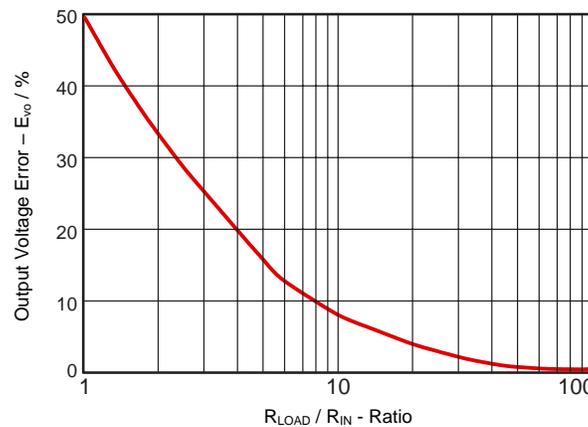


Figure 2. Output-Voltage Error vs Load Resistance

To minimize the error we need a circuit that senses any occurring load changes and, via some kind of feedback, adjusts a variable internal resistor to keep a constant ratio of internal-resistance to load-resistance, as described by Equation 4.

$$R_{IN} = R_{LOAD} \times k \tag{4}$$

When the relationship described in Equation 4 is true, R_{IN} then follows R_{LOAD} in a linear relation, as given by Equation 4. This circuit is shown in Figure 3.

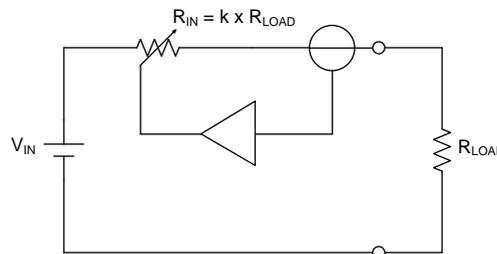


Figure 3. Linear Relation Between R_{IN} and R_{LOAD}

A circuit that achieves this relationship through adjusting the a variable resistor is basically a linear-voltage regulator, and is shown in [Figure 4](#).

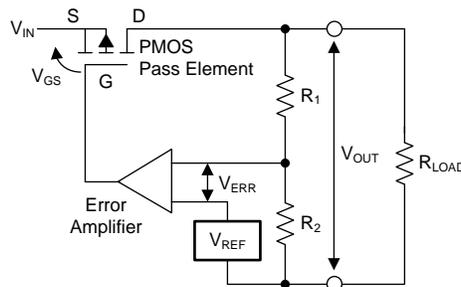


Figure 4. Basic Linear-Voltage Regulator

In the linear-voltage regulator shown in [Figure 4](#), we can identify the building blocks discussed in the following sections.

1.1 Voltage Reference, V_{REF}

The voltage reference is the starting point of all regulators. This reference is usually a band-gap-type because this kind of reference has the ability to work down to low supply voltages, and provides enough accuracy and thermal stability to meet the less-stringent performance requirements of regulators. Band-gap references typically have an initial error of 0.5% to 1.0% and a temperature coefficient of 25 ppm/°C to 50 ppm/°C.

1.2 Error Amplifier

The error amplifier takes a scaled-down version of the output [$V_P = V_{OUT} R_1 / (R_1 + R_2)$], compares it against the reference voltage ($V_P = V_{REF}$), and adjusts V_{OUT} via the series-pass element to the value required to drive the error signal ($V_{ERR} = V_P - V_{REF}$) as close as possible to zero. Setting $V_{REF} = V_P$ yields [Equation 5](#):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right) \quad (5)$$

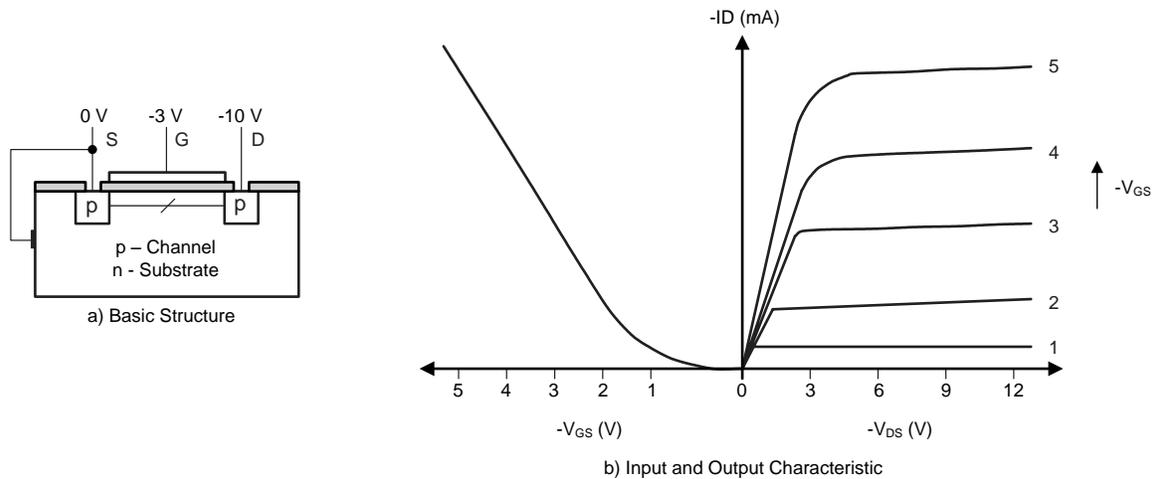
This calculation holds true only if V_{IN} is sufficiently high to keep the error amplifier and the pass element from saturating.

1.3 Feedback Network

The feedback network scales V_{OUT} to a value suitable for comparison against V_{REF} by the error amplifier. Because V_{REF} is fixed, the only way to program the value of V_{OUT} is by adjusting the ratio R_2 / R_1 .

1.4 Pass Element

The series-pass element boosts the output-current capabilities of the error amplifier to the higher levels required by the load. This process involves transferring large currents from the source V_{IN} to the load under the low-power supervision of the error amplifier. A suitable pass element to carry out this task is a PMOS enhancement FET. A PMOS FET has the two p-islands for the source and the drain terminals embedded in an n-substrate; see [Figure 5a](#). The substrate is connected to the source, which usually has the most positive potential. The drain receives the most negative potential. As the PMOS name indicates, the device uses p-type conductivity, which is established by applying a voltage to the gate that is negative relative to the source. The holes, which are the minority carriers in the n-substrate, are attracted by the negative gate electrode. Moving towards the upper region between the two p-islands, the holes now become free-charge carriers, establishing a p-conductive bridge between source and drain. This way, the conductivity of the bridge, and with it the drain current I_D , are controlled by the gate-source voltage, V_{GS} . Because this type of FET enhances its conductivity with increasing V_{GS} , it is called an enhancement or normally-off type ([Figure 5b](#)).


Figure 5. PMOS Enhancement FET

2 Regulator Sequence

This section describes the regulation sequence when R_{LOAD} drops as illustrated in [Figure 6](#). [Figure 7](#) depicts how the regulation sequence described relates to the internal LDO blocks.

When the load resistance drops, the output voltage falls from V_{OUT1} to V_{OUT2} , and the voltage across the pass element rises from $-V_{DS1}$ to $-V_{DS2}$. V_P (which is a scaled-down version of V_{OUT}) falls significantly below V_{REF} causing the gate-source voltage to jump from $-V_{GS1}$ to $-V_{GS2}$.

The PMOS FET now conducts harder, increasing the output current from I_{OUT1} to I_{OUT2} . The output voltage and, by virtue of V_P , the error voltage start to recover. The gate voltage increases gradually to $-V_{GS3}$, thus causing the increased output current I_{OUT3} to generate an output voltage V_{OUT} . When this output voltage is scaled down via R_1 and R_2 , the result is a zero-error voltage $V_{ERR} = 0$.

The output characteristic illustrated in [Figure 8](#) confirms the regulation sequence. When R_{LOAD} drops, the PMOS FET operating point jumps from P_1 to P_2 and then regulates to P_3 .

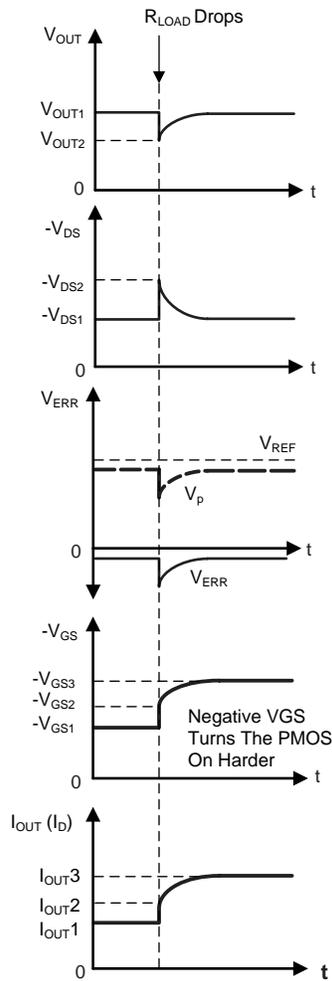


Figure 6. Regulation Sequence When RLOAD Drops

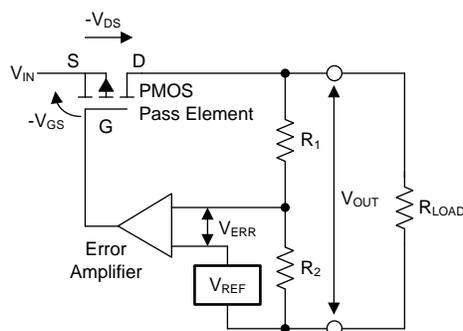


Figure 7. Regulator Block Diagram

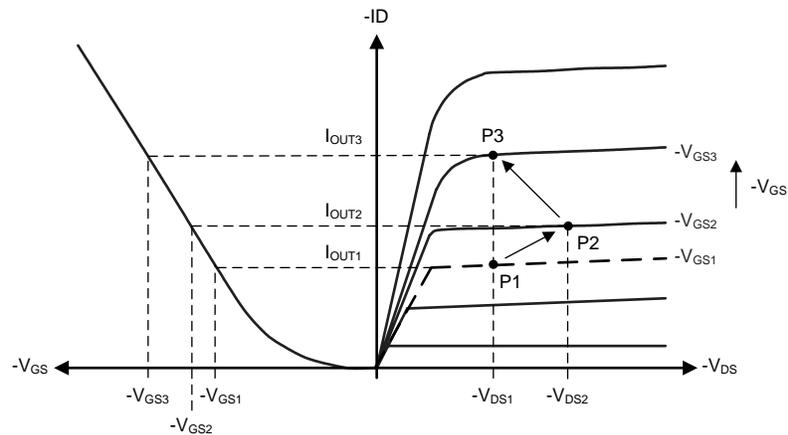


Figure 8. PMOS Input/Output Characteristic

For a given quiescent point P_N where the output voltage is stabilized (that is, V_{OUT} and V_{DS} are constant), we can define the internal resistance of the PMOS FET, and the load resistance in general terms as described in Equation 6:

$$R_{INN} = \frac{V_{DS}}{I_{OUTN}}$$

and

$$R_{LOAD} = \frac{V_{OUTN}}{I_{OUTN}}$$

Solving both equations for I_{OUT} yields:

$$I_{OUTN} = \frac{V_{DS}}{R_{INN}}$$

Solving for R_{IN} results in:

$$I_{OUTN} = R_{LOAD} \times \frac{V_{DS}}{V_{OUT}}$$

(6)

With $k = V_{DS}/V_{OUT}$, Equation 6 provides the linear relation required by a linear voltage regulator.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 1999) to A Revision	Page
• Added <i>Abstract</i> section	1
• Changed document format	1
• Added text references for all figures and equations	1

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