

Using the TPS5602 for Powering DSPs

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ABSTRACT

The synchronous buck converter controllers (TPS56100, TPS56300, TPS56xx, and TPS5602) made by Texas Instruments are specifically designed to provide excellent transient response and high efficiency to the microprocessor power applications such as the TMS320C6000 and TMS320C5000 families from TI, as well as similar digital loads. In addition, hysteresis control method is used such that power supply designers do not have to worry about the stability and compensation issues.

1 Introduction

The TI TPS5602 (a dual-channel synchronous buck switch-mode power supply controller) features very fast feedback control and dual channels. The up and down power sequencing can be easily achieved by setting the standby pins, since both channels are independent. The wide input voltage and adjustable output voltage make the TPS5602 suitable for many applications.

1.1 TPS5602 Operating Conditions

Table 1. Summary of the TI Synchronous Buck Converter Controller and EVM Characteristics

	V_I RANGE (POWER STAGE)	V_{CC} RANGE (CONTROLLER)	V_O RANGE (POWER STAGE)	I_{O, MAX}[†] (POWER STAGE)	DRIVER CURRENT (CONTROLLER)	OTHERS
TPS56100	4.5 ~ 6 V	4.5 ~ 6 V	1.3 to 2.6 V	7 A	2 A	1 channel
TPS56300	2.8 ~ 5.5 V	2.8 ~ 5.5 V	1.3 to 3.3 V	4 A for RR 6 A for LDO	2 A	2 channels
TPS56xx	4.5 ~ 6 V	12 V	1.5V, 1.8 V, 2.5 V, or 3.3 V	8 A	2 A	1 channel
TPS5602	4.5 ~ 25 V	4.5 ~ 25 V	Adjustable	4 A/channel	1.2 A at V _O = 3 V	2 channels

[†] The current capability can be extended if the switching devices are added in parallel; see Table 2 in TI TPS56100/56300 datasheets.

1.2 Key Features

- Independent Dual Channels
- Hysteretic Control for Fast Transient Response
- Adjustable Output Voltage Down to 1.2 V
- Minimized External Component Count
- Synchronous Rectifier Enables Efficiencies of >95%
- Separate Standby Control and Over Current Protection
- Low Supply Current . . . 0.8 mA Typ
- 30-Pin TSSOP
- Low Standby Current (1 uA maximum)
- EVM Available (TPS5602EVM-121)
- Driver current (1.2 A at V_O = 3 V)

2 Application Circuit

Figure 1 shows a typical circuit design using the TPS5602, which features a dual-channel synchronous buck converter (1.8-V and 3.3-V outputs). The two output voltages are independent and can be adjustable (1.2-V to approximately input voltage) by using the sampling resistors such as R1, R2, R3, and R4. The output voltages, OUT1 and OUT2, are set with the following equations, where the reference voltage is 1.185 V:

$$V_{OUT1} = \left(1 + \frac{R3}{R2}\right)V_{ref} \quad (1)$$

$$V_{OUT2} = \left(1 + \frac{R4}{R1}\right)V_{ref} \quad (2)$$

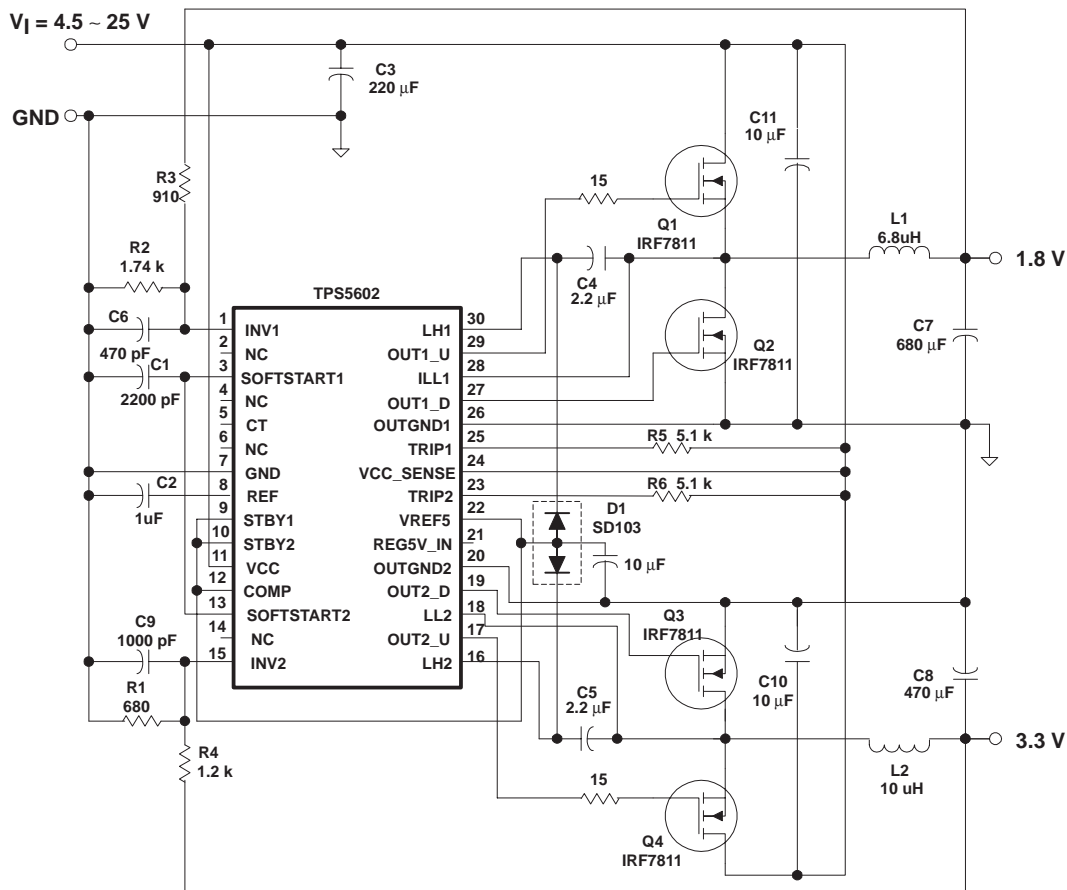


Figure 1. Typical Design Circuit Using TPS5602

Figure 2 shows the TPS5602 transient response. The response is less than 2 microseconds after a load is applied. Conventional PWM buck converters exhibit approximately 100 microseconds of response.

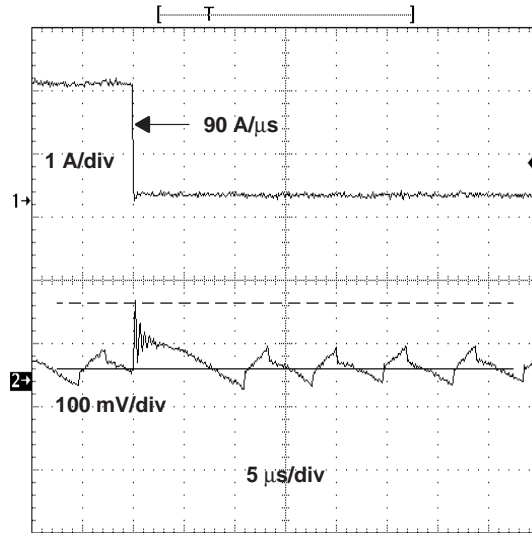


Figure 2. Fast Load Transient Responses

Figure 3 and Figure 4 show the efficiency of the two controllers over load up to 5 A.

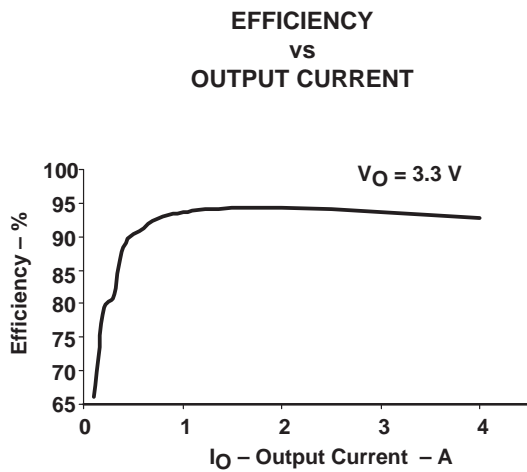


Figure 3. Efficiency of 3.3 V Output

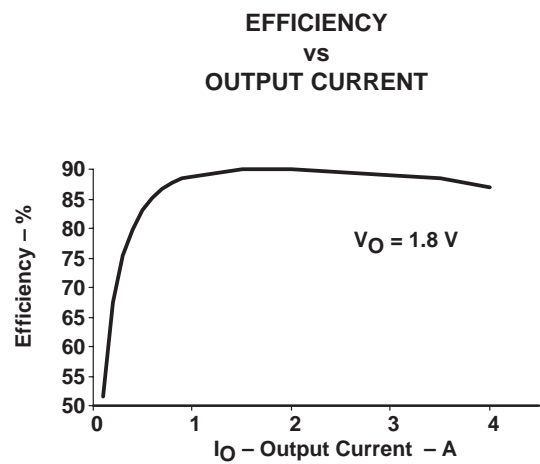


Figure 4. Efficiency of 1.8 V Output

Table 2 shows the setting values of the TPS5602 to generate the output voltages 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

Table 2. Summary of Setting Values for TPS5602 1.5/1.8/2.5/3.3 V Outputs

OUTPUT VOLTAGE (V)	R2 (or R1) (Ω)	R3 (or R4) (Ω)
3.3	680	1.2k
2.5	1k	1.1k
1.8	1.74k	910
1.5	10k	2.67k

3 Power Supply Solutions

The power solutions for 1.8 V core and 3.3 V I/O using TPS5602 are shown in Figures 5.

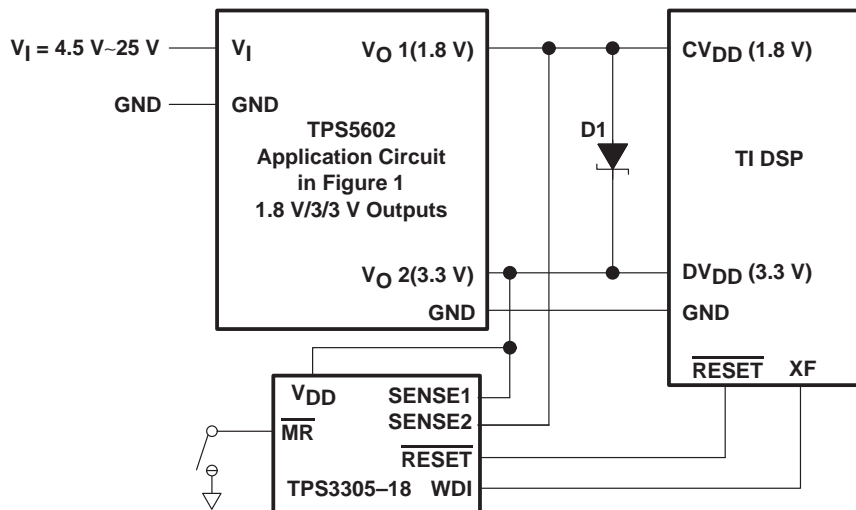


Figure 5. TI DSP Power Supply Solutions Using TPS5602

NOTE: TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to insure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long term reliability of the device. System level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers.

There is a simple solution to meet the power sequencing recommendation. By using the SOFTSTART1 and SOFTSTART2 pins in Figure 1, the start-up sequencing (core voltage first, then peripheral voltage) can be easily achieved. The softstart timing can be adjusted by selecting the softstart capacitor value such as C1 and C12 shown in Figure 1. The equation is:

$$C_{\text{softstart}}(\mu\text{F}) = 2 \times T_{\text{softstart}}(\text{ms}) \quad (3)$$

where $C_{\text{softstart}}$ is the softstart capacitance; $T_{\text{softstart}}$ is the start-up time.

For example, to set the start-up time $T_{\text{softstart1}} = 5 \text{ ms}$ and $T_{\text{softstart2}} = 10 \text{ ms}$, the capacitance value of $C_{\text{softstart1}} = 0.01 \mu\text{F}$ and $C_{\text{softstart2}} = 0.02 \mu\text{F}$ are needed. Figure 6 shows the start-up sequencing. In addition, the TPS5602 has two external pins (STBY1, STBY2) that can be alternatively used for power-up sequencing.

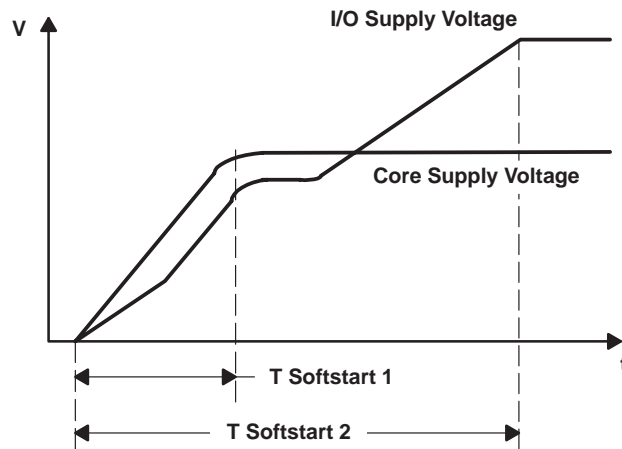


Figure 6. Start-Up Sequencing

The Schottky diode D1 provides a measure of protection during the power-down sequence and during other periods when the DV_{DD} supply is below the CV_{DD} supply by limiting the $CV_{DD} - DV_{DD}$ voltage to the forward drop of D1.

The two power supplies should be placed close to the DSP to minimize the trace resistance and inductance and to minimize the ground loop current between the two output grounds. This ground loop current can generate radiated EMI noise that can adversely affect any circuitry within the loop. The ground connection must be made directly on the DSP to help minimize the problem.

4 References

For detailed information;

Data sheet and EVM Board; <http://www-s.ti.com/sc/psheets/slvs217/slvs217.pdf>

SVS application note; <http://www-s.ti.com/sc/psheets/slva056/slva056.pdf>

Application note; http://www.ti.com/sc/docs/apps/analog/power_management.html

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