

# **Power-Supply Solutions for Multivolt Altera FLEX 10KE and APEX 20K/KE FPGAs**

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## **ABSTRACT**

This report is a reference for design engineers inexperienced with multivoltage devices but who are using Altera 2.5-V and 1.8-V multivoltage APEX 20K/20KE and FLEX 10KE field-programmable gate array (FPGA) products.

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## 1 Introduction

Many devices such as DSPs, microprocessors, and field-programmable gate arrays (FPGAs) are designed to consume minimal power while still providing very high performance at low cost. They achieve this by using geometrically smaller-scale on-chip circuitry. These smaller geometries need lower operating voltages but, for correct operation, they frequently require multivoltage power-supply support.

Texas Instruments has a complete line of power-supply devices suitable for most current Altera APEX FPGA families. This application report discusses the following topics concerning the APEX 20K/20KE and FLEX 10KE families:

- Core and I/O requirements
- Issues associated with multivoltage components
- How to estimate load currents,  $I_{CC(INT)}$  and  $I_{CC(IO)}$
- Options for supply voltage regulation
- TI-recommended solutions for power management

## 2 APEX Core and I/O Voltage Requirements

APEX 20K/20KE and FLEX 10KE family core- and I/O-supply-voltage requirements are summarized in Table 1. The core voltage listed is required for correct internal operation. The required I/O voltage is more flexible and depends on the particular needs of a system interface.

APEX and FLEX devices support 5-V tolerant I/Os as well as many different output types such as LVTTTL, CMOS, LVDS, PCI, LVPECL, SSTL, HSTL, AGP, GTL, GTL+, and CTT.

**Table 1. FLEX 10KE and APEX 20K/20KE Core and I/O Voltage Requirements**

DEVICE	$V_{CC(INT)}$ (V)	$V_{CC(IO)}$ (V)
EPF10KE	2.5	3.3, 2.5
EPF10KS	2.5	3.3, 2.5
EPF20K	2.5	3.3, 2.5
EPF20KE	1.8	3.3, 2.5, 1.8

## 3 Multivolt Device Issues

Smaller feature sizes are driving the need for dual-voltage-rail ICs. When designing with these types of components, be aware of potential issues such as latch-up and device electrical stressing. Latch-up can occur when a device operates in a voltage range that brings about functional uncertainties, putting all (or part) of the device into an unknown state. An example is hot card insertion when the card is plugged into an active system before the power supply can

provide current to the device's  $V_{CC}$  and ground planes. In this situation, larger-than-normal currents can be present on the device because of the creation of low-impedance paths from  $V_{CC}$  to ground, which can lead to electrical damage and device failure.

Electrical overstressing can also occur when incorrect  $V_{CC}$  power sequencing up and down occurs between the different power rails. In multirail devices, differing voltages present the possibility of higher voltages being placed on the gates to the drivers of the I/O. Internal parasitic structures can conduct, reinforcing themselves until potentially destructive conductive currents are produced. These higher voltages across I/O or other pins can lead to abnormal stresses being placed on the oxide levels of the device. The net effect is potentially long-term reliability problems. Such conditions can be avoided if the issues are understood and correct design techniques are used, including:

- Understanding the characteristics of other components in the system, as well as the system power management control implemented
- Correct power-up and power-down sequencing of the core and I/Os
- Correct device power ramp up
- Meeting any special conditions and recommendations for a device

### 3.1 Recommendations for the APEX and FLEX Series of Altera FPGAs

The following points provide guidance in the application of APEX and FLEX devices:

- The core ( $V_{CC(INT)}$ ) and I/O planes ( $V_{CC(IO)}$ ) on Altera FPGAs can be powered in any order.
- $V_{CC}$  must rise monotonically and reach the correct operating level within 100 ms. Slower rise times can cause incorrect device initialization and functional failure.
- For the 10KE FLEX devices, ensure that the STATUS and CONF\_DONE pullup resistors are connected to the same voltage as the configuration device. This avoids driving signals into a configuration device that is not powered.
- Devices can be driven before power up with no damage to the device. Devices that do not support hot-socketing can be damaged if the pins are driven before the device is powered up.
- Devices do not drive out before or during power up. I/O pins are held in a high-impedance state during power up and configuration. Devices that do not support hot-socketing may cause contention by driving out during power up.
- Signal pins do not drive the  $V_{CC(IO)}$  or  $V_{CC(INT)}$  power supplies. There is no current path for the I/O, dedicated input, or dedicated clock pins to the VCCIO or VCCINT pins before and during power up and therefore these devices cannot be powered up through the I/O pins.

## 4 Load Current Estimation

Load current estimates derived from graphs contained in the 1999 Altera data book are summarized for each Altera FPGA family of devices (Tables 2 – 6). These values are typical for powering the device cores. To obtain the most accurate estimate, consult the Altera data book and derive the estimate based on the design requirements, using the power estimation equations provided. Altera recommends the following steps:

1. Estimate the power consumption of the application using the power estimation formula provided in each data sheet.
2. Calculate the maximum power for the device and package.
3. Verify that the estimate falls below the maximum power value.

### 4.1 Formulas and Assumptions

Power consumption consists of the power used internally to maintain the device on standby and for switching logic elements (collectively,  $P_{INT}$ ) which draw from the  $V_{CC}$  plane, and the power used for actively switching output loads,  $P_{IO(OUT)}$ . Internal power is easily related to current draws from  $V_{CC}$ :

$$P = P_{INT} + P_{IO(OUT)} = (I_{CC(STANDBY)} + I_{CC(ACTIVE)}) \times V_{CC} + P_{IO(OUT)} \quad (1)$$

$I_{CC(ACTIVE)}$  depends on the switching frequency, the number of logic elements used, K-factors unique to that family, and the fraction of logic elements switching at one time. This is the dominant contributor to core power usage. Under no-load conditions,  $I_{CC(STANDBY)}$  has a maximum value of 10 mA; under load, values can be found in the individual device data sheets. This current is very small compared to  $I_{CC(ACTIVE)}$  and it can be ignored in estimating.

The power usage for switching output loads,  $P_{IO(OUT)}$ , depends on the characteristics of the output loads and on the switching frequency. The power dissipated by the I/O buffers to maintain steady-state outputs,  $P_{DC(OUT)}$ , must be added to the power used for switching other frequently-switched output loads,  $P_{AC(OUT)}$ . The steady-state component  $P_{DC(OUT)}$  is relatively small compared to the power used for load switching when the output loads are capacitive or are CMOS inputs. In such situations,  $P_{DC(OUT)}$  can be ignored in estimating; otherwise, contributions from all the steady-state outputs, the logic levels they drive, and the resistive load on each output must be included.

If only CMOS inputs are being driven, there are no steady-state loads and Equation (1) simplifies:

$$P = P_{INT} + P_{IO(OUT)} = I_{CC(ACTIVE)} \times V_{CC} + P_{IO(OUT)}$$

The following equations apply to estimating current drains for switching internal logic elements and output loads, respectively, for APEX 20K/20KE and FLEX 10K/10KE FPGAs:

$$I_{CC(ACTIVE)} = f_{\max} K n_{LE} a_{LE} I_{LE}$$

$$I_{AC(OUT)} = \frac{1}{2} n_{out} C_{avg} V_{max} a_{IO} f_{IO}$$

The symbols in these equations have the following meaning:

- $a_{IO}$  = Percentage of output loads toggling at each clock cycle
- $a_{LE}$  = Percentage of logic elements toggling at each clock cycle
- $C_{avg}$  = Average capacitive load of all outputs
- $f_{max}$  = Maximum operating frequency
- $f_{IO}$  = I/O toggle frequency
- $q_{LE}$  = Charge used by a single logic element to switch its state
- $K$  = Constant
- $n_{LE}$  = Total number of logic elements in the array
- $n_{out}$  = Total number of output and bidirectional pins
- $V_{max}$  = Maximum output voltage

Values of  $K$  and  $I_{LE}$  are device dependent and can be found in individual Altera data sheets for the particular device in question.

## 4.2 Estimated Internal Core and External Switching Currents

Internal core and external switching currents were estimated based on the following assumptions and approximations:

- Output capacitive loads are all 35 pF.
- Percentage of outputs instantaneously switching is 25.
- Average percentage of internal elements toggling at each clock is 12.5.
- There is >85% usage of internal logic elements and/or macros in the device.
- Single core clock frequencies were selected to generate  $I_{CC(INT)}$  data.
- For estimating  $I_{CC(ACTIVE)}$ , standby currents were omitted.
- For estimating  $I_{IO(OUT)}$ , the dc-component  $I_{DC(OUT)}$  was ignored because the estimates use capacitive loads.

### 4.2.1 Internal (Core) Currents

The *estimated* internal (core) currents at four frequencies are shown in Table 2 for the EPF10KE and EP20K/20KE devices.

**Table 2. Estimated Internal Current Draw for EPF10KE and EP20K/20KE Families**

	V <sub>CC(INT)</sub> (V)	NUMBER OF LOGIC ELEMENTS	CURRENT (mA) @ 33 MHz	CURRENT( mA) @ 50 MHz	CURRENT (mA) @ 100 MHz	CURRENT (mA) @ 150 MHz
<b>EP10KE</b>						
EPF10K30E	2.5	1728	32	64	97	146
EPF10K50E	2.5	2880	57	114	173	259
EPF10K100E	2.5	4992	93	185	281	421
EPF10K100B	2.5	4992	103	206	312	468
EPF10K130E	2.5	6656	126	253	383	574
EPF10K200E	2.5	9984	198	395	599	899
EPF10K200S	2.5	9984	189	379	574	861
<b>EP20K/20KE</b>						
EP20K60E	1.8	2560	34	68	102	154
EP20K100	2.5	4160	105	209	317	476
EP20K100E	1.8	4160	55	110	166	250
EP20K160E	1.8	6400	84	169	256	384
EP20K200	2.5	8320	227	453	686	1030
EP20K200E	1.8	8320	110	220	333	499
EP20K300E	1.8	11520	152	304	461	691
EP20K400	2.5	16640	487	975	1477	2215
EP20K400E	1.8	16640	220	439	666	998
EP20K600E	1.8	24320	321	642	973	1459
EP20K1000E	1.8	38400	507	1014	1536	2304
EP20K1500E	1.8	51840	684	1369	2074	3110

### 4.2.2 Load Switching Currents

The APEX and FLEX series have user-selectable support for LVTTTL, LVCMOS, SSTL-2, SSTL-3, GTL+, AGP, CTT, and LVDS interface standards. For simplicity, these calculations are based on using LVTTTL I/Os with 3.3-V levels and a 66-MHz clock. Using other types of I/O can significantly increase the load switching current values shown in Table 3.

**Table 3. Estimated External Load Switching Currents**

	NO. I/O	144 TQFP	208 PQFP	240 PQFP	256 BGA†	356 BGA†	484 BGA†	599 PGA	600 BGA	672 BGA†			
<b>EP10K</b>													
EPF10K30E	220	49	71		84		105			105			
EPF10K50E	254	49	71	82	91	105	121			121			
EPF10K100E	338		71	82	91	131	161			161			
EPF10K100B	191		71	82	91								
EPF10K130E	424		82			131	176		202	223			
EPF10K200S	470					131	176	224	224	224			
	NO. I/O	144 TQFP	208 PQFP	240 PQFP	144 BGA†	324 BGA†	356 BGA	484 BGA	652 BGA	655 BGA	672 BGA†	984 PGA	1020 BGA†
<b>EP20K</b>													
EP20K60E	204	44	72	88		97	97	97			97		
EP20K100	252	53	76	90		120	120	120			120		
EP20K100E		44	72	87		117	117	117			117		
EP20K160E	316	42	69	83			130	133			133		
EP20K200/200E	382		69	83			133	182			182		
EP20K300E	408		57	72				194			194		
EP20K400/400E	502								239	239	239		239
EP20K600E	624								233		242		280
EP20K1000E	716								233		242	337	337
EP20K1500E	808								233			385	385

† Fine line BGA

## 5 Supply Voltage Regulator Options

Power supply to the core and I/O requires a 3.3-V, 2.5-V and at times a 1.8-V regulator. Depending on key system requirements, and the cost and time to market, the solution can be a linear regulator, a switching regulator, or a switching power-supply module. Trade-offs of the linear- and switching-regulator power supplies are outlined in the following.

### 5.1 Linear Regulators

Sometimes linear voltage regulators are the most cost effective in terms of the total system cost. They should be used when:

- Board space is critical.
- Low output noise is important (EMI or ripple).
- Efficiency is not critical.
- Simplicity of design is preferred.
- Only low to medium output currents are needed.

- Fast responses to inputs and transients are required.
- The application is a step-down.

In typical applications, a linear regulator requires an input capacitor to reduce the effects of a trace inductance and any noise present on the input of the low-drop-out regulator (LDO). This is usually placed as close as possible to the regulator input pin. The LDO also requires an output capacitor to handle the system transient response and for stability. Its size and effective series resistance (ESR) affect both stability under load and the ability to respond to transients caused by rapid changes in load current. The size of this input capacitor and the ESR must be adjusted according to the required system accuracy. For high frequency applications, a small ceramic bypass capacitor at the output is recommended to help reduce any high frequency noise.

Some of the more recent members of the TPS family of LDO linear regulators from TI offer flexibility by allowing the user to select any capacitor type (small size, low ESR) to address the system needs. At times, lower- and higher-valued capacitors can be placed in parallel to deal with fast transient current spikes better and to reduce the overall ESR.

Additional functions such as on/off control (enable) and under-voltage detection (voltage supervisors) have been integrated on-chip and are available in certain families from TI.

Dual output devices available in medium- to high-output currents are available, too.

## 5.2 Inductive Switching Regulators

Switching supplies are known to have excellent efficiency, but their output is noisy. This degrades regulation and performance which, at times, is critical, especially when powering analog circuits. Inductive switching regulators should be used when:

- Efficiency is critical (80 – 95%).
- The application has a wide input voltage range.
- Larger output currents are required.
- Board space is not a major concern.
- Cost is a secondary issue.
- The application is stepup, stepdown, or inverting.
- Noise is not of major concern.

Switching regulator solutions require inductors, input capacitors, and output capacitors for dc-dc conversion. For ac-dc conversion, isolation transformers with rectification are required. The TI/Unitrode line of PWMs provides solutions for these types of applications, but they are not covered in this report.



### 5.3 Inductive Switching Power-Supply Module

Power-supply modules are complete drop-in power supplies by Power Trends (acquired by TI in late 1999). Most are dc-dc converters with various options available in each module family group. They should be used when:

- There are limited design resources.
- The time to market is critical.
- Prototyping is being done.
- The following requirements, which are provided by inductive switchers, are needed:
  - Efficiency is critical: 80 – 95%.
  - The applications has a wide input voltage range.
  - High output currents are required.
  - Board space is not a critical issue.
  - The application is step-up, step-down, or inverting.
  - Noise is not a major concern.

## 6 TI Solutions

### 6.1 Linear Regulators

Tables 4 and 5 summarize linear regulators from TI that support output currents from 50 mA to 5 A. Although there are many possible solutions for the same output current, the subfamilies focus on other parameters that are critical to different applications, such as low noise, low I<sub>q</sub>, high PSRR, and fast transient response.

**Table 4. Linear Regulators**

DEVICE	MAX I <sub>OUT</sub> (mA)	MAX V <sub>IN</sub> (V)	V <sub>O</sub> OPTIONS (V)	COMMENTS
<b>50 mA - 150 mA Max. Supply Current LDO</b>				
TPS760XX	50	16	3, 3.2, 3.3, 3.8, 5.0	SOT-23, with shut down
TPS770XX	50	13.5	1.2, 1.5, 1.8, 2.5, 2.7, 3.0, 3.3, 5.0 †	SOT-23, with shut down, 17 uA Iq
TPS761XX	100	16 V	5, 3.8, 3.3, 3.2, 3.0	SOT-23, with shut down
TPS769XX	100	13.5	1.2, 1.5, 1.8, 2.5, 2.7, 3.0, 3.3, 5.0 †	SOT-23, with shutdown, 17 uA Iq
TPS763XX	150	10 V	5, 3.3, 2.5, 1.8†	SOT-23, with shut down
TPS764XX	150	10 V	3.3, 3.0, 2.7, 2.5	SOT-23, with shut down
TPS765XX	150	10 V	1.2, 1.5, 1.8, 2.5, 2.7, 3.0, 3.3, 5.0 †	SOIC-8, with shut down and PG
<b>+150 mA up to 250 mA LDO</b>				
TPS74XX	200	7	1.5, 1.8, 2.5, 3, 3.3	SO-8, Enable, 1-μF capacitor for stability
UCC386/87/88	200	9	5, 3.3 †	TSSOP
TPS766XX	250	10	1.2, 1.5, 1.8, 2.5, 2.7, 3.0, 3.3, 5.0 †	SOIC-8, PG, with shut down, stable with 4.7 μF capacitor
TPS72XX	250	10	5, 4.8, 3.3, 2.5 †	Adjustable down to 1.2 – 9.75 V
<b>250 mA up to 500 mA LDO</b>				
TPS71XX	500	10	5, 4.8, 3.3, 2.5 †	1.2 – 9.75V †
TPS71HXX	500	10	5, 4.8, 3.3 †	1.2 – 9.75V, HTSSOP Package †
TPS7333	500	10	5, 4.8, 3.3 †	1.2 – 9.75V, w / SVS †
TPS775XX	500	13.5	1.5, 1.8, 2.5, 3.3 †	With SVS, EN
TPS776XX	500	13.5	1.5, 1.8, 2.5, 3.3 †	With PG, EN
<b>750 mA LDO</b>				
TPS777XX	750	13.5	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5 †	With SVS, EN
TPS778XX	750	13.5	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5 †	With PG, EN
<b>Up to 1 amp LDO</b>				
TPS767XX	1000	10	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5 †	Adjustable from 1.5 – 5 V, En, SVS, PowerPad package, any Cap.
TPS768XX	1000	10	5, 3.3, 3, 2.8, 2.7, 2.5, 1.8, 1.5 †	Adjustable from 1.5 – 5 V, En, PG, PowerPad package, any Cap.
UCC381-X	1000	9	3.3, 5 †	1.25 – 8.85 V †
<b>3 – 5 amp LDO</b>				
UCC383-X	3000	9	3.3, 5 †	1.25 – 8.85 V †
UC382-X	3000	7.5	2.5, 5	1.2 – 6 V †
UC385-X	5000	7.5	1.2, 1.5, 2.1, 2.5	

† Adjustable

**Table 5. Dual Output 250-mA to 1-A LDOs**

DEVICE	MAX I <sub>OUT1</sub> /I <sub>OUT2</sub> (mA)	MAX V <sub>IN</sub> (V)	V <sub>O</sub> OPTIONS (V)	COMMENTS
TPS707XX	250/125	6	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2 †	TSSOP-20 PowerPad package, power sequencing control on chip, EN, SVS.
TPS701XX	500/250	6	3.3/2.5, 3.3/1.8, 3.3/1.5, 3.3/1.2 †	TSSOP-20 PowerPad package, power sequencing control on chip, EN, SVS.
TPS73HD3xx	750/250	10	3.3, 2.5, 1.8 †	Dual, with SVS and EN.
TPS767D3XX	1000/1000	10	3.3/Adj., 3.3/2.5, 3.3/1.8	Dual with SVS and EN, SVS, PowerPad package, any capacitor

† Adjustable

## 6.2 Switching Regulators—3 Amps and Higher

TI offers a number of high-current switching regulator solutions. These include current mode, voltage mode, and synchronous hysteretic controllers, as well as a number of PWMs from the TI/Unitrode families. A sample of the various devices is listed in Table 6.

**Table 6. Power-Supply Controllers**

DEVICE	I <sub>OUT</sub> RANGE (A)	V <sub>IN</sub> RANGE (V)	V <sub>O</sub> OPTIONS (V)	COMMENTS
TL5001A	3 – 10	3.6 - 40	3.6 – 40	3.6 V – 40 V, PWM
UCC3585	< 8	1.2 – 6	1.25 – 4.5	Released 2h00
TPS5102	< 12	4.5 – 25	Down to 1.3V	Dual output PWM / skip
TPS5602	3 – 20	4.5 – 25	5.0, 3.3, 2.5, 1.8, 1.5 †	Dual output, hysteretic control ripple
TPS5103	< 12	4.5 – 25	Down to 1.3	PWM, skip, or hysteretic
TPS56XX	3 – 20	12	5.0, 3.3, 2.5, 1.8, 1.5	Hysteretic, single output
TPS56100	3 – 30	5	5.0, 3.3, 2.5, 1.8, 1.5	Hysteretic, single output
TPS56300	Dual, up to 30 A for switcher output.	2.8 – 5.5	1.3 – 3.3	Ideal for power split rail, sequencing on board with programmable slow-start; second output is LDO.

† Adjustable

## 6.3 Power Modules (Power Trends)

The modules listed in Table 7 are Power Trend 5-V and 3.3-V input devices. There are other modules not listed that support input voltages of 12 – 75 V and output voltages up to 18 V.

**Table 7. 5-V Input Switching Power-Supply Modules**

DEVICE	I <sub>OUT</sub> (A)	V <sub>IN</sub> RANGE (V)	V <sub>O</sub> OPTIONS (V)
PT550x	1.5	5 – 3.3	1.2 – 3.3
PT6405	3	5 only	1.2 – 3.3
PT650x/20	8	5 – 3.3	1.2 – 3.6
PT660x	9	5 – 3.3	1.2 – 3.6
PT670x	13	5 – 3.3	1.3 – 3.5
PT770x	18	5 – 3.3	1.3 – 3.5
PT771x	20	5 – 3.3	1.3 – 3.5
PT7777	32	5 – 3.3	1.3 – 5.5

## 7 Summary

Advanced technologies have made available small device geometries that need lower operating voltages and usually also require multiple-voltage power-supply regulation. These requirements are becoming increasingly common for the correct operation of many digital signal processors, field-programmable gate arrays (FPGAs), and general-purpose microprocessors. FPGA solutions can differ radically from design to design, making it difficult to predict current consumption. This application report has focused on the Altera FLEX 10KE series and the APEX 20K/20KE series FPGAs. Using a simple design example, it has attempted to provide the design engineer with a first-cut estimate of the currents these devices draw.

The report has also discussed potential issues such as latch-up and device overstressing associated with multivoltage components. It has presented a variety of TI power-supply solutions, including LDO linear regulators and inductive switching regulators from TI/Unitrode, and inductive switching power-supply modules from TI/Power Trends.

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