TEXAS INSTRUMENTS

Application Report
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Designing With the TPS54311 Through TPS54316 Synchronous Buck Regulators

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ABSTRACT

The SWIFT™ TPS5431x family of internally compensated synchronous buck regulators offers a quick and easy solution to many power supply applications. These devices require a minimum of six additional components. The simple design procedure can be accomplished with the five basic steps outlined in this application note. Devices in this product family include the TPS54311, TPS54312, TPS54313, TPS54314, TPS54315, and TPS54316. These devices can deliver 3 A of continuous output current from an input voltage of 3 V to 6 V. The output voltage of these devices is fixed by the internal circuitry, and is available in 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V options.

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Introduction

The SWIFT™ TPS5431x family of internally compensated synchronous buck regulators makes designing a power solution quick and easy. Table 1 gives a summary of the devices included in this product family. In addition to this application note, the *SWIFT Designer* software tool is a resource that can greatly reduce design time by providing a complete power supply solution with only a few clicks of a mouse. *SWIFT Designer* allows the user to enter the power requirements and then intelligently selects all of the required components. *SWIFT Designer* is available at the Texas Instruments web site. The design methods presented in this application note are similar to the design methods used by the *SWIFT Designer* software.

Table 1. TPS5431x Family Summary

Device	Output Voltage
TPS54311	0.9 V
TPS54312	1.2 V
TPS54313	1.5 V
TPS54314	1.8 V
TPS54315	2.5 V
TPS54316	3.3 V

A complete power supply design can be accomplished by performing the following five steps:

1. Select a switching frequency.
2. Select the input filter components.
3. Select the output filter components.
4. Select the bias and bootstrap capacitors.
5. Select a slow start time.

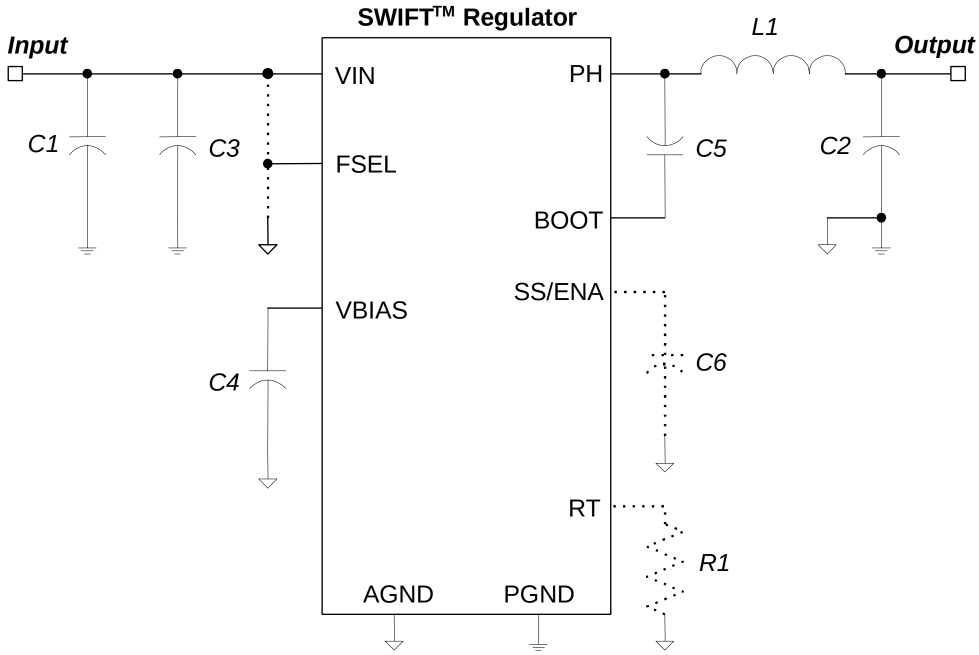

Figure 1. Typical Schematic

Step One: Select a Switching Frequency

The switching frequency can be fixed at 350 kHz or 550 kHz without using any external components. To set the switching frequency to 350 kHz, simply pull the FSEL pin to ground. For a 550 kHz switching frequency, the FSEL pin should be connected to the input voltage. Using the FSEL pin to set the switching frequency results in a frequency accuracy of +/- 20%.

If a more precise switching frequency or a switching frequency other than 350 kHz or 550 kHz is desired, the switching frequency can be programmed by connecting an external resistor (R1 in Figure 1) between the RT pin and ground. The switching frequency can be programmed to any value between 280 kHz and 700 kHz by selecting R1 from the graph in Figure 2. When setting the frequency through this method, the FSEL pin should be left open. Using a 100 kΩ resistor for R1 results in a 500 kHz switching frequency with an accuracy of +/- 8%.

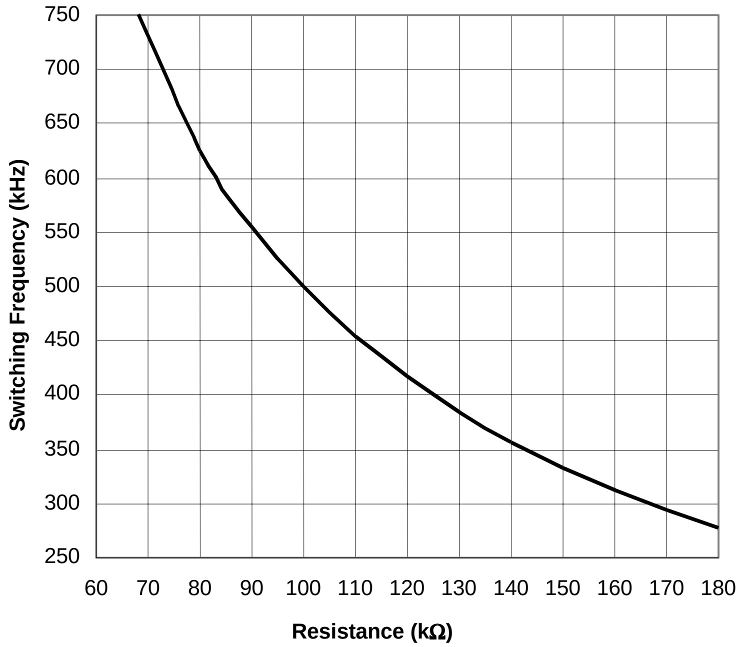

Figure 2. Switching Frequency Trimming Resistor Selection

Step Two: Select the Input Filter Components

The input of the TPS5431x requires a decoupling capacitor and a bulk input capacitor.

Input Decoupling Capacitor

The input decoupling capacitor (C3 in Figure 1) is needed to attenuate high frequency noise on the input of the device. This capacitor should be a ceramic capacitor in the range of 1 µF to 10 µF. A 10-uF, 10-V, 1210, X5R (or X7R) capacitor is recommended. This capacitor needs to be located as close as possible to the IC to be fully effective.

Bulk Input Capacitor

The purpose of the bulk input capacitor (C1 in Figure 1) is to reduce the ripple voltage on the input bus. Depending on the application, a 10-µF ceramic decoupling capacitor may provide enough filtering, and a bulk input capacitor may not be required.

To determine if a bulk capacitor is needed, first determine what the maximum allowable input ripple voltage is for the application. To ensure proper operation of the TPS5431x, the maximum input ripple voltage should not exceed 300 mV_{pp}. Next, calculate the expected worst case input ripple voltage with only the 10-µF ceramic capacitor using Equation 1. If the value calculated by Equation 1 is greater than the maximum allowable input ripple voltage, then a bulk input capacitor is required.

Equation 1

$$\Delta V_{IN} = \frac{0.25 \cdot I_{OUT(MAX)}}{10\mu F \cdot F_{SW}}$$

Where: ΔV_{IN} *is the maximum peak-to-peak input ripple voltage w/o a bulk capacitor.*

$I_{OUT(MAX)}$ *is the maximum dc load current.*

F_{SW} *is the selected switching frequency.*

The bulk input capacitor stores additional energy that keeps the input voltage from drooping too much when the TPS5431x draws a pulse of current during the on time of the topside MOSFET. Larger bulk input capacitors will result in less of a voltage droop. The voltage drop across the equivalent series resistance (ESR) of the bulk capacitor also adds to the input ripple voltage. As a result, the bulk capacitor should be a relatively high valued capacitor with a low ESR. Aluminum electrolytic, tantalum, POSCap, and Oscon capacitors all work well as bulk input capacitors.

Equation 2 can be used to estimate the maximum input ripple voltage for a specific bulk input capacitor. If a particular bulk capacitor results in too high of an input ripple voltage, multiple capacitors can be used in parallel.

Equation 2

$$\Delta V_{IN} = \frac{0.25 \cdot I_{OUT(MAX)}}{C_{BULK} \cdot F_{SW}} + I_{OUT(MAX)} \cdot ESR_{MAX}$$

Where: ΔV_{IN} *is the maximum peak-to-peak input ripple voltage with a bulk capacitor.*

$I_{OUT(MAX)}$ *is the maximum dc load current.*

F_{SW} *is the selected switching frequency.*

C_{BULK} *is the selected bulk capacitance.*

ESR_{MAX} *is the maximum ESR of the selected bulk capacitor.*

The voltage and current ratings of the bulk capacitor must also be checked. The maximum voltage across the bulk capacitor can be estimated using Equation 3. The maximum RMS current in the bulk input capacitor can be estimated using Equation 4. Ensure that the voltage and RMS current rating of the selected bulk input capacitor are not exceeded.

Equation 3

$$V_{CIN(MAX)} = V_{IN(MAX)} + \frac{\Delta V_{IN}}{2}$$

Where: $V_{CIN(MAX)}$ *is the maximum voltage across the bulk capacitor.*

$V_{IN(MAX)}$ *is the maximum input voltage.*

ΔV_{IN} *is the peak-to-peak input ripple voltage calculated by Equation 2.*

Equation 4

$$I_{CIN,RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$$

Where: $I_{CIN,RMS(MAX)}$ *is the maximum RMS current in the bulk capacitor.*

$I_{OUT(MAX)}$ *is the maximum dc load current.*

Step Three: Select the Output Filter Components

Selecting the output filter is perhaps the most critical part of designing with a TPS5431x regulator. Because the feedback compensation is fixed, the output filter components determine the stability of the regulator. Two components must be selected for the output filter : an output inductor (L1 in Figure 1) and an output capacitor (C2 in Figure 1). One of the key parameters that determines the power supply stability is the equivalent series resistance (ESR) of the output capacitor. The maximum ESR for most capacitors is provided in the manufacturer's data sheets. The minimum ESR is not typically expressed in the data sheets. However, as a general rule, the minimum ESR can be assumed to be 40% to 60% of the maximum ESR. The variation of ESR with temperature should also be considered when selecting an output capacitor.

Inductor Selection

When selecting an inductor, the RMS current and saturation current ratings must be checked. The maximum RMS current in the inductor can be calculated using Equation 5. The maximum instantaneous current in the inductor can be calculated using Equation 6. Select an inductor with an RMS current rating greater than the value calculated by Equation 5, and a saturation current rating greater than the value calculated by Equation 6.

Equation 5

$$I_{L(RMS,MAX)} = \sqrt{I_{OUT(MAX)}{}^{2} + \frac{1}{12}\cdot\left(\frac{\left(V_{IN(MAX)} - V_{OUT}\right)\cdot V_{OUT}}{V_{IN(MAX)}\cdot L_{OUT}\cdot F_{SW}\cdot 0.8}\right)^{2}}$$

Where: $I_{L(RMS,MAX)}$ *is the maximum RMS output inductor current.*

$I_{OUT(MAX)}$ *is the maximum dc load current.*

$V_{IN(MAX)}$ *is the maximum input voltage.*

V_{OUT} *is the output voltage.*

L_{OUT} *is the selected output inductance.*

F_{SW} *is the selected switching frequency.*

Equation 6

$$I_{L(PEAK,MAX)} = I_{OUT(MAX)} + \frac{1}{2}\cdot\frac{\left(V_{IN(MAX)} - V_{OUT}\right)\cdot V_{OUT}}{V_{IN(MAX)}\cdot L_{OUT}\cdot F_{SW}\cdot 0.8}$$

Where: $I_{L(PEAK,MAX)}$ *is the maximum instantaneous output inductor current.*

$I_{OUT(MAX)}$ *is the maximum dc load current.*

$V_{IN(MAX)}$ *is the maximum input voltage.*

V_{OUT} *is the output voltage.*

L_{OUT} *is the selected output inductance.*

F_{SW} *is the selected switching frequency.*

Capacitor Selection

When selecting an output capacitor, four factors must be considered : the capacitor's DC voltage rating, the capacitor's ripple current rating, the maximum output ripple voltage, and the stability of the power supply.

Verifying the output capacitor dc voltage rating is simple. Simply ensure that the DC voltage rating is greater than the output voltage. It is a good idea to pick an output capacitor rated at least ten percent greater than the output voltage of the regulator to account for ripple and transients.

The maximum output capacitor ripple current can be calculated using Equation 7. Select an output capacitor with a ripple current rating greater than the value returned from Equation 7.

Equation 7

$$I_{C(RMS,MAX)} = \frac{1}{\sqrt{12}} \cdot \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN(MAX)} \cdot L \cdot F_{SW}}$$

Where: $I_{C(RMS,MAX)}$ *is the maximum RMS output capacitor current.*

$V_{IN(MAX)}$ *is the maximum input voltage.*

V_{OUT} *is the output voltage.*

L_{OUT} *is the selected output inductance.*

F_{SW} *is the selected switching frequency.*

Regarding the output ripple voltage, first determine the maximum ripple voltage requirements of the application that will be using the output voltage of the TPS5431x regulator. To ensure proper operation of the TPS5431x, the maximum output ripple voltage should be limited to less than 30 mV_{pp}. Next, calculate the maximum allowable ESR using Equation 8. The selected capacitor should have a maximum ESR rating less than the value calculated by Equation 8 in order to ensure that the output ripple voltage does not exceed the application requirements. ESR variation with temperature should also be considered.

Equation 8

$$ESR_{MAX,RIPPLE} = \frac{\Delta V_{PK-PK(MAX)} \cdot V_{IN(MAX)} \cdot L_{OUT} \cdot F_{SW} \cdot 0.8}{\left(V_{IN(MAX)} - V_{OUT}\right) \cdot V_{OUT}}$$

Where: $ESR_{MAX,RIPPLE}$ *is the maximum allowable output capacitor ESR.*

$\Delta V_{PK\_PK(MAX)}$ *is the maximum peak to peak output ripple voltage.*

$V_{IN(MAX)}$ *is the maximum input voltage.*

V_{OUT} *is the output voltage.*

L_{OUT} *is the selected output inductance.*

F_{SW} *is the selected switching frequency.*

Once the dc voltage rating, current rating, and maximum ESR due to the ripple voltage have been determined, use the capacitor selection graphs in Figure 3 through Figure 7 to select a capacitor that results in a stable power supply. The shade regions of the capacitor selection graphs show the stable region of ESR and capacitance for typical inductor values.

To summarize, when selecting an output capacitor the following items must be checked:

1. Verify that the dc voltage rating is greater than the output voltage.
2. Verify that the ripple current rating is greater than the value calculated by Equation 7.
3. Verify that the maximum ESR is less than the value calculated by Equation 8.
4. Verify that the capacitance and minimum and maximum ESR fall in the stable region of the capacitor selection graphs.

If no capacitor can be found that meets these requirements, try increasing the inductance, increasing the switching frequency, or using multiple output capacitors in parallel. If there are still not any capacitors that meet the preceding requirements, a solution can be achieved with an externally compensated SWIFT™ device (TPS54310).

Multiple Output Capacitors

Some applications may require more than one output capacitor. One possible reason for using multiple output capacitors is a stringent load transient requirement. For applications that provide power to high slew rate loads, adding additional capacitance to the output limits voltage fluctuations on the output. To create a design with multiple output capacitors using the method presented above, treat the parallel combination of capacitors as a single capacitor. The equivalent capacitance is equal to the sum of the parallel capacitors, and (provided that all the paralleled capacitors are the same) the ESR is the parallel combination of the ESRs.

Description of Capacitor Selection Graphs

The capacitor selection graphs shown in Figure 3 through Figure 7 show the stable region of ESR and capacitance in the shaded areas. The lower bounds of the selection graphs are dictated by a 45° phase margin requirement. Using a capacitor with an ESR value below the stable region of the graphs will result in less than 45° of phase margin.

There are two upper bounds shown in Figure 3 through Figure 7. These upper bounds are dictated by the maximum unity gain crossover frequency requirement. The upper bound for switching frequencies greater than 500 kHz limits the crossover frequency to 100 kHz, while the upper bound for switching frequencies less than 500 kHz limits the crossover frequency to 50 kHz. Both upper bounds are higher at lower input voltages.

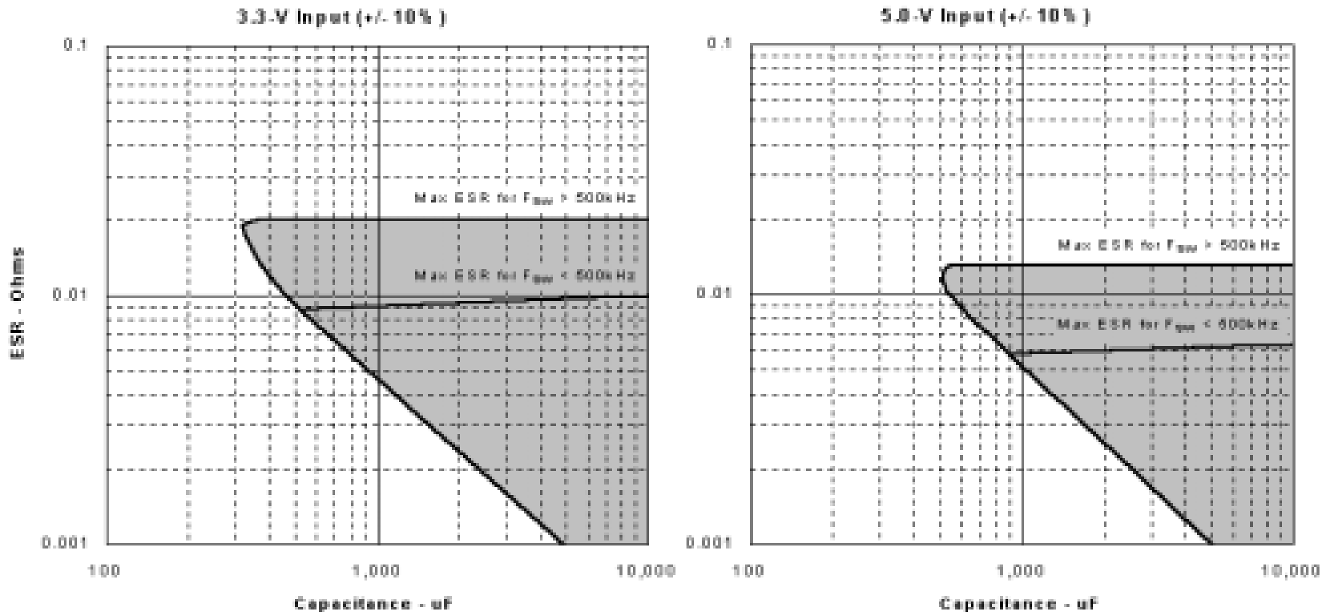

Figure 3. Regions of Stability for 2.2-µH Inductor

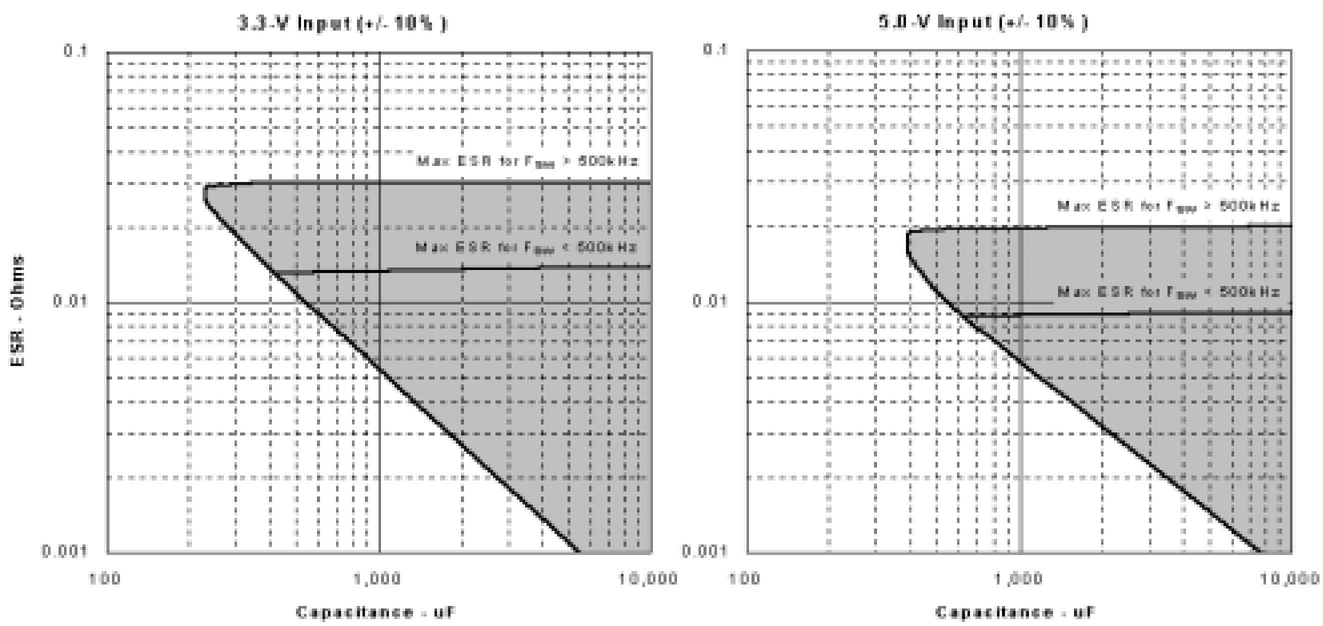

Figure 4. Regions of Stability for 3.3-µH Inductor

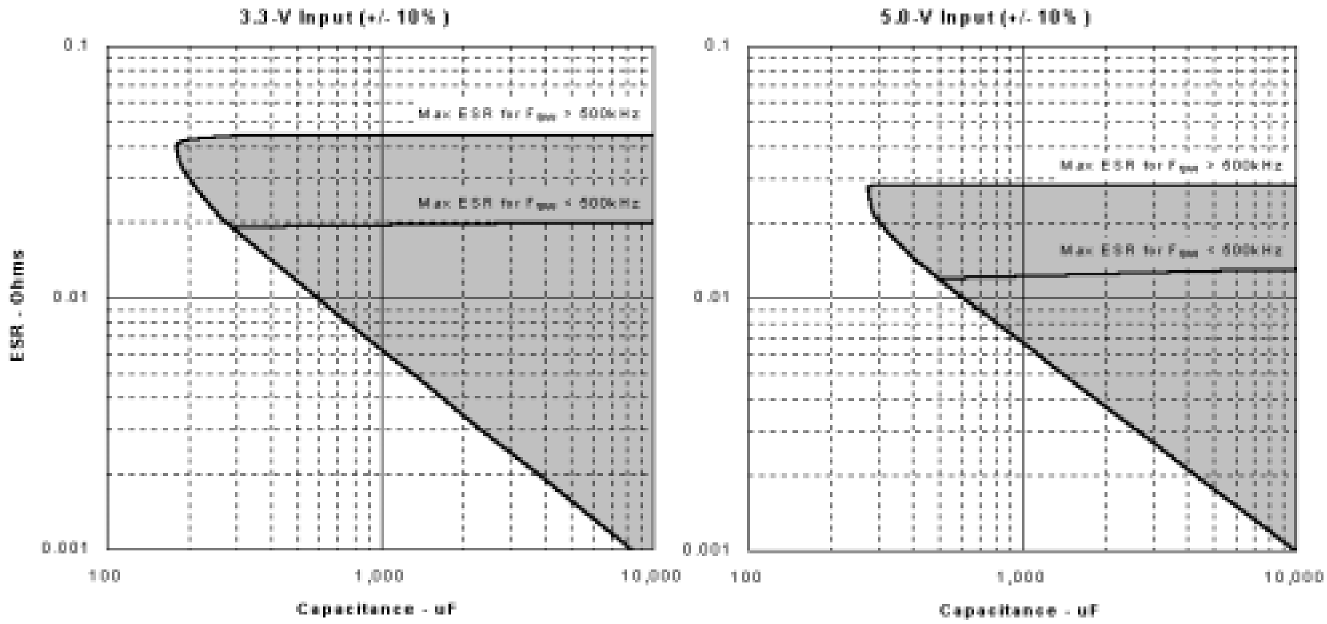

Figure 5. Regions of Stability for 4.7-μH Inductor

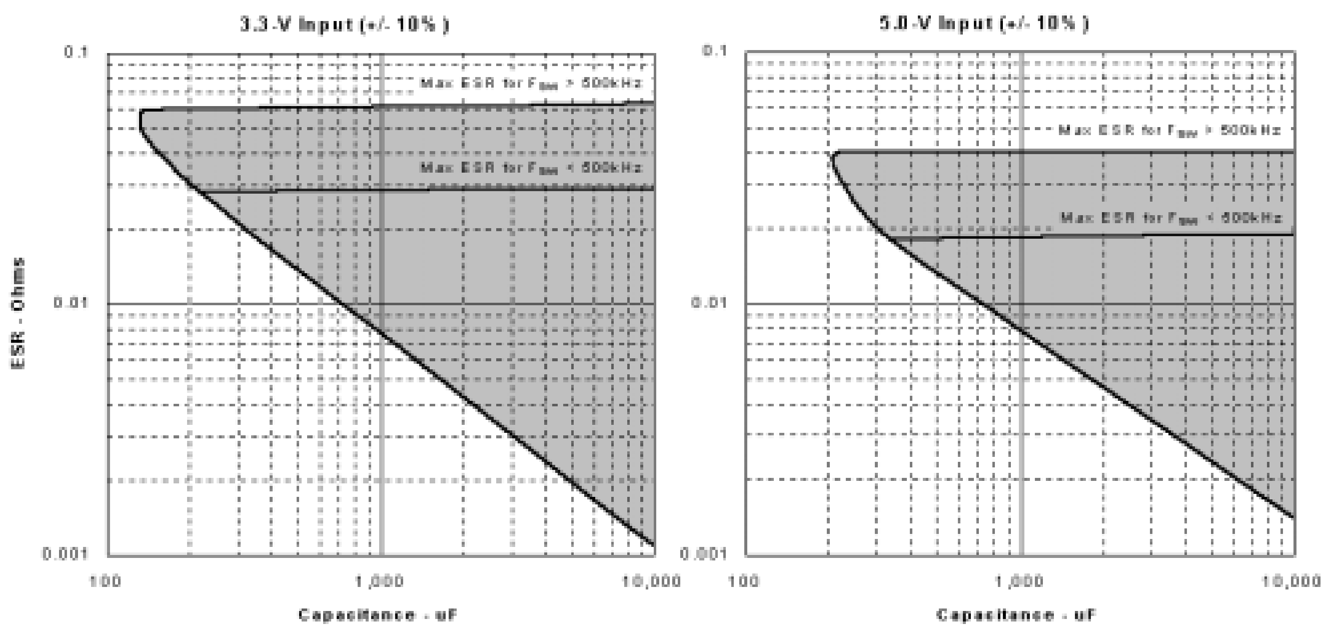

Figure 6. Regions of Stability for 6.8-μH Inductor

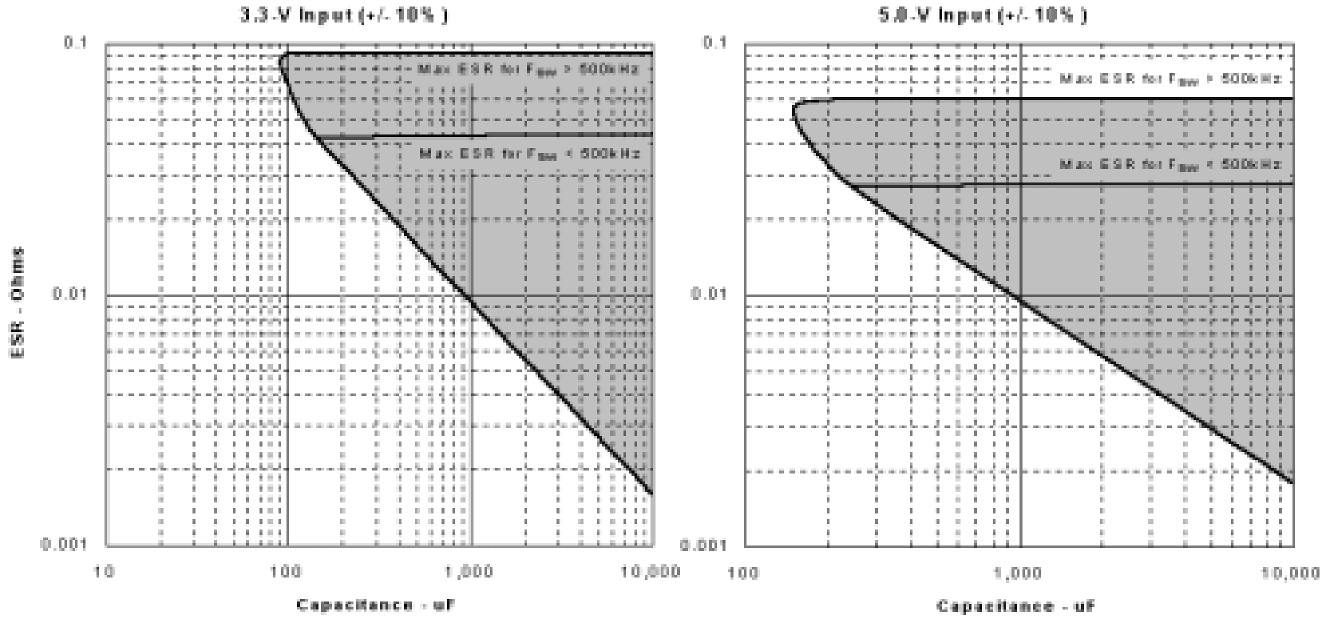

Figure 7. Regions of Stability for 10-μH Inductor

Step Four : Select the Bias and Bootstrap Capacitors

Every TPS5431x application requires a bias capacitor (C3 and C4 in Figure 1) and a bootstrap capacitor (C5 in Figure 1). The bias capacitor should be a ceramic 0.1 μF, and should be placed between the VBIAS pin and analog ground. The bias capacitor should be physically located as close to the IC as possible. The bootstrap capacitor should be ceramic and in the range of 0.022 μF to 0.1 μF. The bootstrap capacitor should be connected between the BOOT pin and the PH pin.

Step Five : Select a Slow Start Time

The TPS5431x contains an internal slow start circuit that controls the rise time of the output voltage during startup. The internal slow start time is different for the different devices in the TPS5431x family, and is given by Table 2. Alternatively, the output voltage rise time can be extended beyond the internal slow start time by connecting a capacitor (C6 in Figure 1) between the SS/ENA pin and analog ground. The equation for selecting a slow start capacitor is given by Equation 9. Using either method, the slow start time is independent of input voltage and load current.

The slow start cycle begins once the input to the TPS5431x rises above the 3-V startup threshold, or the enable pin is released from ground. With an internally controlled slow start, the output voltage then begins to rise in a linear fashion until it reaches the final output voltage level. If an external slow start capacitor is used, there is an inherent time delay from the start of the slow start cycle to the time where the output voltage begins to rise. This time delay is dependent on the size of the slow start capacitor, and can be calculated by Equation 10.

Equation 9

$$C_{(SS)} = t_{(SS)} \cdot K$$

Where: $C_{(SS)}$ *is the slow start capacitance in Farads.*
$t_{(SS)}$ *is the desired slow start time in seconds.*
K *is a device dependent coefficient given by Table 3.*

Equation 10

$$t_d = \frac{C_{(SS)} \cdot 1.2V}{5\mu A}$$

Where: t_d *is the slow start delay time in seconds.*
$C_{(SS)}$ *is the slow start capacitance in Farads.*

Table 2. Internally Fixed Slow Start Times

Device	Output Voltage	Slow Start Time
TPS54311	0.9 V	3.3 ms
TPS54312	1.2 V	4.5 ms
TPS54313	1.5 V	5.6 ms
TPS54314	1.8 V	3.3 ms
TPS54315	2.5 V	4.7 ms
TPS54316	3.3 V	6.1 ms

Table 3. Externally Programmed Slow Start Coefficients

Device	Output Voltage (V)	Slow Start Coefficient (F/sec)
TPS54311	0.9	5.5×10^{-6}
TPS54312	1.2	4.2×10^{-6}
TPS54313	1.5	3.3×10^{-6}
TPS54314	1.8	5.5×10^{-6}
TPS54315	2.5	4.0×10^{-6}
TPS54316	3.3	3.0×10^{-6}

Layout Considerations

All the components of a TPS5431x design should be kept as close together as possible. In particular, the decoupling and bootstrap capacitors should be located next to the pins of the IC.

The TPS5431x has two internal grounds (analog and power). Inside the TPS5431x, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD™ is tied internally to the analog ground. Noise injected between the two grounds can degrade the performance of the TPS5431x, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground planes are recommended. These two planes should tie together directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54310. The layout of the TPS54314 evaluation module is representative of a recommended layout for a 2 layer board. Documentation for the TPS54314 evaluation module can be found on the Texas Instruments web site under the TPS54314 product folder.

Alternative ground structures are also possible, as long as care is taken to minimize the ground noise. One alternative is to tie the analog and power ground together at the point of regulation (usually the output capacitor). The advantage of this ground structure is that converter's load regulation is slightly improved. Using this method, a wide power ground should be used to limit the noise injected between the analog and power grounds. A primary source of this noise is the circulating current from the input capacitor. When laying out a board in this manner, try to place the input capacitor such that its ground current does not flow between the two ground connections.

Yet another grounding technique is to use one common ground plane for both analog and power grounds. This ground structure simplifies the layout process, but still requires caution. The power and analog ground connections to the IC must still be made as close as possible to the IC. In addition, any ground plane obstructions should not force the noisy power ground currents to flow by any of the sensitive control signal ground connections.

The PowerPAD device package helps the TPS5431x keep junction temperatures from becoming excessive, particularly at high load currents. To ensure that the regulator has good heat sinking capabilities, the PowerPAD layout guidelines provided by the data sheet should be followed.

PowerPAD is a trademark of Texas Instruments

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