Application Report

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ESR, Stability, and the LDO Regulator

Jeff Falin, John Cummings

Linear Power

ABSTRACT

Choosing an output capacitor for LDO $_{\text{regulators}}$ with PNP or PMOS pass element can be difficult due to specific ESR requirements. This application report explains how ESR impacts stability and how to determine whether or not the regulator is stable.

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Trademarks

1 Introduction

As the typical PMOS or PNP open loop gain plot of Figure 1 shows, there are three important poles in a PMOS or PNP pass element based LDO regulator. The dominant pole, P(DOM), is set in the error amplifier of the regulator. The load pole, P(LOAD), is formed by the output capacitor and load and therefore varies with load current. The pass device pole, P(PASS), is formed by the parasitic capacitance of the pass element. In order for any negative feedback system to be stable, the open loop gain of the system must be below 0 dB when the phase is 360° (180° of the fed-back signal plus the 180° from the inverting input of the error amplifier). Stated another way, the system must have sufficient phase margin, that is,, the amount of phase shift remaining until 360° degree when the gain is at 0 dB. Since each pole contributes 90° of phase shift and 20 dB/decade (or –1) roll off in gain, a three-pole, high gain system requires compensation in order to be stable. A regulator is unconditionally stable (that is, has sufficient phase margin) if the open loop gain curve rolls off at 20 dB/decade (that is, like a single pole system) before crosses 0 dB. The most common method of compensation is to insert a zero in the system to cancel the phase shift and roll off of one of the poles. Since an LDO already requires an output capacitor for normal operation, using the ESR of the output capacitor is typically the simplest and least expensive method for generating this zero, see $f_{Z(ESR)}$ in Figure 1.

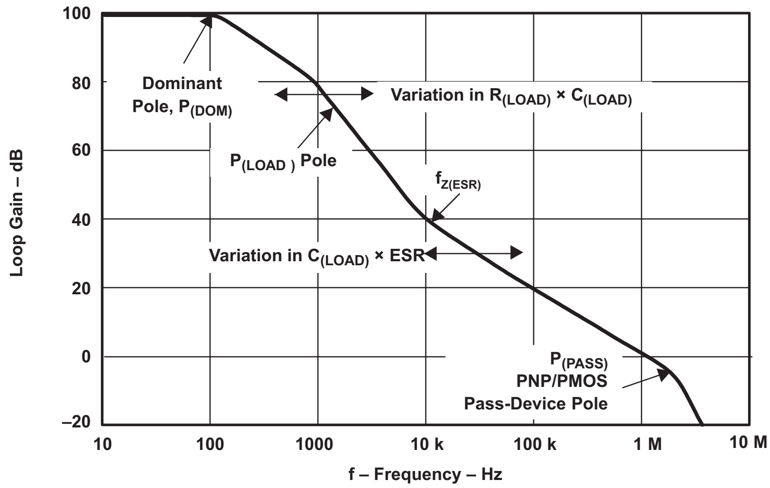

Figure 1. Open Loop Response of Typical PMOS or PNP LDO Regulator

The challenge is choosing a capacitor with the correct amount of ESR. The ESR must be high enough to lower the $f_{Z(ESR)}$ frequency so that the gain slope is –20 dB/decade instead of –40 dB/decade (–2) when it crosses 0 dB, but low enough so that the $f_{Z(ESR)}$ frequency is high enough for the gain to be below 0 dB before $P_{(PASS)}$.

In TI's older regulator data sheets that were designed when tantalum or high-ESR capacitors were more common, a minimum capacitor value is specified and an ESR vs output current for that output capacitor (and usually another capacitor) is provided. Figure 2 shows a typical curve for the TPS76050 device.

NOTE: The ESR used in these plots is the minimum ESR of the capacitor as ESR does vary over frequency.

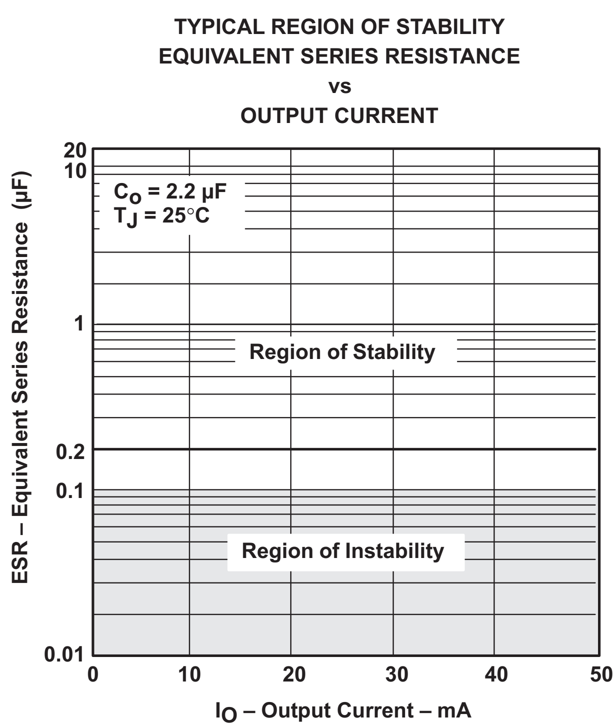

Figure 2. Typical ESR vs Output Current

The curve of this device requires that, for the minimum 2.2-µF of output capacitance, the ESR must be between 0.1 Ω and 20 Ω. Few capacitors have more than 2 Ω of ESR, so the upper limit on the ESR can usually be ignored. The lower limit actually sets the maximum value for the $f_{Z(ESR)}$. For the case of 2.2-µF capacitor referenced in Figure 2, use Equation 1 to calculate the maximum value:

$$f_{Z(ESR)} = 1 / (2 \times \pi \times R_{ESR} \times C_{OUT}) = 72.3 \text{ kHz}$$

where

- R_{ESR} is 0.1 Ω
- C_{OUT} is 2.2 µF (1)

For an older LDO which depended on higer ESR for stability like the TPS760 device, a capacitance and ESR product larger than 0.1 Ω × 2.2 × 10^{-6}F = 2.2 × 10^{-7} ΩF (but less than 20 × 2.2 × 10^{-6} ΩF = 4.4 × 10^{-5} ΩF) is stable, as long as the capacitance is above the minimum required capacitance value.

The TPS760 was designed when tantalum capacitors were common and 1.1 mA was considered low I_Q. For newer LDOs like the TPS7A25 device which have been designed to be optimized with low ESR or ceramic capacitors, there is no need to be concerned about ESR unless you wish to use very large capacitors for hold up.

Performing a load transient test and observing the amount of ringing on the output is the best way to determine if the capacitor selected is stable. Figure 3 shows a test setup for a load transient test using a MOSFET switch and function generator. This setup is preferable to most electronic loads because the simulated transient is much faster.

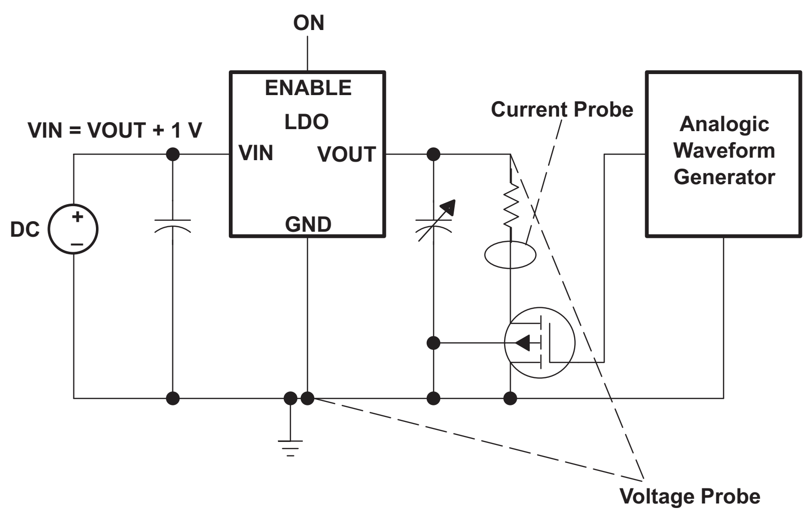

Figure 3. Load Transient Setup

Figure 4 shows the measured results using a TPS76050 device with a 2.2-μF ceramic (low ESR) capacitor. Figure 5 shows the measured results of a TPS76050 device with a 2.2-μF and a 1-Ω series resistor. The results in Figure 4 show multiple oscillations or rings after the initial spike, indicating instability, while the results in Figure 5 shows a stable load transient. Typically, four rings or less indicate sufficient phase margin for the device to be stable.

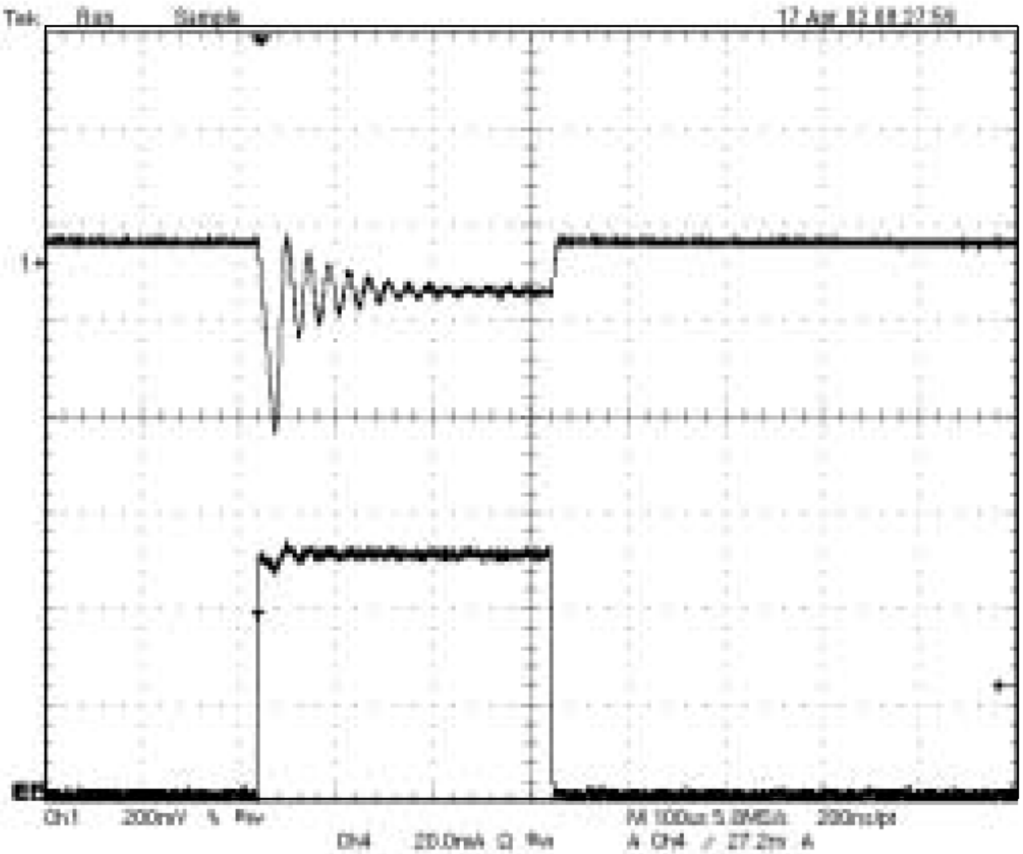

Figure 4. TPS76050 Load Transient With 2.2-μF Ceramic Capacitor

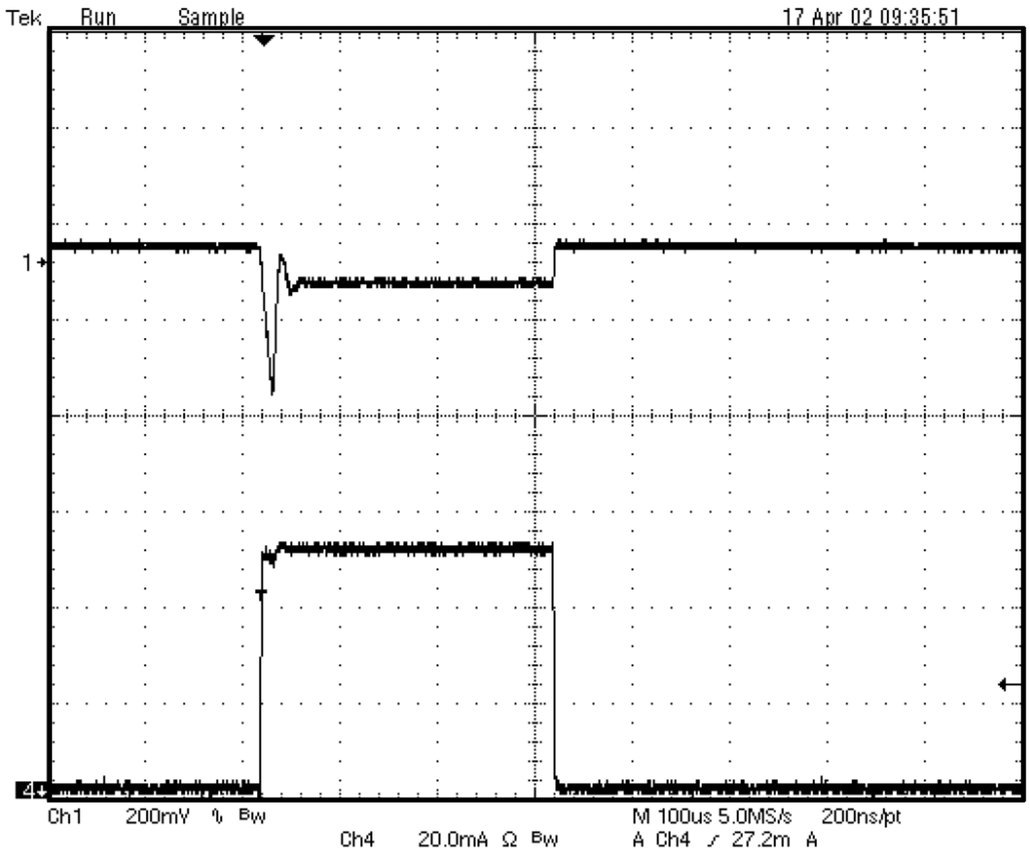

Figure 5. TPS76050 Load Transient With 2.2-µF Ceramic Capacitor and 1-Ω ESR

Comparing to the TPS7A25 device which is stable with a minimum of 1.0-µF ceramic capacitor with no additional ESR, there are no oscillations at the output as Figure 6 shows.

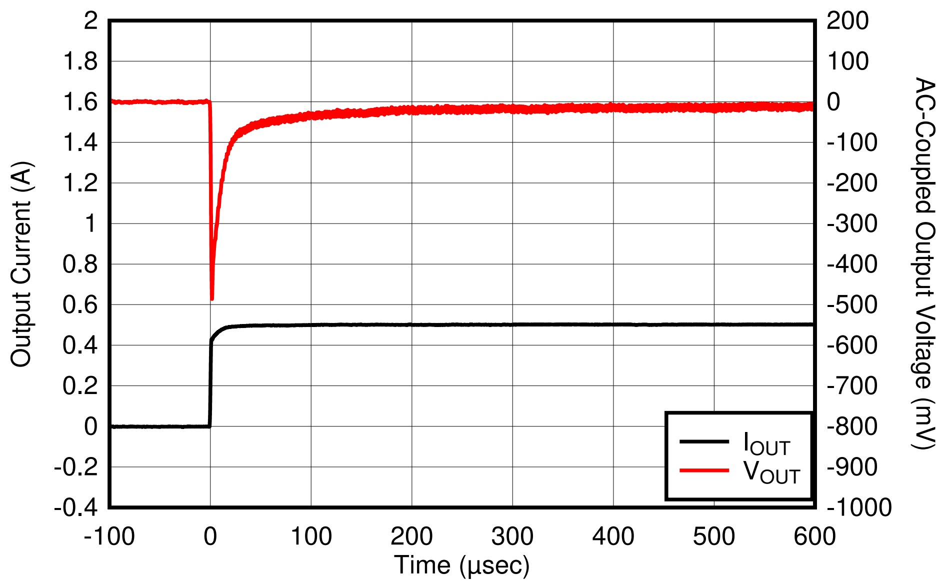

Figure 6. Load Transient (0.5 A) With 1-µF Output Capacitor

Figure 7 shows that the TPS7A26 device is even stable with a capacitor as large as 100 µF.

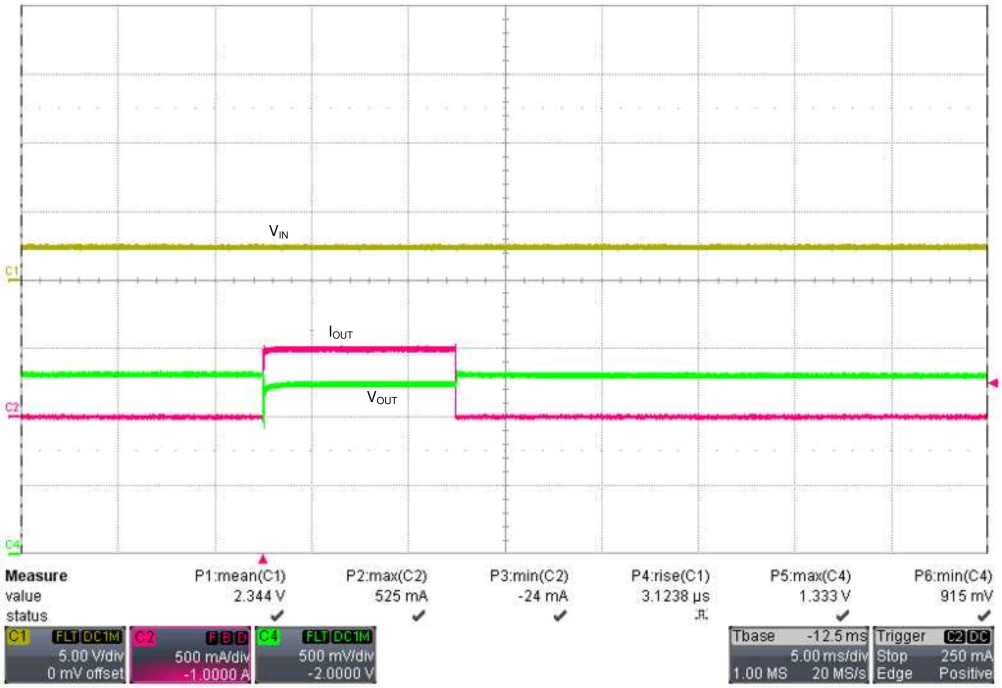

Figure 7. TPS7A26 Load Transient Response With a 100-µF Capacitor at the Output

2 Conclusion

When designing with older linear regulators, ESR is very important to consider when selecting the output capacitor. As the ESR is a function of frequency, the minimum ESR is used in simulations. Newer LDOs like the TPS7A26 device are inherently ceramic capacitor stable which helps to improve cost, size, and performance in the application.

Post ESR and stability questions to TI's *E2E Community*.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2002) to A Revision **Page**

- Deleted TPS7A25 capability and removed the *Example Output Capacitance vs ESR* and *General Shape of an Impedance Curve for a Capacitor* images. 3
- Added Load Transient (0.5 A) With 1-µF Output Capacitor image. 5
- Added *TPS7A26 Load Transient Response With a 100-µF Capacitor at the Output* image. 6
- Added the *Conclusion*. 6