A FET OR-ing Circuit For Fault-Tolerant Power Systems

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ABSTRACT

Fault-tolerant power systems commonly achieve redundancy by diode OR-ing the outputs of several power supply modules. The OR-ing circuit is inefficient if the diode forward voltage drop represents a significant percentage of the load voltage. In low-voltage applications, a FET OR-ing circuit can be more efficient. This application note discusses the design and performance of a FET OR-ing circuit using Texas Instruments TPS2331 IC as a controller.

Introduction

Mission critical systems often require a fault tolerant power system. This requirement can be met by paralleling two or more power supply modules for (N+1) redundancy. The module outputs are diode OR-ed so that a failure in one module does not diminish the system's ability to supply full power to the host. Diode isolation is an effective, low cost, and simple way to obtain redundancy, but it is inefficient for low voltage applications. Replacing each isolation diode with a FET that has a lower voltage drop dramatically improves the OR-ing circuit efficiency. Unlike a diode, a FET can conduct current in both directions and must be turned off by a controller. Devices like Texas Instruments TPS2331 hot-swap IC can control the FETs in the OR-ing circuit.

Using the TPS2331

The TPS2331 limits the load inrush current and protects the system from a load fault in its traditional role as a hot-swap controller. In an OR-ing circuit however, the TPS2331 must protect the system against a *power supply module fault*. The former role requires the TPS2331 circuit breaker to trip if excessive current flows into the load (i.e., $I_{SINK} < 0$) whereas the latter role requires the circuit breaker to trip if excessive current flow into the power supply (i.e., $I_{SINK} > 0$).

Figure 1 shows a TPS2331 hot-swap circuit. The TPS2331 circuit breaker trips when the ISET pin voltage is greater than the ISENSE pin voltage. The 50μA ISET pin sink-current and resistor R_{ISET} determine the circuit-breaker trip point as shown in (1).

$$I_{TRIP} = \frac{R_{ISET}}{R_{SENSE}} \times 50\mu A \quad (1)$$

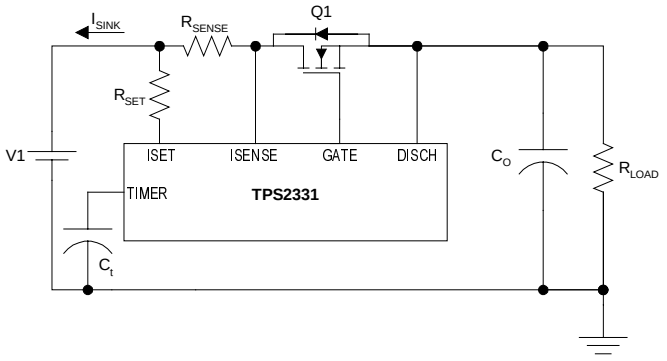


Figure 1. Simplified Diagram of a Hot-Swap Circuit

The circuit in Figure 2 swaps the TPS2331 current sense connections so the circuit breaker trips if excessive current flows *into the power supply*. The TPS2331 measures the power-supply module output current to detect a fault. A power supply module that fails open circuit (e.g., blown input fuse) puts out no current. This failure does not jeopardize power to the host, so there is no need to turn off the FET. On the other hand, a power supply module that fails short circuit (e.g., a bad output rectifier, a bad output filter capacitor, or an over-voltage crowbar that trips) can jeopardize power to the host. The TPS2331 can detect the excessive reverse current and quickly turn off the FET to isolate the fault from the system.

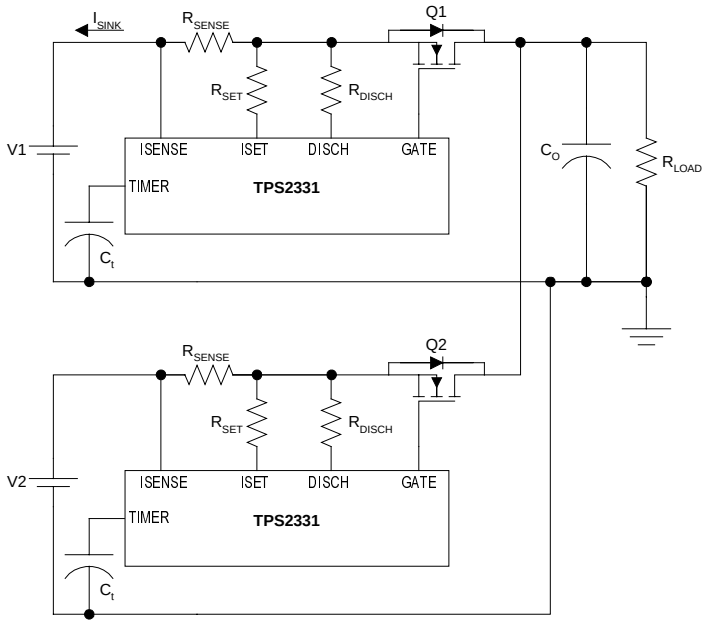


Figure 2. An OR-ing Circuit for Two Power Supply Modules

The circuit in Figure 2 reverses the FET drain and source connections to prevent a bad power supply module from sinking current through the body diode when the FET is off. The DISCH pin (pin 14) pulls low if the TPS2331 circuit breaker trips. Resistor R_{DISCH} limits the DISCH pin current should the power supply output recover.

Output Hold-up Capacitance

The minimum common-mode input voltage of the TPS2331 current-sense comparator is 0.8 V—a lesser voltage can trip the TPS2331 circuit breaker. Short circuiting power supply V1 can bring power supply V2 below this minimum common-mode voltage, and trip the TPS2331 circuit breaker for *both* power supplies. This situation is clearly undesirable and can be avoided by sizing capacitor C_o to hold the load above 0.8V until the circuit breaker for power supply V1 trips.

An equation for capacitor C_o is derived using the worse case circuit model in Figure 3, *where the load current I_o is the maximum that an (N+1) redundant power system can source with a single power supply module failure.*

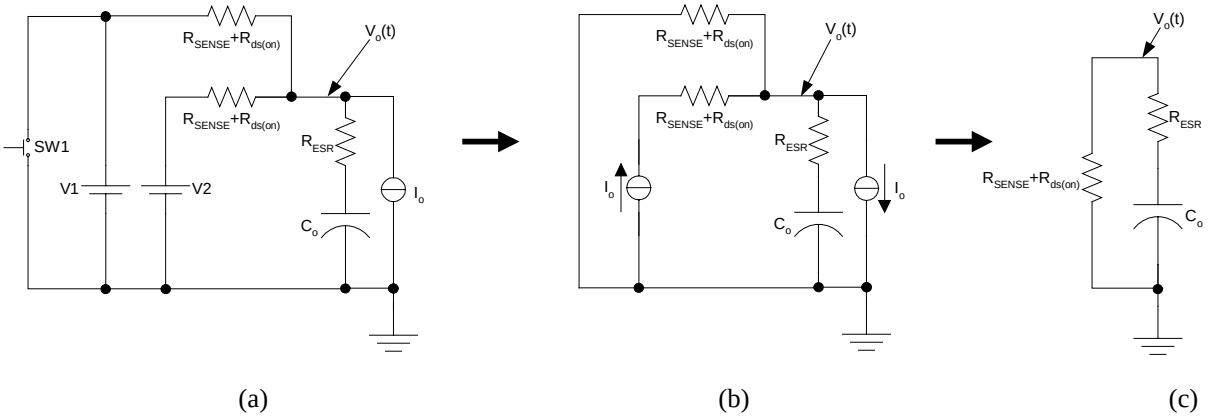


Figure 3. OR-ing Circuit Electrical Model

(a) SW1 is open (b) SW1 is closed (c) SW1 is closed - simplified model

The load voltage decays according to (2) if power supply V1 fails as a short circuit.

$$V_o(t) = \frac{1}{1+\left(\frac{R_{ESR}}{R_{ds(on)}+R_{SENSE}}\right)} \times V_i \times e^{-\left(\frac{t}{\left(R_{ds(on)}+R_{SENSE}+R_{ESR}\right)\bullet C_o}\right)} \quad (2)$$

R_{ESR} is the equivalent series resistance of capacitor C_o, and V_i is the load voltage just before power supply V1 fails. The load voltage $V_o(\tau)$ equals 0.8 V if τ is the circuit breaker response time. Applying this constraint to (2) yields:

$$C_o \geq \frac{-\tau}{\left(R_{ds(on)}+R_{SENSE}+R_{ESR}\right)\times \ln\left(\frac{0.8}{V_i}\times\left[1+\frac{R_{ESR}}{R_{ds(on)}+R_{SENSE}}\right]\right)} \quad (3)$$

Extending the above analysis, we can show that (3) is valid for two or more paralleled power supply modules.

A Design Example

To design a FET OR-ing circuit that meets the following specification:

Power supply modules:	2
Current limit (per module):	7A
Load voltage:	3.3V
Input-to-output voltage drop:	< 150mV
Load current:	5A
Circuit breaker response time:	as fast as possible

Selecting the Fault-timing Capacitor (C_t)

The fault-timing capacitor, C_t, equals 50 pF. This capacitor prevents false triggering of the circuit breaker as explained in the data sheet. Larger capacitances should be avoided as they delay activation of the TPS2331 circuit breaker, increasing the duration of the voltage glitch at the host if a power supply module fails. The data sheet specifies a circuit breaker propagation delay of 1.3 μs (typ) for a 50 pF fault-timing capacitance.

Selecting R_{DISCH}

A reasonable resistance for R_{DISCH} is 1 kΩ to 5 kΩ. The DISCH pin must be connected as shown in Figure 2 to ensure that the gate protection circuitry inside the TPS2331 remains functional.

Selecting R_{ISET}

Resistor R_{ISET} should satisfy (4) for good noise immunity

$$(R_{ISET} \times 50\mu A) \geq 20mV \quad (4)$$

Choose resistor R_{ISET} equal to 402 Ω for maximum sensitivity to reverse current detection.

Selecting R_{SENSE} and Q1

The resistance of R_{SENSE} should be as large as possible for the lowest reverse current detection threshold, and as small as possible for the lowest input-to-output voltage drop. These opposing requirements should be balanced to meet the design specification.

The input-to-output voltage drop specification is 150mV(max) for a 5A load, so:

$(R_{ds(on)} + R_{SENSE}) \times 5A \leq 150mV$, or

$\left(R_{ds(on)} + R_{SENSE}\right) \leq 30m\Omega$

If the resistance is equally distributed between the FET and current-sense resistor, then:

$R_{ds(on)} \leq 15m\Omega$ and $R_{SENSE} \leq 15m\Omega$

The exact trip threshold is not critical since the goal is to shut off the FET *as soon as significant reverse current is detected*. A 12 mΩ resistor for R_{SENSE} meets the above design constraint and sets a trip current of:

$$I_{TRIP} = \left(\frac{402\Omega}{12m\Omega} \times 50\mu A \right) = 1.68A$$

An IRF7413 MOSFET has an on resistance of 11 mΩ (max) so this device is suitable for transistor Q1.

Selecting the Output Hold-up Capacitor (C_o)

Figure 4 plots (3) for V_i = 3.3 V and τ = 2 µsec. Capacitor C_o should have a low series resistance (ESR). OS-CON capacitors from Sanyo and FC-series capacitors from Panasonic are suitable for capacitor C_o.

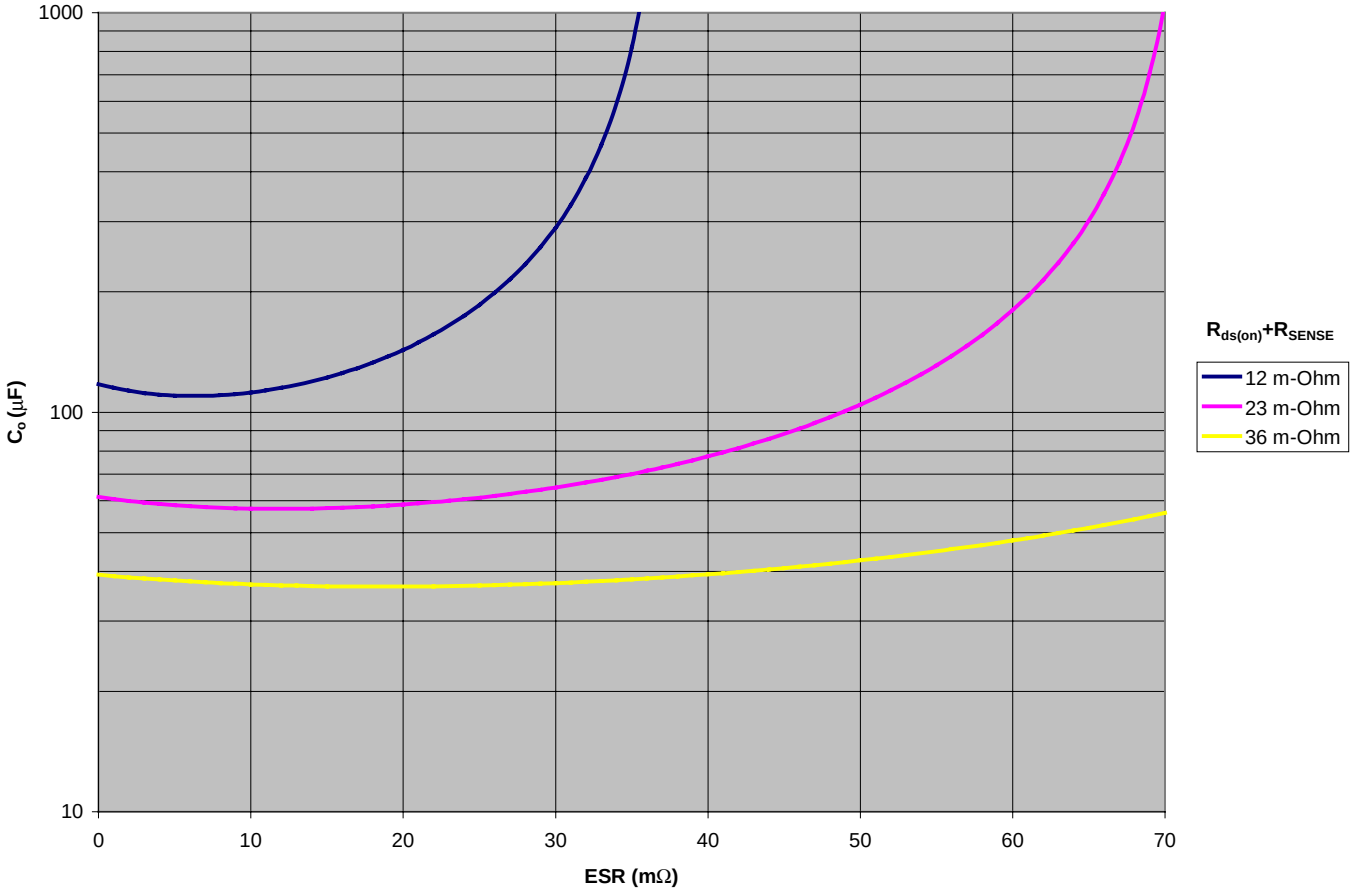


Figure 4. Minimum Hold-Up Capacitance for V_i = 3.3Vand τ = 2µsec

A Sanyo 20SP120 (120 µF, 24 mΩ ESR) capacitor, or a Panasonic EEUFC1H471L (470 µF, 60 mΩ ESR) capacitor works in this design example.

Test Results

The schematic in Appendix A shows a FET OR-ing circuit that meets the design specification. The setup in Figure 5 is used to evaluate this circuit.

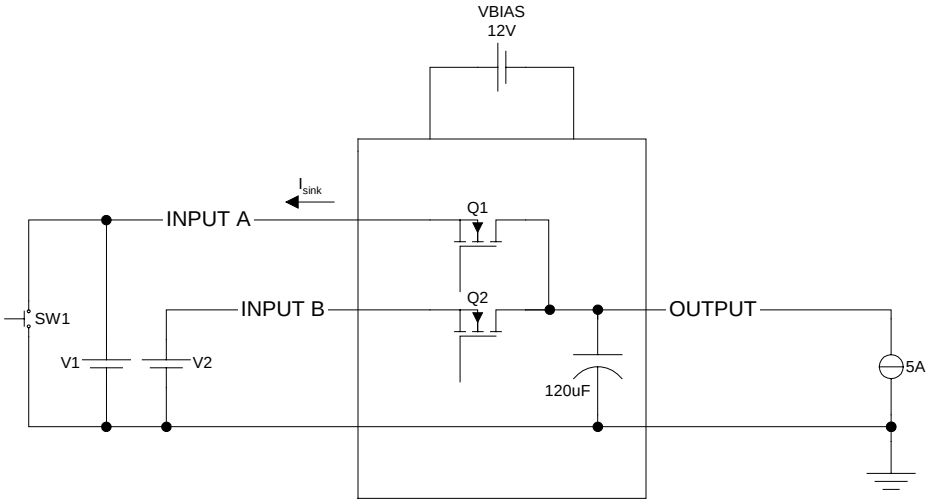


Figure 5. Test Setup

V1 and V2 are 3.3-V power supplies—each current limited to 7 A. Pressing SW1 simulates a short-circuit fault in V1. Figure 6 shows the circuit response to this fault.

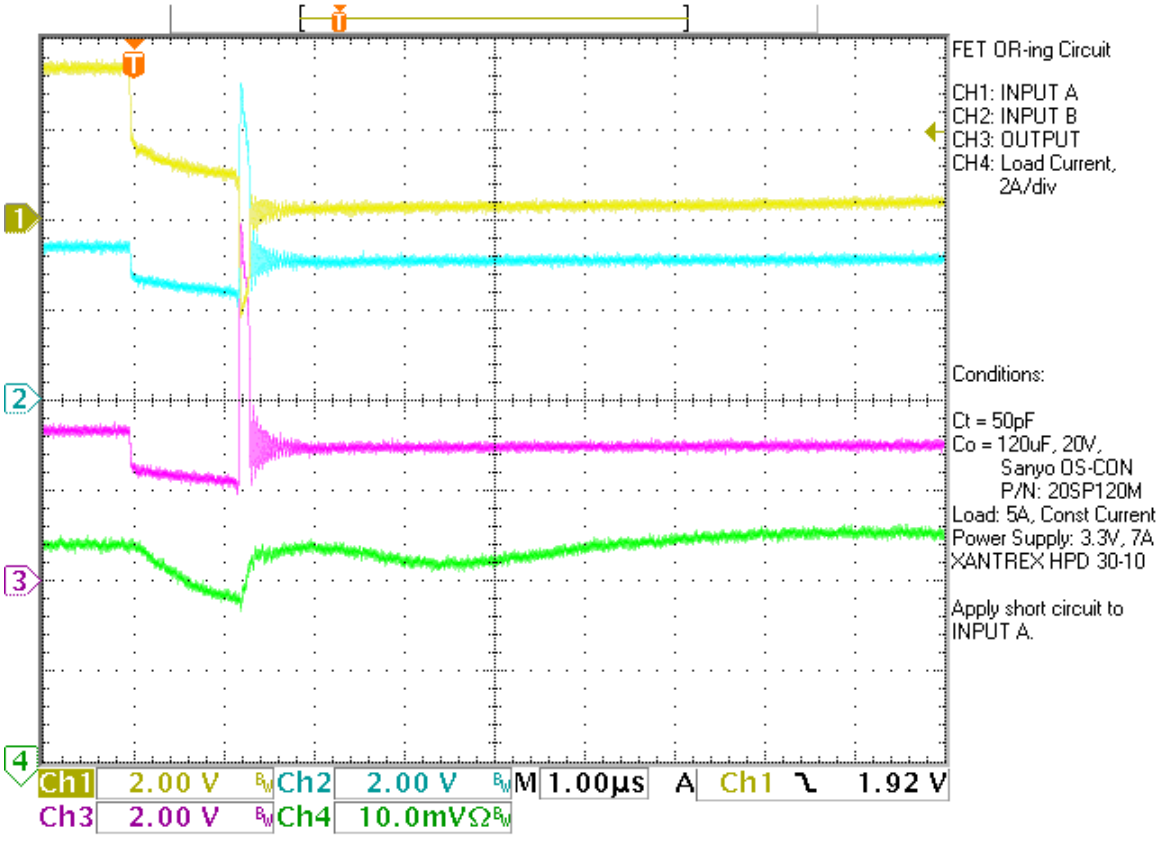


Figure 6. Test Circuit Waveforms

The fault loads down V2 and causes its output voltage to dip. This voltage dip varies inversely with the number of power supply modules. The circuit breaker eventually trips and isolates the fault from the system. The transients on trace #4 in Figure 6 are caused by active feedback inside the electronic load used to conduct the test.

A Zener diode and a series R-C snubber across the test circuit output can suppress the voltage overshoot and ringing when the circuit breaker trips.

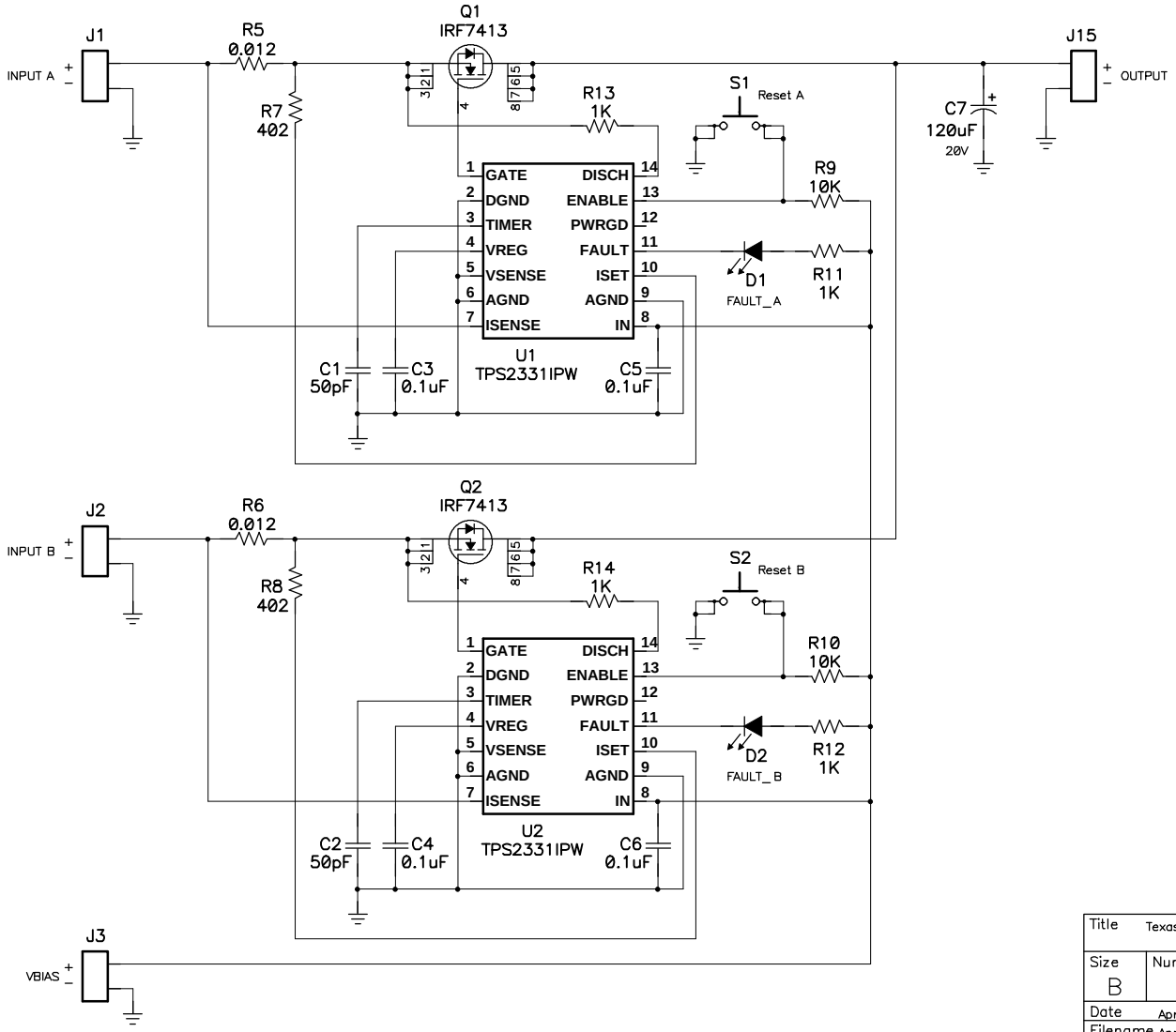
References

TPS2330, TPS2331 Single Hot-Swap Power Controllers With Circuit Breaker and Power-Good Reporting; data sheet; Texas Instruments Literature No. SLVS277; September 2001

A. Levy, *"Understanding (N+1) Redundancy, Hot Swap, Paralleling, Current Sharing, and Multiple Input Source Fault Tolerant Power Systems"*, Technology Dynamics Inc., January 4, 2002

Appendix A - Schematic Diagram

The following page shows a full schematic of a FET circuit for OR-ing two 3.3-V power supplies.



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