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Optimizing Output Voltage Ripple for the REG710

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ABSTRACT

Many portable power applications require a power source that has buck–boost capability with low output ripple. For this application, the REG710 is a prime choice; however understanding the affects of the pump and output capacitors allows designers to take full advantage of the REG710's capabilities in order to minimize output voltage ripple.

A fundamental step in minimizing output ripple is to optimize the PCB layout. A poor layout adversely affects device operation, resulting in increased output ripple, EMI, and poor regulation. To minimize these effects, the pump capacitor, output capacitor, and input capacitor should be placed as close as possible to the REG710 with the load connected directly across the output capacitor. For best performance, surface-mount ceramic capacitors should be used. For a recommended layout pattern, refer to the REG710 data sheet.

The REG710 family of products, except for the REG710–5, operates in both the buck and boost modes. Since the modes of operation are different, different techniques can be used to minimize the output ripple. The 2.5-V and 2.7-V versions of the REG710 operate in the boost mode until the input voltage increases to about 0.9 V above the nominal output voltage. At the higher input voltages, they operate in the buck mode. The 3.0 V and 3.3 V versions switch modes at about 0.7 V above the output voltage. The REG710–5 always operates in boost mode. At lower input voltages the input and output current peaks are limited by the switch on resistance. At higher input voltages the peak switch current is limited to approximately 200 mA. This prevents large inrush currents and helps to reduce both input and output ripple.

In the buck mode, the pump capacitor, Cp, is disconnected and not used. In this mode the device connects the input voltage to the output capacitor for a fixed charge time of approximately 500 ns. The discharge or *off* time is varied to regulate the output voltage. Due to the switch on resistance and switch current limit compliance, the ripple tends to get larger with higher input voltage; therefore, when reducing ripple in the buck mode, the ripple should be optimized for the maximum input voltage expected in the application. In the buck mode, the ripple is influenced by the charging time, switch on resistance, switch current limit, and output capacitor. Increasing the output capacitor is the only way to reduce output ripple in the buck mode.

In the boost mode, the REG710 synchronizes to a 1-MHz clock with a 50% duty cycle. In the first half cycle, the input voltage charges the pump capacitor. In the second half cycle, the negative terminal of the pump capacitor is placed on top of the input supply. Simultaneously the positive terminal of the pump capacitor is connected to the output, where the stored charge is delivered to the load and output capacitor. Regulation is achieved by skipping clock cycles as needed to lower the output voltage. Refer to the REG710 data sheet for illustrations detailing the different modes of operation. For the device to stay in regulation, the value of the pump capacitor must be large enough to deliver the needed charge to the output. However, a pump capacitor that is too large delivers excess charge to the output, causing the output ripple to increase. At loads under 10 mA, changing the value of the pump capacitor is the most effective method of reducing output ripple.

The first step in picking the optimum pump capacitor value in boost mode is to properly model the REG710. In boost mode, the REG710 is modeled as a voltage source in series with a source resistor. The voltage source is twice the actual input voltage, and the source resistance is given by the following formula.

$$Rsource = \frac{1}{Fmax \times Cp} \times \frac{1 + e^{\frac{-1}{4 \times Rsw \times Cp \times Fmax}}}{1 - e^{\frac{-1}{4 \times Rsw \times Cp \times Fmax}}} \qquad (1)$$

Fmax is the maximum frequency of operation, for the REG710 this value is typically 1 MHz; however, due to process variation this value may be as low as 700 kHz. Rsw is the switch on resistance. A good approximation for the switch on resistance is 2 Ω. Cp is the value of the pump capacitor and is the only variable that can be adjusted by the user. To minimize the ripple, Cp should be chosen to be as small as possible. As equation 1 suggests, lowering the value of Cp increases the value of the source resistance. The pump capacitor, Cp, can be reduced until the voltage drop across Rsource exceeds the requirement for regulation. Since solving for Cp in equation 1 can be difficult, Table 1 is included to show the relationship between Rsource and Cp for commonly available capacitors. The values in Table 1 were calculated from equation 1 assuming an Fmax of 700 kHz, an Rsw of 2 Ω, and a Cp tolerance of 10%.

Table 1. Equivalent Source Resistances for Standard Capacitor Values

Rsource (Ω)	Cp (μF)
481	0.0033
407	0.0039
338	0.0047
283	0.0056
233	0.0068
194	0.0082
159	0.01
132	0.012
106	0.015
88	0.018
72	0.022
59	0.027
48	0.033
41	0.039
35	0.047
30	0.056
26	0.068
23	0.082
21	0.1

For a given application, the value for Cp_{min} can be calculated if the minimum required input voltage and maximum load condition are known. These conditions set the worst case conditions governing the transfer of charge to the output. The equation shown below gives the maximum value of Rsource for the worst case condition.

$$Rsourcemax = \frac{2 \times Vinmin - Vout}{Ioutmax} \qquad (2)$$

Once $Rsource_{max}$ is calculated, Table 1 can be used to find the minimum value for Cp. For example, given the following conditions: Vin_{min} = 3.2 V, Vout = 5 V, $Iout_{max}$ = 10 mA the value of $Rsource_{max}$ is calculated from equation 2 to be 140 Ω. By referring to Table 1, the capacitor that gives the closest equivalent resistance less than $Rsource_{max}$ is 0.012 µF. Figure 1 shows the effect of optimizing the output ripple for the above example. Channel R1 shows the effect of decreasing the pump capacitor, while channel 1 is the output ripple with the pump and output capacitor values from EVM and product data sheet.

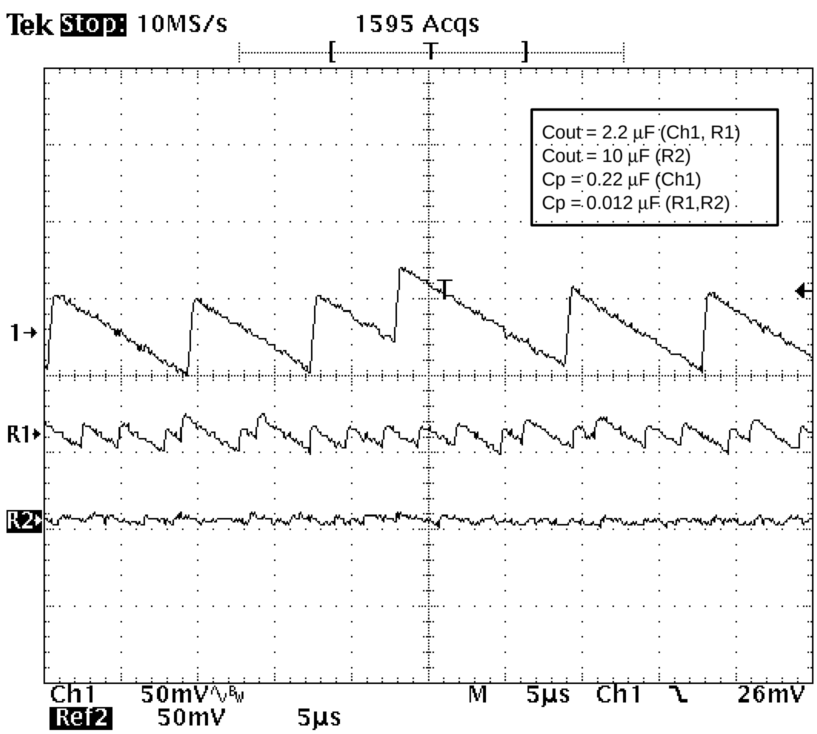

Figure 1. Output Ripple at Vin = 3.6, Iout = 10 mA

Channel R2 shows the effect of increasing the output capacitor from 2.2 µF to 10 µF with an optimized pump capacitor.

There are a few precautions to be aware of when minimizing the pump capacitor. For minimum input voltage and maximum output current, the part switches close to the maximum frequency with minimum pulse skipping. This condition produces minimum output ripple; however the REG710 is on the threshold of regulation and any increase in load current or reduction in input voltage causes the part to fall out of regulation.

At load currents above 10 mA with an output capacitor of 2.2 µF, optimizing the pump capacitor can cause an increase in output ripple when the input voltage is near Vin_{min}. At these conditions, the device has multiple output pulses between off times of typically 2 µs. Equation 3, shown below, is the equation for the output ripple for this case.

$$Vripple = \frac{Toff \times Iout}{Cout} \tag{3}$$

In general, reducing the pump capacitor below 0.22 µF is most effective for loads under 10 mA. The pump capacitor can be reduced for higher currents; however, this can cause an increase in output ripple near Vin_{min}. If the increase in output ripple near Vin_{min} is a concern, first increase the output capacitor; if further reduction in output ripple is needed, reduce the value of the pump capacitor.

References

1. *REG710 data sheet* (Texas Instruments literature number SBAS221C)

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