![TEXAS INSTRUMENTS]

Avoiding Clock Jitter With the bq2085 Advanced Gas Gauge

Battery Management

ABSTRACT

The internal-oscillator performance of the TI bq2085 advanced gas-gauge device depends on proper printed-circuit-board layout of the external 113-kΩ resistor and phase-locked loop filter components. Component placement, grounding, and crosstalk avoidance must be carefully considered in the layout.

Failure Modes

Voltage-measurement drift, voltage-measurement spikes, CEDV failure, and data-flash corruption are some of the observed effects of an unstable gas-gauge clock. The symptoms range from subtle to complete nonfunctionality depending on the severity of the disruption.

The bq2085 uses an internal phase-locked loop (PLL) to generate a high-frequency clock from the 32.768-kHz low-frequency internal oscillator. When significant jitter is present in the low-frequency oscillator, the PLL can momentarily lose lock. Fortunately, this is easy to detect with an oscilloscope by monitoring the FILT signal (pin 32).

Failure Detection Example

In Figure 1, the top trace is the 32-kHz clock output of the bq2085 (pin 35). The bottom trace is the FILT (pin 32) signal, where the recommended low-pass filter network is connected.

In normal operation, the FILT signal is a flat dc signal with a magnitude of about 0.8 V. In Figure 1 we see a significant disturbance on this pin. The jitter has caused the PLL circuit to momentarily lose lock.

In this example, the pulse on the FILT pin was found to be coincident with the bursts of communication on the I^2C lines (pins 6, 10) that occur every 40 ms. Disconnecting the I^2C lines at the bq29311 eliminated the jitter problem, demonstrating that the issue was caused by unwanted electromagnetic coupling between the I^2C lines and the printed traces associated with the ROSC signal (pin 33).
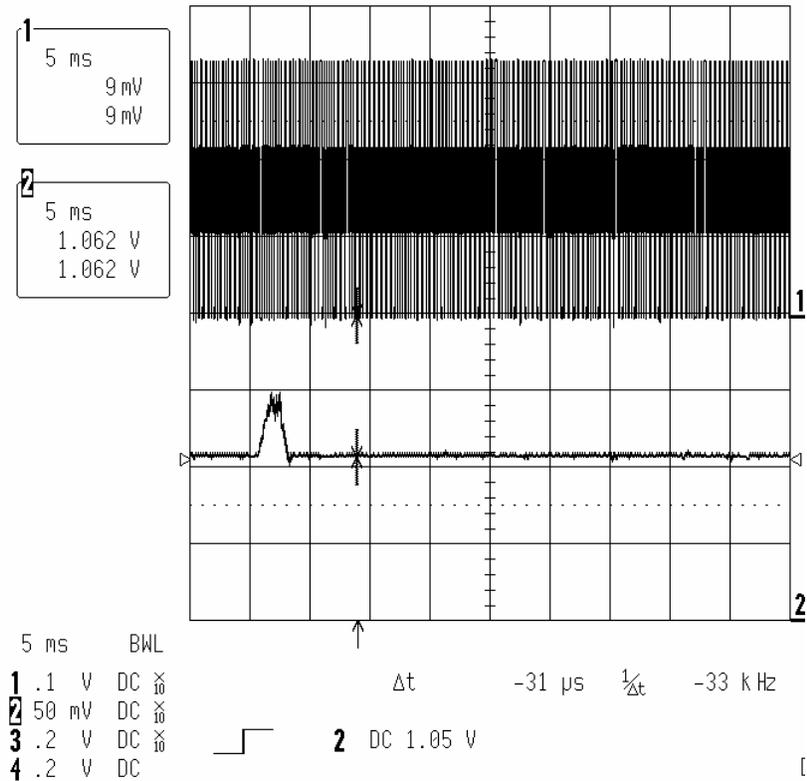
Figure 1.   bq2085 CLOCKOUT and FILT Pins

Layout Recommendations

From an electromagnetic-interference (EMI) point of view, the ROSC and FILT pins act as receivers. The SMBus and I²C communication lines, along with the CLKOUT signal act as transmitters. The PCB design and layout process must reduce the EMI potential.

ROSC Component Placement

The placement of the 113-kΩ oscillator resistor is critical. Place it close to pins 33 and 34. Connect it with absolute-minimum trace length and trace-loop areas. Place the resistor next to the IC. The recommended length of the lead to pin 33 is 3 mm or less. The trace to pin 34 must be no longer than 5 mm.

Avoid using vias to connect the oscillator resistor to either of the pins. To reduce the possibility of crosstalk, route all digital communications (I²C and SMBus) and clock signals away from pin 33 and the trace leading to the resistor, even if they are on different layers.

FILT Component Placement

The three PLL-filter components connected to the FILT signal (pin 32) must be as close as possible to the device with minimal loop area from pin 32 to analog ground.

Note that all of the digital-communication lines are on the opposite side of the TSSOP package from the critical analog nodes discussed here. However, the 32-kHz CLKOUT signal is on pin 35. In some cases, it may be helpful to place ground copper between pins 35 and 33 to shield possible coupling effects.

Grounding Considerations

Good ground layout is always desirable, not only for issues discussed here, but also for electrostatic-discharge (ESD) mitigation and to achieve optimal analog performance. Three distinct ground systems are important to understand for gas-gauge circuits: high-current ground, low-current digital ground, and low-current analog ground.

High-current ground is the battery-current-carrying path from the Pack(–) terminal to the sense resistor. Connect nothing to this trace except at the ends. Protection devices can be attached at the pack-connector end; the other ground systems are attached at the sense-resistor end.

Low-current digital ground is the return path for all of the digital components, including the processor in the bq2085 (but not its clock generator), and surprisingly, the bq29311 analog front end. Everything that can produce digital noise is referenced to this ground, which connects to the high-current ground only at a single point at the sense resistor. If possible, implement this path with a ground plane. If not, use wide traces and maximum fill where applicable.

Low-current analog ground is the return path for circuitry that benefits from a minimum of ground-induced digital noise. This includes the clock-generator circuit. The ground symbols are clearly differentiated on the reference-design schematic. As with the digital low-current ground, this ground is best implemented with a ground plane, if possible. If not, use wide traces and maximum fill where applicable.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated