Application Report
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Voltage Mode Boost Converter Small Signal Control Loop Analysis Using the TPS61030

Rick Zaitsu *PMP - PPM Converters*

ABSTRACT

A voltage-mode controlled boost converter running in continuous conduction mode is more difficult to stabilize than a buck converter due to the boost converter's inherent Right Half Plane-zero (RHP-zero). The boost converter's double-pole and RHP-zero are dependant on the input voltage, output voltage, load resistance, inductance, and output capacitance, further complicating the transfer function. Understanding the transfer function and having a method to stabilize the converter is important to achieve proper operation.

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1 Transfer Function of Boost Converter

1.1 Transfer Function of Power Stage

Figure 1 shows the block diagram of the boost converter. Using the *state space averaging model*, the small-signal transfer function from the duty cycle (*D*) of the switch to the boost converter output (v_o) in continuous conduction mode (CCM) can be derived. Equation 1 through Equation 6 are well known simplified equations for this model as derived previously in application note (SLVA061) [1].

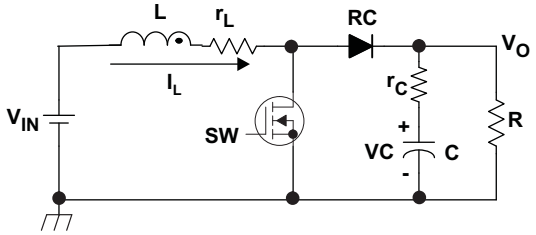


Figure 1. Boost Converter Block Diagram

$$G_{dv} = \frac{\hat{v}_O}{\hat{d}} \cong G_{do} \cdot \frac{\left(1+\frac{s}{\omega_{Z1}}\right)\cdot\left(1-\frac{s}{\omega_{RHP-zero}}\right)}{1+\frac{s}{\omega_0 \cdot Q}+\frac{s^2}{\omega_0^2}} \tag{1}$$

Where

$$G_{do} \approx \frac{V_{IN}}{(1-D)^2} = \frac{V_o^2}{V_{IN}} \tag{2}$$

$$\omega_{Z1} = \frac{1}{r_C \cdot C} \tag{3}$$

$$\omega_{RHP-zero} \approx \frac{(1-D)^2 \cdot (R-r_L)}{L} \approx \frac{R}{L}\cdot\left(\frac{V_{IN}}{V_o}\right)^2 \quad \text{or} \quad \left(f_{RHP-zero} \approx \frac{R}{2\pi \cdot L}\left(\frac{V_{IN}}{V_o}\right)^2\right) \tag{4}$$

$$\omega_0 \approx \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{r_L + (1-D)^2 \cdot R}{R}} \approx \frac{1}{\sqrt{L \cdot C}} \cdot \frac{V_{IN}}{V_o} \quad \text{or} \quad \left(f_O \approx \frac{1}{2\pi\sqrt{LC}} \cdot \frac{V_{IN}}{V_o}\right) \tag{5}$$

$$Q \approx \frac{\omega_0}{\frac{r_L}{L} + \frac{1}{C \times (R + r_C)}} \tag{6}$$

Equation 1 consists of a double-pole, RHP-zero and ESR-zero. For this discussion, the ESR-zero will be ignored because it is at a much higher frequency than the double-pole frequency and RHP-zero. Figure 2 shows a Bode plot of the double-pole transfer function.

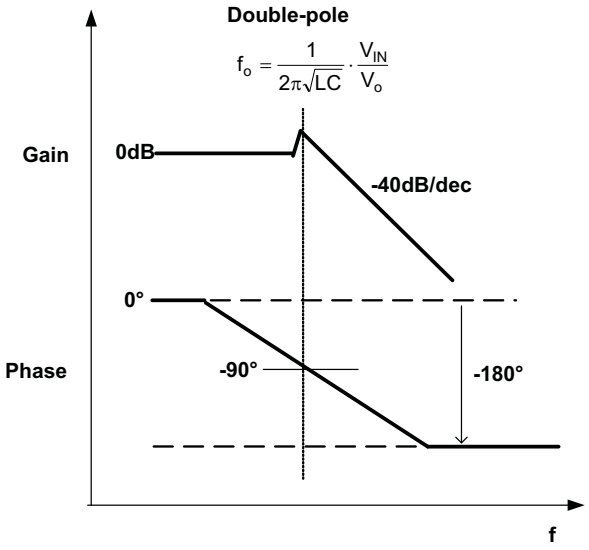


Figure 2. Bode plot of the Double-Pole Transfer Function

The double pole frequency f_O depends on the input voltage (V_{IN}) and the output voltage (V_o) as well as inductance (L) and output capacitance (C).

Figure 3 shows a Bode plot of the RHP-zero, $f_{RHP\text{-}zero}$ transfer function.

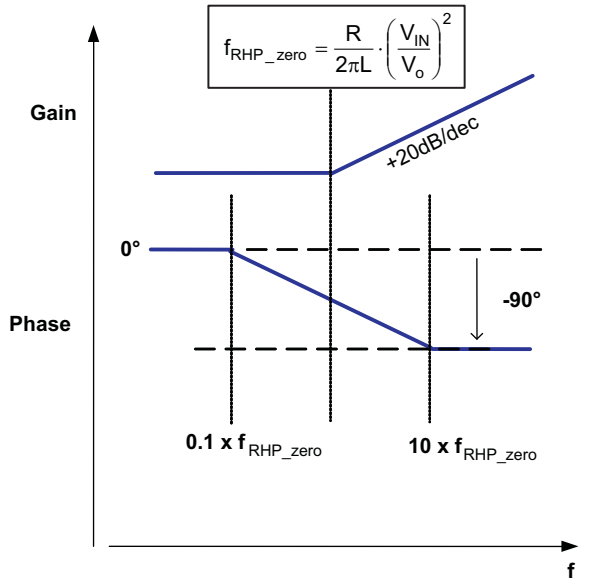


Figure 3. Bode plot of the RHP-Zero Transfer Function

It is also important to note that $f_{RHP\text{-}zero}$ depends on load resistance (R) and inductance (L) as well as input voltage (V_{IN}) and output voltage (V_o). Complicating loop gain stabilization is the fact that while the RHP-zero phase begins to drop at $0.1 \times f_{RHP\text{-}zero}$, the gain increases at 20 dB/dec from $f_{RHP\text{-}zero}$. The following example helps illustrate the RHP-zero complexity.

Consider the following parameters:

L = 10 µH,
C_o = 100 µF
V_{IN} = 3 V
V_o = 3.6 V
I_o = 2 A (R = 1.8 Ω)

The frequency of f_O and $f_{RHP\text{-}zero}$ are calculated using Equation 4 and Equation 5 as follows;

$$f_{RHP-zero} = \frac{1.8}{2\pi \times 10\,\mu H} \times \left(\frac{3}{3.6}\right)^2 = 20\ kHz \quad (7)$$

$$f_o = \frac{1}{2\pi\sqrt{10\,\mu H \times 100\,\mu F}} \times \frac{3}{3.6} = 4.2\,kHz \quad (8)$$

As shown in Figure 4, even though the addition of the RHP-zero is at a higher frequency than the converter double pole, the RHP-zero phase drop starts a decade earlier, and therefore negatively impacts the potential phase margin of the converter's control loop. This is the nature of instability of a voltage-mode controlled boost converter running in CCM.

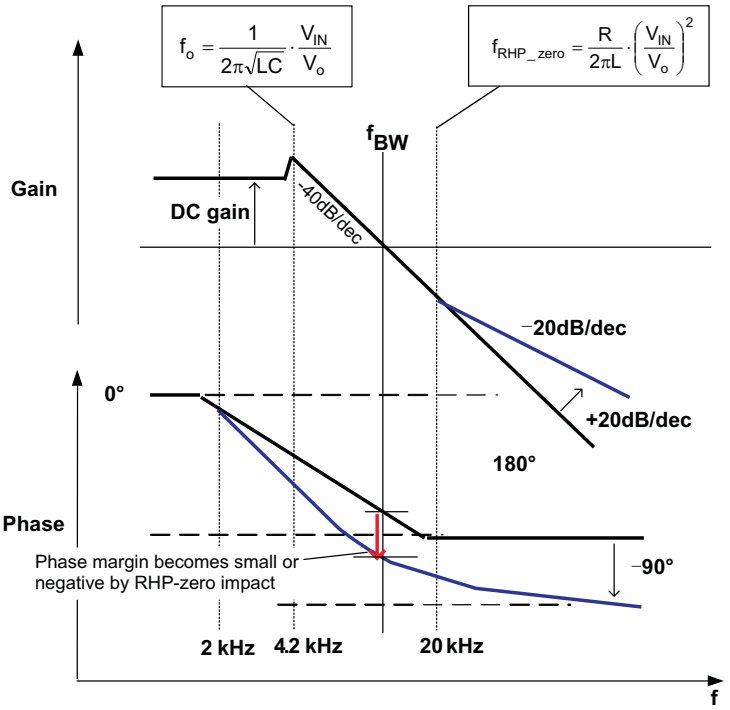


Figure 4. Bode-Plot of Boost Converter

As shown in Equation 7 and Equation 8, the f_O and $f_{RHP\text{-}zero}$ depend on V_{IN}, V_o, R (I_o), L, and C. A larger load current I_o (smaller load resistance R) has a significant impact on $f_{RHP\text{-}zero}$, bringing it closer to f_o, which decreases stability margin.

1.2 Complete CCM Boost Converter Power Stage Transfer Function

The simplified versions of Equation 1 through Equation 6 do not illustrate the effect of the output capacitor's ESR (r_c in Figure 1) and the inductors DCR (r_L) as damping factors on the double pole. In order to get an accurate bode-plot, the full version of Equation 9 and Equation 10 are used. See the appendix for the derivation of the entire equation.

$$G_{dv}(s) = \frac{\Delta v_O(s)}{\Delta D} = c(sI - A)^{-1}\frac{\partial A}{\partial D}X(s) + \frac{\partial c}{\partial D}X(s) = \frac{(R + r_C)(sCr_C + 1)\left\{-(sL + r_L)(R + r_C) + D'^2R^2\right\}}{P(s)\left\{D'R(D'R + r_C) + r_L(R + r_C)\right\}} \cdot RV_i \quad (9)$$

Where,

$$P(s) = s^2LC(R + r_C)^2 + s\left\{L(R + r_C) + r_LC(R + r_C)^2 + D'Rr_CC(R + r_C)\right\} + r_L(R + r_C) + D'R(D'R + r_C) \quad (10)$$

1.3 Complete Voltage-Mode Controlled CCM Boost Converter Transfer Function

Figure 5 shows the block diagram of a typical boost converter, consisting of the power stage, feedback and feed-forward compensation network, and error amplifier. The complete transfer function G(s) is given as;

$$G(s) = G_{dv}(s) \cdot G_{FB\_ffc}(s) \cdot G_{error}(s) \quad (11)$$

Where,

$G_{dv}(s)$; Transfer function of power stage of boost converter

$G_{FB\_ffc}(s)$; Transfer function of feedback network and feed forward compensation network

$G_{error}(s)$; Transfer function of error amp

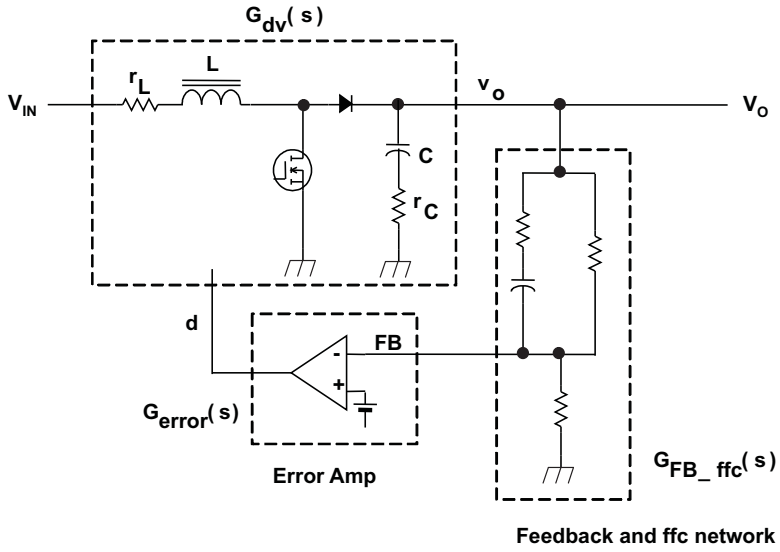


Figure 5. Block Diagram of a Typical Boost Converter

2 Method for Stabilizing the TPS61030

In order to maintain stability for boost converters with voltage mode control schemes, the following conditions must be met:

1. $f_{RHP\text{-}zero}$ must be higher in frequency than f_O (by ratio M to be explained later) in order to prevent the RHP-zero's phase drop from affecting the power stage's double-pole.
2. The crossover frequency (f_{BW}) must be set at or lower than the frequency of the maximum phase-boost effect generated by feed-forward compensation network with zero set at f_Z. If f_{BW} is set higher than the frequency of the maximum phase boost, the phase-boost effect becomes small while gain increases, reducing the stability margin.

To simplify the calculation, assume that the maximum phase-boost frequency is $2 \times f_z$. These conditions are illustrated in Figure 6.

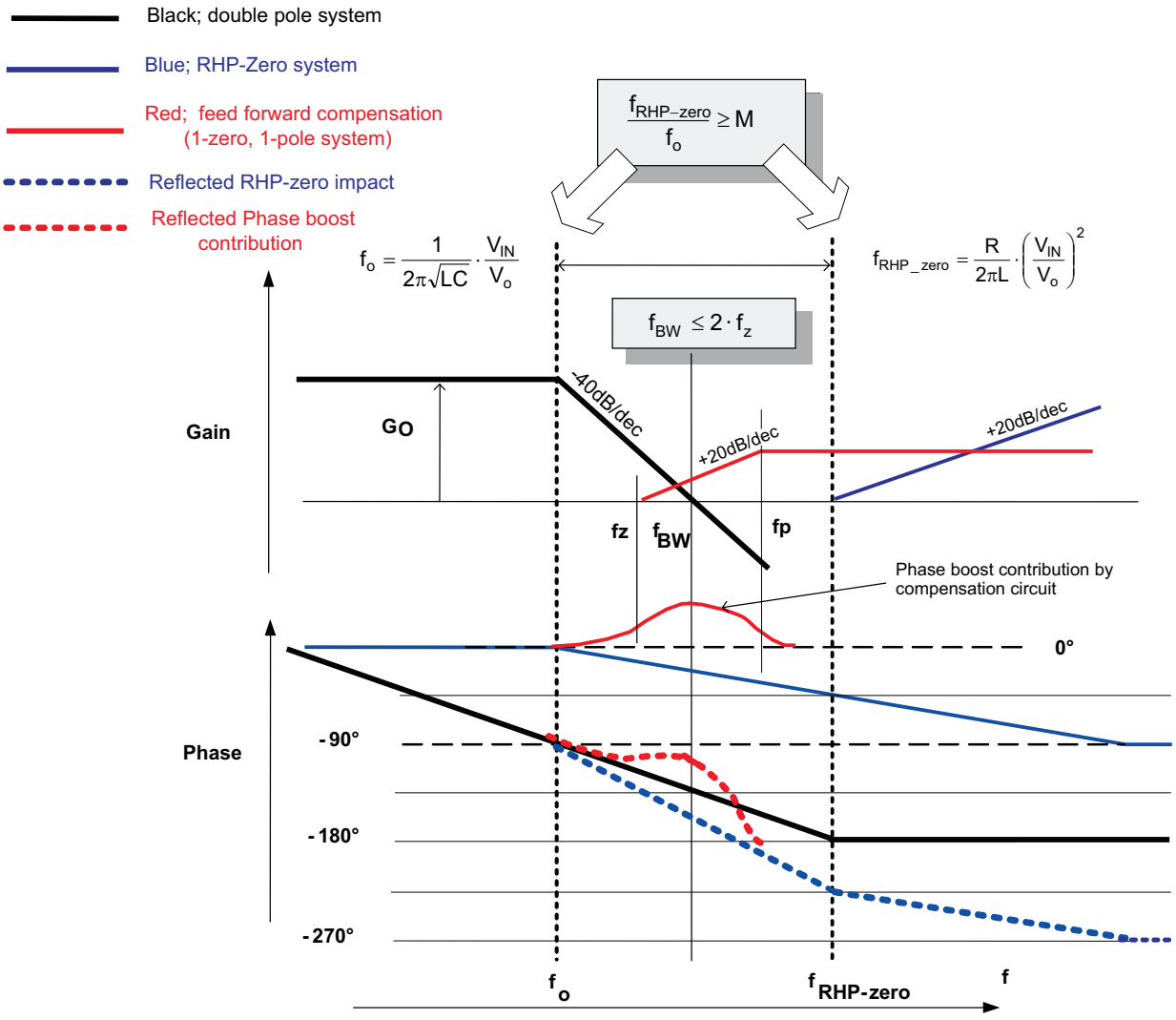


Figure 6. Bode-Plot Illustration of Stability Criteria

2.1 [STEP 1] Select Output Capacitor

Before calculating the inductance, the minimum output capacitance C_{min} is the larger of the minimum capacitance needed to provide the maximum acceptable ripple or minimum voltage dip due to a load transient. The total output ripple is the sum of the ESR ripple (Equation 12) and the output capacitor ripple (Equation 13). Subtracting the ESR ripple from the total acceptable ripple gives the maximum allowed output-capacitor ripple. Rearranging Equation 13 gives Equation 14, from which the minimum output capacitance to provide the maximum acceptable ripple is computed.

$$V_{o\_ripple\_ESR} = I_o \times ESR \tag{12}$$

$$V_{o\_ripple\_cap} = \frac{I_o \cdot T_{on}}{C} = \frac{I_o}{C} \cdot \left(1 - \frac{V_{IN}}{V_o}\right) \cdot \frac{1}{f} \tag{13}$$

$$C_{min\_ripple} = \frac{I_o}{V_{o\_ripple\_cap}} \cdot \left(1 - \frac{V_{IN}}{V_o}\right) \cdot \frac{1}{f} \tag{14}$$

The transient response should also be taken into account when selecting the output capacitance. The worst case output-voltage dip due to a load transient occurs when the output capacitor must supply the current for the transient until loop response takes over. So, if the transient duration (dt) and load current (i_{tran}) is known, Equation 15 can be used to determine the minimum required capacitance to prevent output voltage dip ($V_{O\text{-}dip}$) due to a load transient:

$$C_{min\_tran} = \frac{i_{tran}}{V_{o\_dip}} \cdot dt \approx \frac{i_{tran}}{V_{o\_dip}} \cdot \frac{1}{4 \times f_{BW}} \tag{15}$$

Where dt is approximated to $1/4 f_{BW}$ to simplify the calculation.

Increasing the output capacitance in most cases decreases the dip during load transients.

2.2 [STEP 2] Determine Inductance DCR

Similar to the output capacitor's ESR, the inductor's DCR (r_L) has a significant impact on the boost converter power stage's transfer function. In lower output-current applications, relatively high DCR helps the stability by phase damping. The maximum allowable DCR is determined by the amount of loss that is acceptable, i.e., the maximum efficiency required at maximum load. The total power loss consists of the inductor AC and DC losses, SW (N-MOS FET) loss, Diode (P-MOS FET) loss, and control-circuitry power loss. To simplify the calculation, the designer can ignore the inductor's AC losses, compute the inductor's DC loss $I_{in}^2 \cdot r_L$ (by ignoring ripple component), and set the maximum acceptable inductor DC loss to 30% of the total power loss.

So, setting a target efficiency η,

$$r_{L\_MAX} = \frac{30\% \times P_{total-loss}}{I_{in}^2} \tag{16}$$

Where, $P_{total\_loss} = P_{out} \times \left(\frac{1}{\eta} - 1\right)$

2.3 [STEP 3] Separating the Double-Pole and RHP-Zero Frequencies

Separating the double-pole and RHP-zero frequencies is the most important requirement for maintaining stability. M is the frequency separation ratio between $f_{RHP\text{-}zero}$ and f_o, and provides a relative measure of phase drop between the two frequencies. Through empirical testing it has been determined that the phase damping received from tantalum output capacitors with ESR values between 20 mΩ to 100 mΩ allows a value of M=10. When using ceramic capacitors that have ESR values of a few mΩ, thus providing a little phase damping between the two frequencies, more frequency separation is required (M≥15). Note M=10 or M=15 are starting points and final stability should be verified by transient testing in the lab (as mentioned in [STEP 5]).

$$\frac{f_{RHP-zero}}{f_o} \geq M \tag{17}$$

Where,

M=10 (one decade) — for tantalum capacitors.

M=15 — for ceramic capacitors.

Using Equation 4 and Equation 5, we can get:

$$L \leq C \cdot \left(\frac{R}{M} \cdot \frac{V_{IN}}{V_o} \right)^2 \tag{18}$$

When load resistance R is at its minimum (meaning I_o is MAX) and the input voltage is at its minimum, the f_o and $f_{RHP\text{-}zero}$ are closest (as shown in Equation 4 and Equation 5) and open loop phase margin is at its minimum. Therefore, Equation 19 provides the maximum limitation of inductance.

$$L_{MAX} = C \cdot \left(\frac{R_{min}}{M} \cdot \frac{V_{IN\_min}}{V_o} \right)^2 \tag{19}$$

2.4 [STEP 4] Maximize Phase Boost Effect of Feed Forward Compensation Network

Figure 7 shows the feedback network and feed-forward compensation (ffc) network. The complete transfer function, zero frequency and pole frequency equations are shown in Equation 20 through Equation 22, respectively.

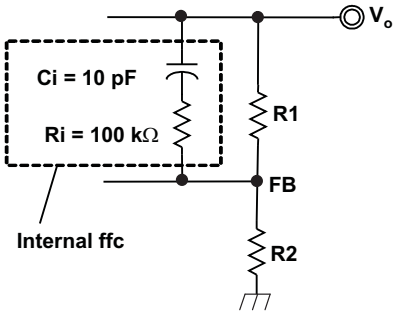


Figure 7. Feedback network and Feed Forward

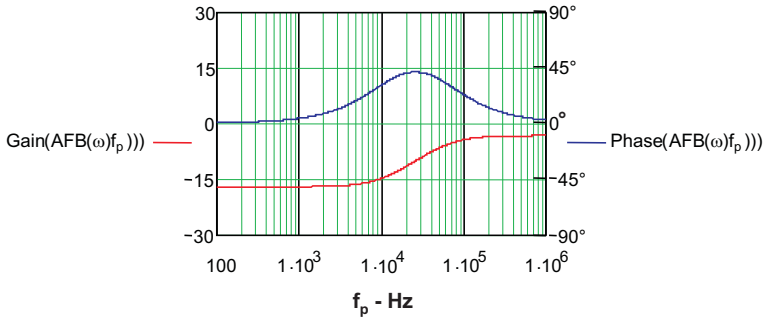
Compensation Network

$$G(s) = \frac{1 + sC_i\left(R1 + R_i\right)}{1 + \frac{R1}{R2} + sC_i\left(R1 + R_i + \frac{R1R_i}{R2}\right)} \tag{20}$$

$$fz = \frac{1}{2\pi C_i\left(R1 + R_i\right)} \tag{21}$$

$$fp = \frac{1}{2\pi C_i \times \frac{R1R2 + R_iR2 + R1R_i}{R1 + R2}} \tag{22}$$

Figure 8 shows the calculated transfer function of this network when R1=1.24 MΩ, R2=200 kΩ, Ci=10 pF, and Ri=100 kΩ. Here Ri and Ci are the integrated ffc network shown in the TPS61030 data sheet. The calculated results are fz=11 kHz, fp=58 kHz, and the maximum phase boost frequency is around 25 kHz as shown in Figure 8. Note that f_z varies for different output voltages due to R1.



$$f_z = \frac{1}{2 \cdot \pi \cdot C_i \cdot (R1 + R2)} \qquad f_p = \frac{1}{2 \cdot \pi \cdot C_i \cdot \left(\frac{(R1 \cdot R2) + (R_i \cdot R2) + (R1 \cdot R_i)}{R1 + R2} \right)}$$

$$f_z = 1.105 \times 10^4 \qquad f_p = 5.84 \times 10^4$$

Figure 8. Example of Transfer Function of Feedback Network and Feed Forward Compensation Network

In order to simplify the calculation, assume the maximum frequency for phase boost from the feed-forward network is 2 × f_z.

$$f_{BW} \le 2 \cdot f_Z \tag{23}$$

Where:

$$f_{BW} \cong f_o \cdot 10^{\frac{G_O}{30}} \tag{24}$$

$$G_o(dB) = 20 \log\left(G_{do} \cdot \frac{5 \cdot R2}{R1 + R2} \right) = 20 \times \log\left(\frac{V_o^2}{V_{IN}} \cdot \frac{5 \cdot R2}{R1 + R2} \right) \tag{25}$$

Noting that the double-pole has a –40-dB/dec theoretical roll-off, but –30 dB/dec was used to approximate the damping effects of the output capacitor's ESR and the inductor's DCR.

Using Equation 5 and Equation 23 through Equation 25 we can get:

$$L \ge \frac{1}{C} \cdot \left(\frac{1}{2\pi} \cdot \frac{V_{IN}}{V_o} \cdot \frac{10^{\frac{G_o}{30}}}{2 \cdot f_Z} \right)^2 \tag{26}$$

As shown in Equation 5 f_o; therefore, f_{BW}, becomes the highest frequency when input voltage V_{IN} is at maximum. Therefore, L_{min} is calculated when V_{IN} is at maximum.

$$L_{min} = \frac{1}{C} \cdot \left(\frac{1}{2\pi} \cdot \frac{V_{IN\_MAX}}{V_o} \cdot \frac{10^{\frac{G_o}{30}}}{2 \cdot f_z} \right)^2 \tag{27}$$

2.5 [STEP 5] Evaluating the Stability Experimentally

The Bode plot obtained from loop gain measurements is important to consider for stability, but should be verified by transient-response test results. To ensure that the load step has frequency components up to the control loop bandwidth, the rise time of the current step should be faster than $1/f_{BW}$. The transient-response test includes not only the small signal response, but also the large signal response behavior that occurs in normal applications, while the measured Bode plot shows only the small signal response.

The criteria for evaluating stability using a load-transient test is that if the output rings more than 3 times before settling, the converter has low phase margin and should be re-compensated.

Figure 9 summarize the flow chart of design procedure for stability.

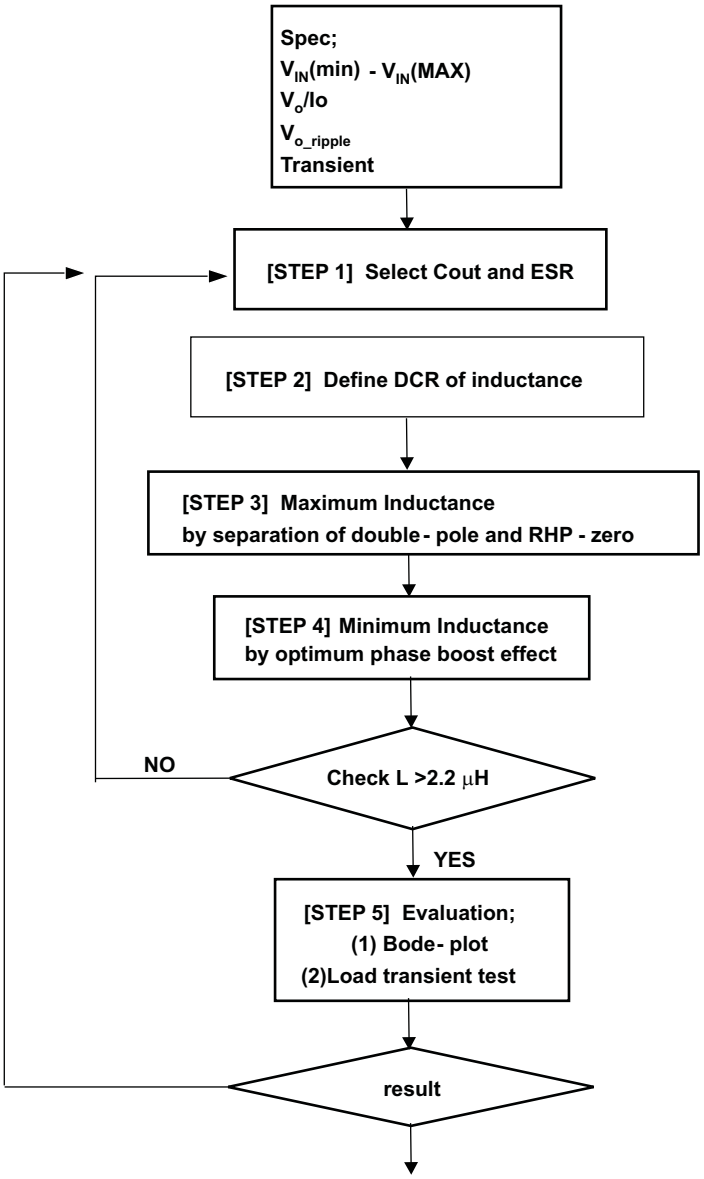


Figure 9. Flow Chart of Design Process

3 Example 1; High Output Current (2 A) With Tantalum Capacitor

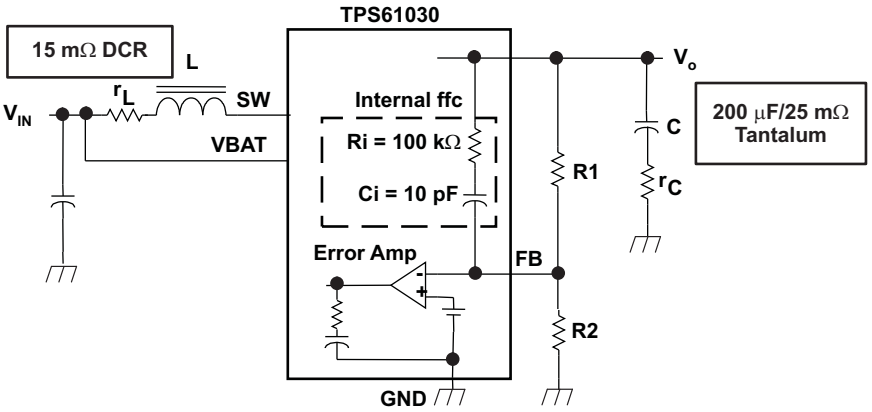


Figure 10. Block Diagram of Converter

The parameters are:

V_{IN} = 3.0 V–3.3 V
V_o = 3.6 V
I_o = 2 A (7.2 W)
V_{o_ripple} = 5 mV (by capacitance)
Target efficiency 90% (Ploss = 0.8 W, Iin = 2.67 A at 3.0 V_{IN})
$V_{o\_transient}$ = 250 mV (assume transient I_o = 0 A to 2 A, and f_{BW} = 10 kHz for calculation purpose below)

Calculating the minimum capacitance using the criteria of the output voltage ripple from Equation 14;

$$C_{min\_ripple} = \frac{I_o}{V_{o\_ripple\_cap}} \cdot \left(1 - \frac{V_{IN}}{V_o}\right) \cdot \frac{1}{f} = \frac{2}{5mV} \times \left(1 - \frac{3}{3.6}\right) \times \frac{1}{600kHz} \approx 100\mu F \quad (28)$$

F.Y.I; Ripple caused by ESR is

$V_{o\_ripple\_ESR} = I_o \times ESR = 2\ A \times 25\ m\Omega = 50\ mV$.

Calculating the minimum capacitance using the criteria of the transient output voltage dip from Equation 15;

$$C_{min\_tan} = \frac{i_{tran}}{V_{o\_dip}} \cdot \frac{1}{4f_{BW}} = \frac{2A}{250mV} \times \frac{1}{4 \times 10kHz} = 200\mu F \quad (29)$$

From the result of Equation 28 and Equation 29, 200µF was chosen.

In Figure 10, the feedback network consists of R1=1.24 MΩ and R2=200 kΩ. TPS61030 has internal feed forward compensation network (Ri and Ci) across top resistor R1.

$$G_o(dB) = 20 \times \log\left(\frac{V_o^2}{V_i} \times \frac{5 \times R2}{R1 + R2}\right) = 9.5(dB) \quad (30)$$

$$L_{MAX} = C \cdot \left(\frac{R_{min}}{10} \cdot \frac{V_{IN\_min}}{V_o}\right)^2 = 200\,\mu F \times \left(\frac{1.8}{10} \times \frac{3}{3.6}\right)^2 = 4.5\,\mu H(MAX) \quad (31)$$

$$L_{min} = \frac{1}{C} \cdot \left(\frac{1}{2\pi} \cdot \frac{V_{IN\_MAX}}{V_o} \cdot \frac{10^{\frac{Go}{30}}}{2 \cdot f_Z}\right)^2 = \frac{1}{200\,\mu F} \times \left(\frac{1}{2\pi} \times \frac{3.3}{3.6} \times \frac{10^{\frac{G_o}{30}}}{2 \times 11k}\right)^2 = 1\mu H(min) \quad (32)$$

$$r_{L\_MAX} = \frac{P_{Inductance\_loss}}{I_{in\_MAX}^2} = \frac{0.24W}{2.67\ A^2} = 33\ m\Omega \quad (33)$$

Where, $P_{induc\ tan\ ce\_loss} = 30\% \times P_{LOSS} = 30\% \times 0.8\ W = 0.24\ W$

Using the stability design rules, the allowable inductance range is 1 µH to 4.5 µH. Using the efficiency design requirements, the allowable DCR (r_L) of the inductor is less than 33 mΩ. Figure 11 shows a Mathcad™-calculated Bode plot of the transfer function including the boost power stage, feedback network, feed forward compensation network, and error amp. The inductance values used for these calculations is 6.8 µH, 3.9 µH and 2.2 µH to demonstrate how stability improves due to changing the inductance. The phase gain (M) achieved using these inductance values are as follows:

L = 6.8 µH is M=8
L = 3.9 µH is M=11
L = 2.2 µH is M=15

The calculations consolidate the inductor's DCR and the *ON* resistance of internal SW into one 50 mΩ resistor in order to simplify the calculation.

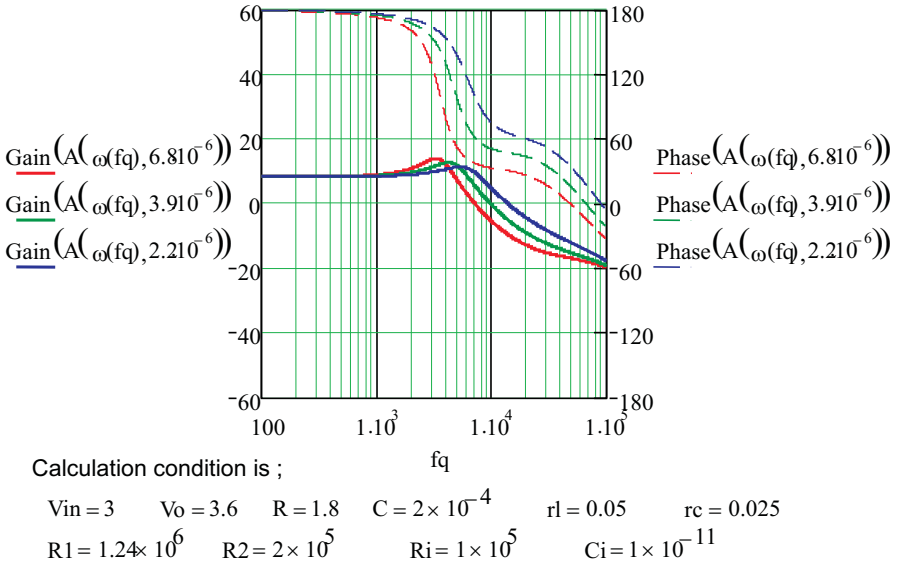


Figure 11. Mathcad Calculated Bode-Plot of Transfer Function for High Current With Tantalum Output Capacitor

Figure 12 shows the measured Bode-plot of the transfer function and load-transient test waveform. When L=6.8 µH (frequency separation ratio M=8), the transient response shows slight ringing while settling. This is a symptom of low phase margin. When L=3.9 µH, which is M=11, the transient test shows good response with no ringing while settling. As shown in Equation 17, M>10 is reasonable to provide enough stability margin when a tantalum output capacitor used. 2.2 µH shows acceptable phase margin as well. The iInductance DCR used in the test is around 15 mΩ.

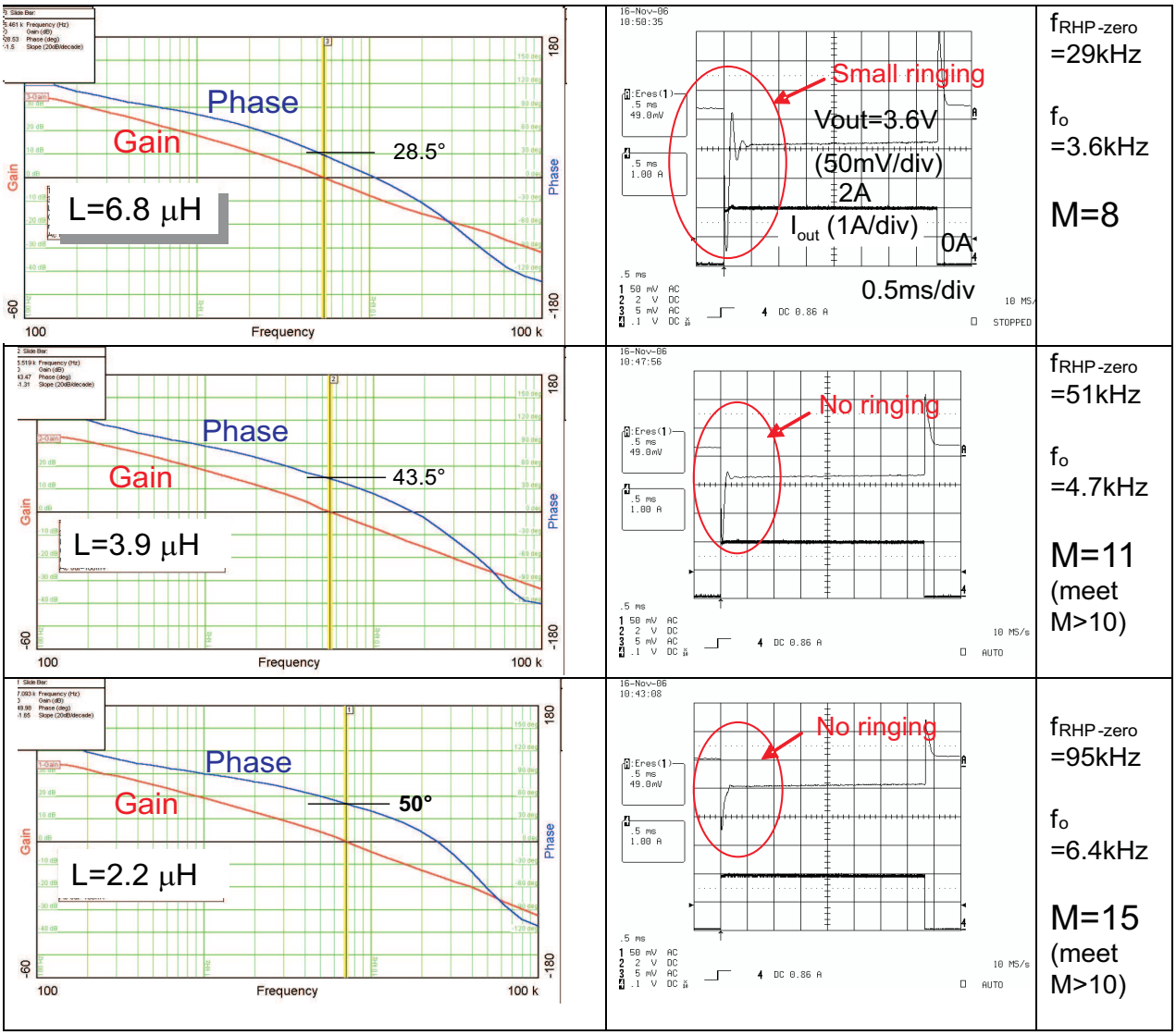


Figure 12. Measured Bode-Plot and Load Transient Waveform With Tantalum Capacitor (V_{IN} = 3.0 V, V_o = 3.6 V, I_o = 2 A, C = 100 µF × 2 tantalum capacitor)

4 Example 2; High Output Current (2 A) With Ceramic Capacitor

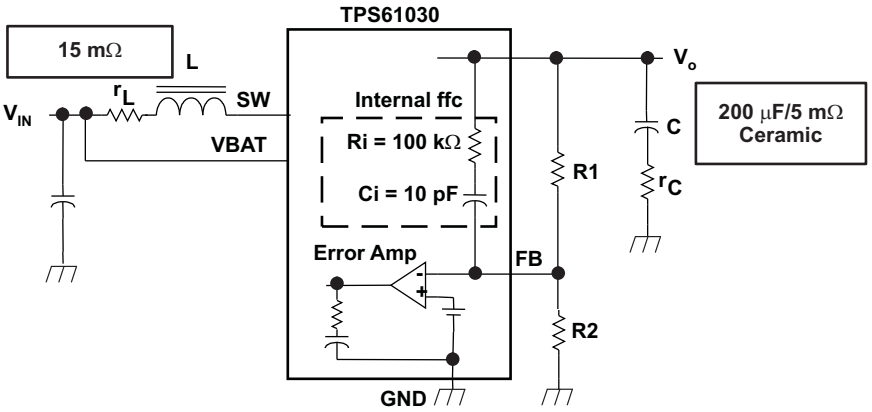


Figure 13. Block Diagram of Converter

The next example uses the same parameters as the previous example but with a ceramic output capacitor.

V_{IN} = 3.0 V–3.3 V
V_o = 3.6 V
I_o = 2 A

With ceramic capacitors on the output, special attention is needed for stability due to the low ESR. The target of the frequency separation is M>15 as shown by Equation 17.

Following the calculation process,

$$L_{MAX\_ceramic} = C \cdot \left(\frac{R_{min}}{15} \cdot \frac{V_{IN\_min}}{V_o} \right)^2 = 2\,\mu H \tag{34}$$

$$L_{min\_ceramic} = \frac{1}{C} \cdot \left(\frac{1}{2\pi} \cdot \frac{V_{IN\_MAX}}{V_o} \cdot \frac{10^{\frac{Go}{30}}}{2 \cdot f_Z} \right)^2 = \frac{1}{200\,\mu F} \times \left(\frac{1}{2\pi} \times \frac{3.3}{3.6} \times \frac{10^{\frac{G_o}{30}}}{2 \times 11 k\Omega} \right)^2 = 1\,\mu H(min) \tag{35}$$

From the calculation results, the range of inductance is 1 µH to 2 µH. Choose 2.2 µH due to minimum inductance requirement in the data sheet.

Figure 14 shows a Mathcad-calculated Bode-plot of the transfer function with ESR=5 mΩ (assuming capacitor ESR and connection resistance total 5 mΩ). The phase curve is steeper in Figure 14 than Figure 11, which means that the phase margin is smaller. Inductance values of 6.8 µH, 3.9 µH and 2.2 µH were used to demonstrate how stability improves even though L=6.8 µH (M=8) and L=3.9 µH (M=11) do not satisfy the M>=15 guideline. The calculated Bode-plot curve in Figure 14 shows that the phase margin is 20° for L=6.8 µH, and 30° for L=3.9 µH. The 2.2-µH (M=15) inductor provides a 45° phase margin shown in Figure 14.

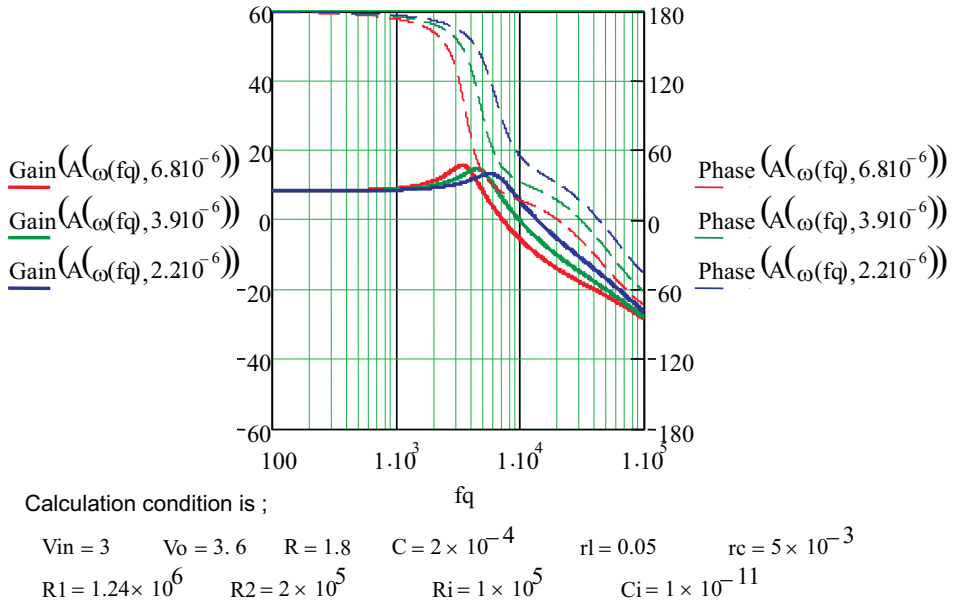


Figure 14. Mathcad Calculated Bode-Plot of Transfer Function for High Output Current and Ceramic Output Capacitor

Figure 15 shows the measured Bode-plot of the transfer function and load-transient test waveform. To ensure that biasing has not reduced the effective output capacitance, two 100 µF/6.3 V ceramic capacitors plus one 47 µF/6.3 V ceramic capacitor in parallel were used to provide an effective 200 µF of output capacitance.

L=6.8 µH (M=8) and L=3.9 µH (M=11) show ringing during settling time at transient test, indicating that the phase margin is too low. When L=2.2 µH (M=15), no ringing was observed, indicating adequate phase margin.

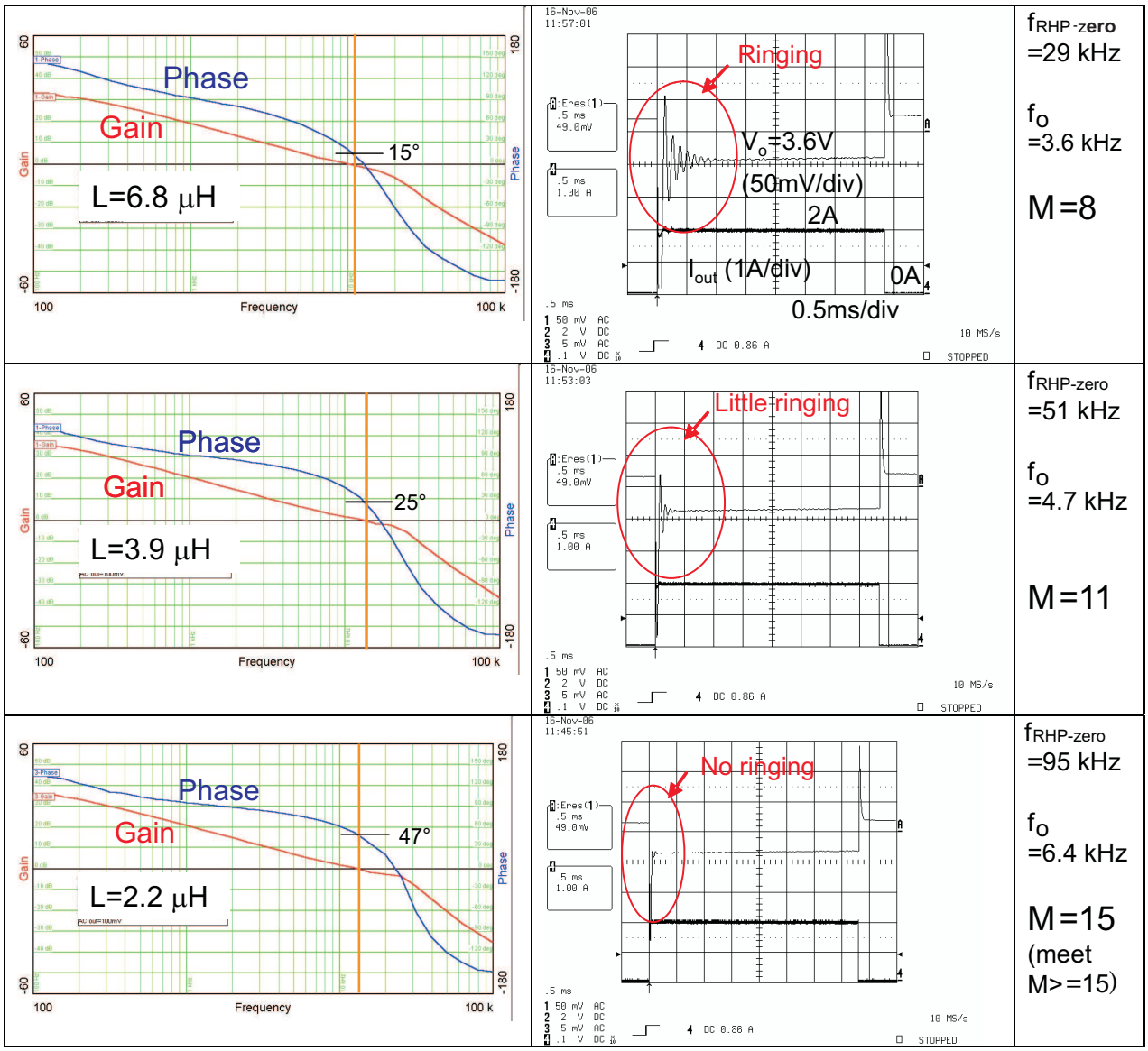


Figure 15. Measured Bode-Plot and Load Transient Waveform With Ceramic Capacitor (V_{IN} = 3.0 V, V_o = 3.6 V, I_o = 2 A, C = 100 µF × 2 Ceramic Capacitor)

5 Example 3; Low Output Current (I_o = 0.4 A) With Ceramic Capacitor

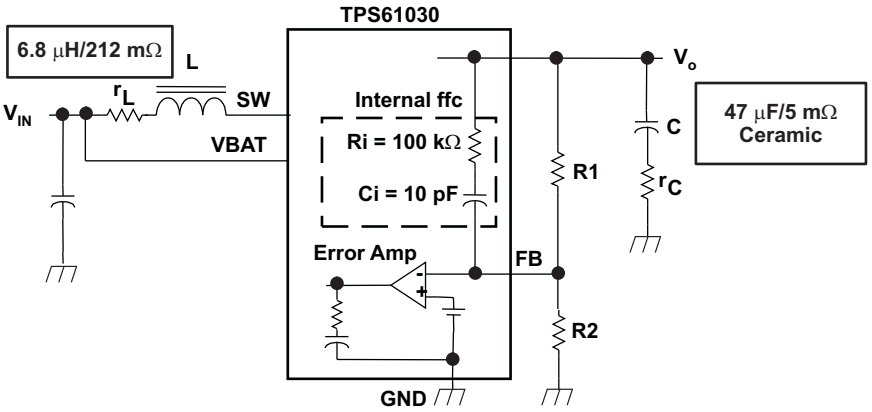


Figure 16. Block Diagram of Converter

V_{IN} = 3.0 V–3.3 V
V_o = 3.6 V
I_o = 0.4 A (R = 9 Ω) (1.44 W)
V_{o_ripple} = 5 mV (by capacitance)
Target efficiency 90% (P_{loss}=0.16 W, I_{IN}=0.53 A at 3.0 V_{IN})
$V_{o\_transient}$=250 mV (assume transient I_o=0 A to 0.4 A, and f_{BW}=10kHz for calculation purpose below)

Following the design process;

$$C_{min\_ripple} = \frac{I_o}{V_{o\_ripple\_cap}} \cdot \left(1 - \frac{V_{IN}}{V_o}\right) \cdot \frac{1}{f} = \frac{0.4}{5\,mV} \times \left(1 - \frac{3}{3.6}\right) \times \frac{1}{600\,kHz} = 22\,\mu F \quad (36)$$

$$C_{min\_tran} = \frac{i_{tran}}{V_{o\_dip}} \cdot \frac{1}{4 f_{BW}} = \frac{0.4\,A}{250\,mV} \times \frac{1}{4 \times 10\,kHz} = 40\,\mu F \quad (37)$$

From the result of Equation 36 and Equation 37, 47 µF ceramic capacitor available was chosen.

$$L_{MAX} = C \cdot \left(\frac{R_{min}}{15} \cdot \frac{V_{IN\_min}}{V_o}\right)^2 = 47\,\mu F \times \left(\frac{9}{15} \times \frac{3}{3.6}\right)^2 = 12\,\mu H(MAX) \quad (38)$$

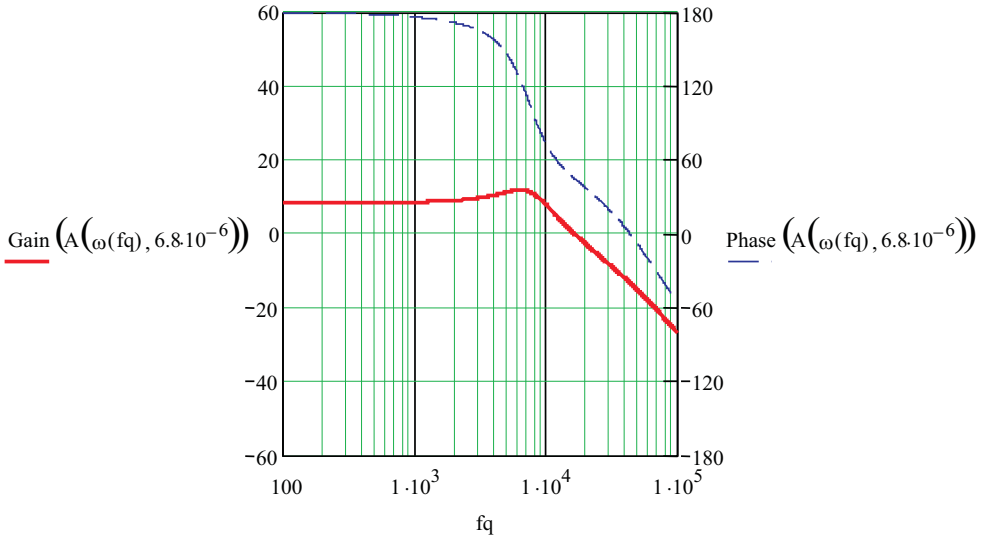
$$L_{min} = \frac{1}{C} \cdot \left(\frac{1}{2\pi} \cdot \frac{V_{IN\_MAX}}{V_o} \cdot \frac{10^{\frac{Go}{30}}}{2 \cdot f_Z}\right)^2 = \frac{1}{47\,\mu F} \times \left(\frac{1}{2\pi} \times \frac{3.3}{3.6} \times \frac{10^{\frac{G_o}{30}}}{2 \times 11\,k\Omega}\right)^2 = 4\,\mu H(min) \quad (39)$$

$$r_{L\_MAX} = \frac{P_{Inductance\_loss}}{I^2_{in\_MAX}} = \frac{0.048W}{0.53\,A^2} = 170\,m\Omega \quad (40)$$

Where, $P_{inductance}$ = 30% × P_{LOSS} = 30% × 0.16 W = 0.048 W

The calculated inductance range is 4 µH to 12 µH. For this discussion 6.8 µH is chosen. The inductance used has a saturation current of 0.8 A (r_L=212 mΩ, higher than 170 mΩ but acceptable practically) to handle the maximum input current of 0.6 A. From Equation 1 through Equation 10, we know the inductor DCR (r_L) has a damping effect similar to the capacitor r_C. In low power applications, the relatively large DCR (r_L) helps to offset the instability caused by the low ESR (r_C) of the ceramic capacitors.

Figure 17 shows a Bode plot of the Mathcad-calculated transfer function with inductor L=6.8 µH, and rL=250 mΩ (after consolidating the inductance DCR and SW *ON* resistance) and ceramic output capacitor of 47 µF/5 mΩ. The expected phase margin is 50°.



Calculation condition is ;

$Vin = 3 \quad Vo = 3.6 \quad R = 9 \quad C = 4.7 \times 10^{-5} \quad rl = 0.25 \quad rc = 5 \times 10^{-3}$

$R1 = 1.24 \times 10^{6} \quad R2 = 2 \times 10^{5} \quad Ri = 1 \times 10^{5} \quad Ci = 1 \times 10^{-11}$

Figure 17. Mathcad Calculated Bode-Plot of Transfer Function for Low Output Current and Ceramic Output Capacitor

Figure 18 shows the measured transient response. The inductor used is 6.8 µH, 0.81 A_sat, 212 mΩ, Based on the transient waveform, the application is stable.

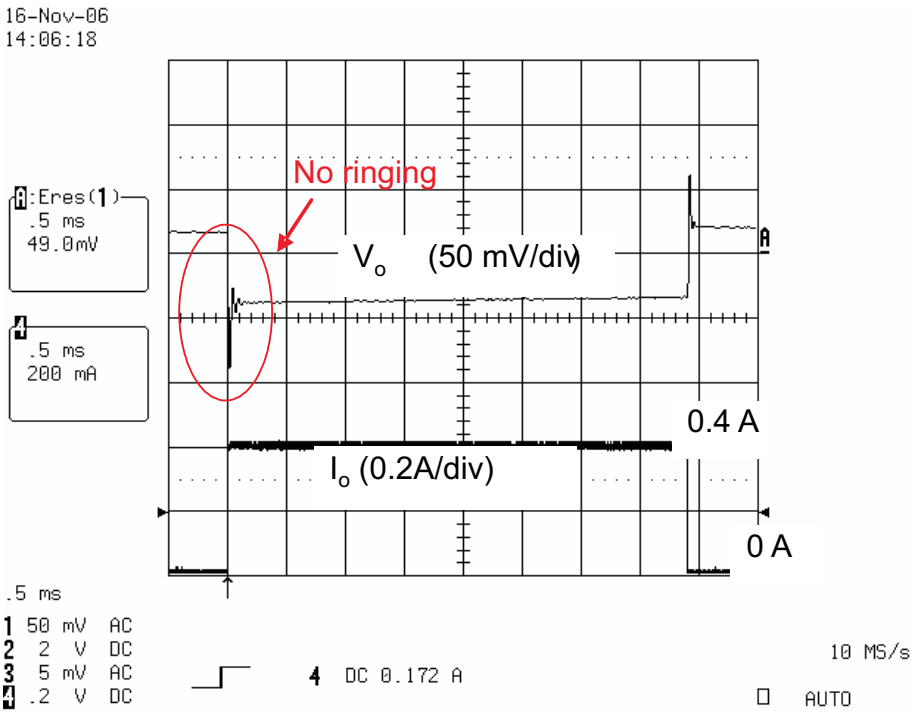


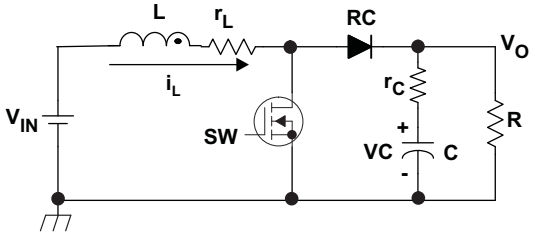
Figure 18. Measured Load Transient Waveform

6 Conclusion

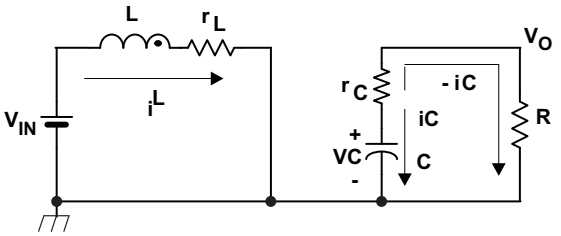
A transfer function for a voltage-mode boost converter in continuous-conduction mode was developed using *state space averaging model*. From the transfer function, the challenges of stabilizing a voltage-mode boost converter were explained, and a design procedure for achieving loop stability was provided.

Appendix A State Space Averaging Method

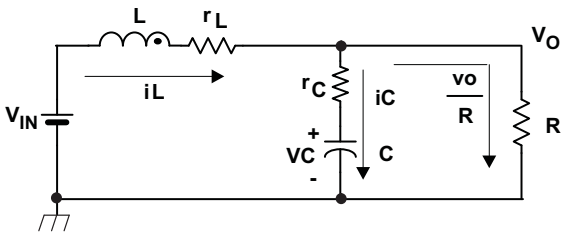
Deriving Transfer function using state space averaging method.



[State 1: SW ON]



[State 2: SW OFF]



State 1 [SW: ON, RC: OFF]

$$V_{in} = L\frac{di_L}{dt} + i_L r_L . \quad \text{(A1)}$$

$$i_C = C\frac{dv_C}{dt} . \quad \text{(A2)}$$

$$v_C = -i_C(R + r_C) . \quad \text{(A3)}$$

$$v_O = v_C + r_C i_C . \quad \text{(A4)}$$

State 2 [SW: OFF, RC: ON]

$$V_{in} = L\frac{di_L}{dt} + r_L i_L + v_O \quad \text{(A5)}$$

$$i_C = C\frac{dv_C}{dt} . \quad \text{(A6)}$$

$$i_L = i_C + \frac{v_O}{R} . \quad \text{(A7)}$$

$$v_O = v_C + r_C i_C . \quad \text{(A8)}$$

By *State Space Averaging Method*, the state averaging equations are described as follows.

$$\begin{cases} \dfrac{dX}{dt} = AX + bV_{in} \\ v_O = cX\,. \qquad \text{where } X = \begin{bmatrix} i_L \\ v_C \end{bmatrix}. \end{cases} \tag{A9}$$

The state equation is derived as below.

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} i_L \\ v_C \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{L}\left(r_L + \dfrac{D'R \cdot r_C}{R + r_C}\right) & -\dfrac{D'R}{L(R + r_C)} \\ \dfrac{D'R}{C(R + r_C)} & -\dfrac{1}{C(R + r_C)} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} V_{in} \\ v_O = \begin{bmatrix} \dfrac{D'R \cdot r_C}{R + r_C} & \dfrac{R}{R + r_C} \end{bmatrix}\begin{bmatrix} i_L \\ v_C \end{bmatrix} \end{cases} \tag{A10}$$

AC analysis (small signal transfer function)

Gdv transfer function from Duty to Output voltage is derived as follows.

$$G_{dv}(s) = \frac{\Delta v_O(s)}{\Delta D} = c(sI - A)^{-1}\frac{\partial A}{\partial D}X(s) + \frac{\partial c}{\partial D}X(s) = \frac{(R + r_C)(sCr_C + 1)\left\{-(sL + r_L)(R + r_C) + D'^2R^2\right\}}{P(s)\left\{D'R(D'R + r_C) + r_L(R + r_C)\right\}} \cdot RV_i$$

Where:

$$P(s) = s^2LC(R + r_C)^2 + s\left\{L(R + r_C) + r_LC(R + r_C)^2 + D'Rr_CC(R + r_C)\right\} + r_L(R + r_C) + D'R(D'R + r_C)$$

A.1 Reference

1. *Understanding Boost Power Stages in Switchmode Power Supplies* (SLVA061), Everett Rogers, Texas Instruments, March 1999.

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