Designing with the TPS23753 Powered-Device and Power Supply Controller

Eric Wright   *HPA/Power Interface*

ABSTRACT

The TPS23753 is an IEEE 802.3-2005-compliant powered-device and power supply controller optimized for isolated converter topologies. This application report provides a comprehensive design example for the TPS23753EVM-002 evaluation module (EVM). This EVM is targeted at low-cost, simple, 7-W flyback converter applications.

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1 Introduction

The TPS23753 supports designs using isolated flyback converter topologies. Benefits include lower voltage operation along with built-in features including:

- Devices optimized for isolated converters
- Programmable frequency with synchronization
- Adjustable leading-edge blanking
- Simplified dc/dc control 100-V ratings
- –40°C to 125°C junction temperature range
- Current and inrush limit
- Thermal protection

2 Design Example and Component Selection

Table 1 outlines the electrical requirements for this design example.

Table 1. TPS23753EVM-002 Electrical Specifications

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
POWER INTERFACE						
Input voltage	Applied to the power pins of connectors J1 or J2		0	–	57	V
Operating voltage	After start-up		30	–	57	
Input UVLO	Rising input voltage		–	–	36	
	Falling input voltage		30	–	–	
DC/DC CONVERTER						
Output voltage	20 V ≤ Vin ≤ 57 V, $I_{LOAD} ≤ I_{LOAD}$ (max) 10.8 V ≤ Vin ≤ 13.2 V, $I_{LOAD} ≤ I_{LOAD}$ (max)	3.3-V output	3.13	3.3	3.47	V
Output current	20 V ≤ Vin ≤ 57 V	3.3-V output	–	–	2	A
	10.8 V ≤ Vin ≤ 13.2 V		–	–	1.2	
Output ripple voltage, peak-to-peak	Vin = 44 V, I_{LOAD} = 2 A	3.3-V output	–	65	–	mV
Efficiency, end-to-end	Vin = 44 V, I_{LOAD} = 2 A	3.3-V output	–	77%	–	
Switching frequency			225	–	275	kHz

The equations that follow are associated with the schematic diagram in Figure 1. The reference designators in Figure 1 perform a cross-reference function to both the TPS23753EVM-002EVM and the TPS23753 data sheet (SLVS853).
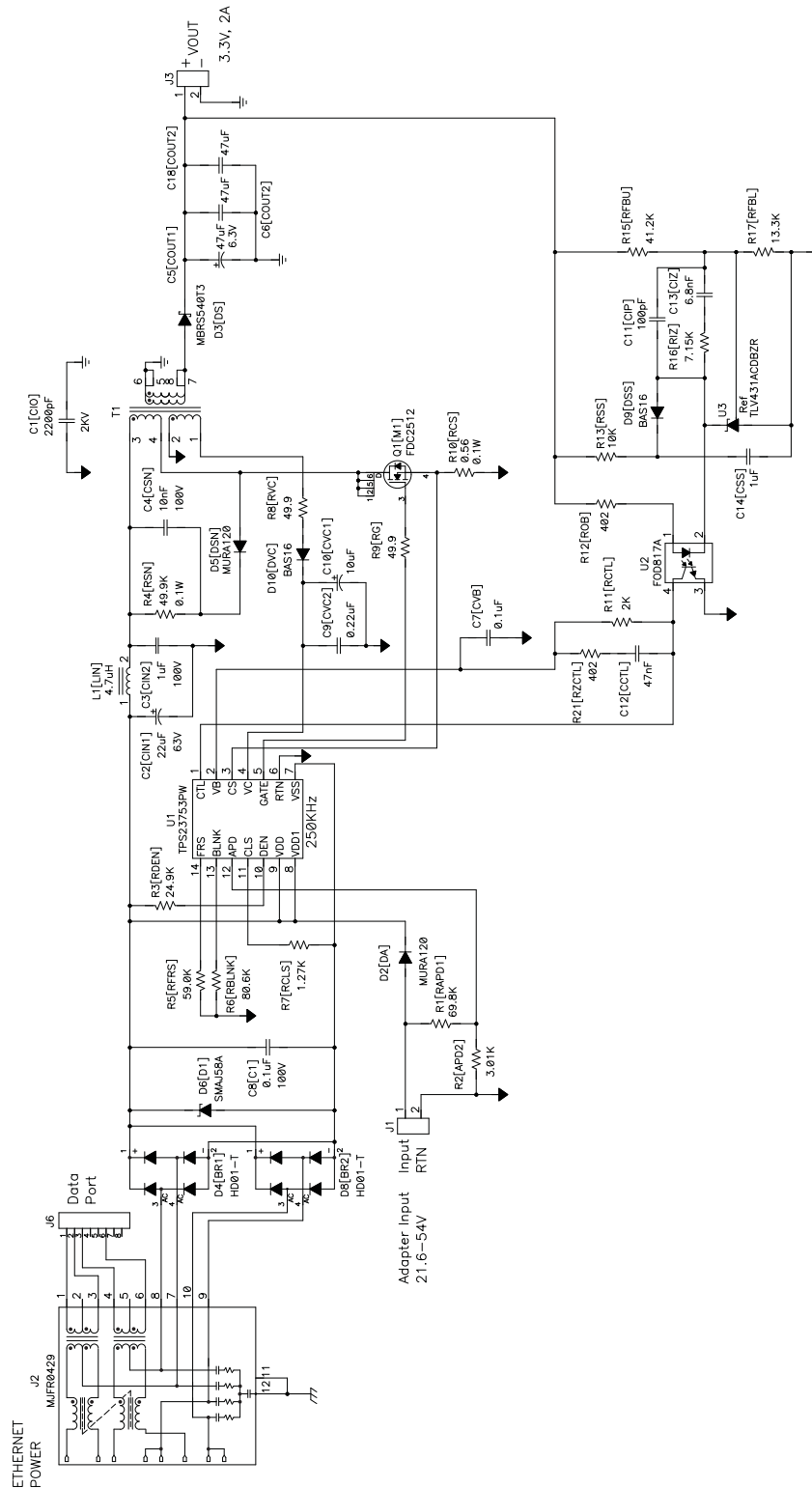

Figure 1. Generic PD and Flyback Converter Circuit Block Diagram

2.1 Powered-Device Controller

2.1.1 TVS, D1

D1 is used to protect the powered-device (PD) controller front-end from overvoltage due to line transients, hotplug into 48-V sources, and output faults. A transient suppressor diode, such as the SMAJ58A, must be connected from V_{DD} to V_{SS}.

2.1.2 Capacitor, C1

The IEEE 802.3-2005 standard specifies a V_{DD}-V_{SS} bypass capacitor whose value is required to be 0.05 µF–1.2 µF. Typically, a 0.1-µF, 100-V, 10% ceramic capacitor is used.

2.1.3 Detection Resistor, R_{DEN}

The IEEE 802.3-2005 standard specifies a detection signature resistance, R_{DEN}, between 23.75 kΩ and 26.25 kΩ.

$$R_{DEN} = \frac{23.75 \text{ k}\Omega + 26.25 \text{ k}\Omega}{2} = 25 \text{ k}\Omega$$

Choose R_{DEN} = 24.9 kΩ, 1%

(1)

2.1.4 Classification Resistor, R_{CLS}

Connect a resistor from CLS to V_{SS} to program the classification current according to the IEEE 802.3-2005 standard. The power assigned must correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to the following table.

CLASS	POWER AT PD PI		CLASS CURRENT		RESISTOR (Ω)	MINIMUM PACKAGE SIZE	NOTES
	MINIMUM (W)	MAXIMUM (W)	MINIMUM (mA)	MAXIMUM (mA)			
0	0.44	12.95	0	4	1270	0402	
1	0.44	3.84	9	12	243	0402	
2	3.84	6.49	17	20	137	0402	
3	6.49	12.95	26	30	90.9	0603	
4	12.95	25.5	36	44	63.4	0603	802.3at only, not allowed for IEEE 802.3-2005

Because this design example is 7 W, either class 0 or class 3 can be chosen. Because the output loading is not fixed, class 0 and R_{CLS} = 1270 Ω is chosen.

2.2 Adapter Input

The adapter configuration shown in Figure 1 bypasses the PD hotswap MOSFET by applying the adapter voltage directly to the TPS23753 converter section (V_{DD1} and RTN). Other adapter O-ring configurations are possible and are discussed in application report SLVA306.

2.2.1 Input Blocking Diode, D_A

D_A should be rated for the reverse voltage required which is typically 80 V–100 V. A Schottky diode rated for the maximum adapter low line input current is preferred to minimize diode power loss. For this example, the MURA120 diode is used (200 V, 1 A, VF = 0.75 V maximum, VF = 0.7 V nominal at 550 mA).

2.2.2 APD Pin Divider Network, R_{APD1}, R_{APD2}

The APD pin can be used to disable the TPS23753 internal hotswap MOSFET giving the adapter source priority over the PoE source. An active APD pin also disables the internal class regulator and CLS pin.

R_{APD1} and R_{APD2} provide ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. The APD divider ratio DR_{APD} must be chosen with consideration given to the APD pin maximum recommended input voltage, class regulator and resistor power dissipation, and adapter disable threshold.

The following example illustrates selection of R_{APD1} and R_{APD2}.

1. To prevent the converter from operating at an excessively low adapter voltage, choose a start-up voltage, V_{START}, approximately 75% of nominal. Assuming that the adapter output is 48 V ± 10%, this provides 15% margin below the minimum adapter operating voltage.

2. Choose $V_{START} = 48 \times 0.75 = 36$ V.

3. Select R_{APD2}, considering power dissipation. Choose $R_{APD2} = 3.01$ kΩ

$$DR_{APD} = \frac{Vin_{MIN}}{V_{APDEN}} = \frac{36 \text{ V}}{1.5 \text{ V}} = 24 \tag{2}$$

$$R_{APD1} = R_{APD2} \times (DR_{APD} - 1) = 3.01 \text{ k}\Omega \times 23 = 69.23 \text{ k}\Omega \tag{3}$$

4. Choose $R_{APD1} = 69.8$ kΩ

5. Check the adapter turnon and turnoff voltage.

$$V_{ADPTR\_ON} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times V_{APDEN} = \frac{72.81 \text{ k}\Omega}{3.01 \text{ k}\Omega} \times 1.5 \text{ V} = 36.3 \text{ V} \tag{4}$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times (V_{APDEN} - V_{APDH}) = \frac{72.81 \text{ k}\Omega}{3.01 \text{ k}\Omega} \times 1.2 \text{ V} = 29 \text{ V} \tag{5}$$

6. Check the APD pin voltage at maximum adapter input.

$$V_{APD} < \frac{Vin_{MAX}}{\left(\dfrac{R_{APD1} + R_{APD2}}{R_{APD2}} \right)} = \frac{48 \times 1.1 \text{ V}}{\left(\dfrac{72.81 \text{ k}\Omega}{3.01 \text{ k}\Omega} \right)} = 2.19 \text{ V} \tag{6}$$

7. V_{APD} is less than V_B, so is within the recommended maximum.

APD turns the class regulator off when the input voltage is above the threshold. When low-voltage adapters are to be used, the APD pin divider can be chosen with class regulator and class resistor power dissipation in mind. With lower APD divider ratios, caution must be exercised to avoid damage to the APD pin if used with a higher voltage adapter.

2.3 Frequency and Blanking

2.3.1 Frequency Setting Resistor, R_{FRS}

For this design, $f_{SW} = 250$ kHz

$$R_{FRS}(k\Omega) = \frac{15000}{f_{SW}(kHz)} = \frac{15000}{250} = 60 \text{ k}\Omega$$

Choose $R_{FRS} = 59$ kΩ

$$\tag{7}$$

2.3.2 Blanking Interval, R_{BLNK}

External blanking can be achieved by installing R_{BLNK}. If the internal blanking interval is sufficient, connect the R_{BLNK} pin to RTN. Choose the blanking interval to be a percentage of the switching period.

$$\frac{BI(\%)}{f_{SW}(kHz)} \times 10^4 (nS) = R_{BLNK}(k\Omega)$$

Choose BI(%) = 2%

$$R_{BLNK}(k\Omega) = \frac{2}{250} \times 10^4 = 80 \text{ k}\Omega$$

Choose $R_{BLNK} = 80.6$ kΩ

$$\tag{8}$$

2.3.3 Internal Control Rail Capacitor, C_{VB}

V_B must be bypassed with a 0.1-µF ceramic capacitor to RTN. V_B is an internal 5-V control rail and must be used to bias the feedback opto-coupler, U2

2.4 Bias Supply

2.4.1 Bias Supply Diode, D_{VC}

D_{VC} can be a small, general-purpose diode. For this example, BAS16 diode is used (75 V, 150 mA).

2.4.2 Bias Supply Resistor, R_{VC}

R_{VC} helps to reduce peak charging from the bias winding. Typical R_{VC} values range from 0 Ω to 100 Ω. Choose R_{VC} = 49.9 Ω.

2.4.3 Bias Supply Capacitance, C_{VC1}, C_{VC2}

V_C must be bypassed with a 0.22-µF minimum ceramic capacitor (C_{VC2}) to RTN. The value of the bulk V_C capacitor (C_{VC1}) affects the converter start-up time as well as shorted output hiccup frequency. C_{VC1} is charged by the internal V_C bootstrap current source as V_C approaches $UVLO_1$. C_{VC1} affects the charge-up time as follows:

$$C_{VC1} = \frac{I_C \times T_{ST}}{UVLO_1}$$

$$I_C \approx 3 - 4 \text{ mA}, T_{ST} \approx 30 \text{ mS}, UVLO_1 = 9 \text{ V}$$

$$C_{VC1} = \frac{0.0035 \times 0.05}{9} = 11.7 \text{ µF}$$

Choose C_{VC1} = 10 µF

(9)

2.5 DC-DC Converter Characteristics

2.5.1 Output

3.3V OutputLoad

$Vout_{NOM}$ = 3.3 V, $Vout_{RIPPLE}$ = 1.5%

$Pout_{MAX}$ = 7W, $Pout_{MIN}$ = 0W

$Iout_{MAX}$ = 2.15A, $Iout_{MIN}$ = 0A

12V Bias

$Vout_{NOM}$ = 12V, $Vout_{RIPPLE}$ = 5%

$Pout_{MAX}$ = 60mW, $Pout_{MIN}$ = 0W

$Iout_{MAX}$ = 5mA, $Iout_{MIN}$ = 0A

(10)

2.5.2 Input

PoE (at PSE Power Interface)

$Vpse_{MAX}$ = 57V, $Vpse_{MIN}$ = 44V

$Ipse_{MAX}$ = 350mA, $Ipse_{MIN}$ = 0A

Adapter (24V)

$Vadp_{NOM}$ = 24 V, $Vadp_{TOL}$ = ±10%

(11)

2.5.3 Efficiency Target

$\eta_{FB} \not= 78\%$

2.5.4 Maximum Adapter Input Current

$$Iadp_{MAX} = \frac{Pout_{MAX}}{Vadp_{MIN} \times \eta_{FB}} = \frac{7W}{21.6V \times 0.78} = 415 \text{ mA}$$

(12)

2.5.5 Minimum Converter Input Voltage

$$Vfb_{MIN} = Vadp_{MIN} - V_{DA} = 21.6V - 0.7V = 20.9V$$

design for $Vflyback_{MIN} = 20V$

$\hspace{13cm}$ (13)

2.5.6 Duty Cycle

The TPS23753 supports duty cycles up to 80%. Choose a maximum operating duty cycle for the converter that includes plenty of margin.

$$Dmax_{DESIGN} \neq 60\%$$

2.6 Flyback Transformer

2.6.1 Primary Voltage Drops

Estimate the primary element voltage drops assuming that the peak primary input current is twice the maximum adapter low line input current.

$$Rds\text{-}on_{M1} + R_{CS} \approx 1\Omega$$

$$Vdrop_{PRIMARY} = 2 \times Iadp_{MAX} \times 1\Omega = 0.831V$$

$\hspace{13cm}$ (14)

2.6.2 Secondary and Bias Winding Voltage Drops

$$Isecondary = \frac{Vflyback_{MIN}}{Vout_{MIN}} \times 2 \times Iadp_{MAX} = \frac{20V}{3.15V} \times 2 \times 0.415A = 5.27A$$

$$Vdrop_{secondary} \approx 0.4V$$

$$V_{DVC} \approx 0.5V$$

$$I_{VC} \approx 5mA$$

$$R_{VC} = 50 \, \Omega$$

$$Vdrop_{BIAS} = V_{DVC} + I_{VC} \times R_{VC} = 0.5V + 0.005 \times 50 = 0.75V$$

$\hspace{13cm}$ (15)

2.6.3 Required Transformer Turns Ratios

The equations yield a maximum turns ratio at $Vflyback_{MIN}$ and $Dmax_{DESIGN}$

$$N_{P\_S} = \frac{Dmax_{DESIGN}}{1 - Dmax_{DESIGN}} \times \frac{Vflyback_{MIN} - Vdrop_{PRIMARY}}{Vout_{NOM} + Vdrop_{SECONDARY}} = 7.77$$

$$N_{P\_B} = \frac{Dmax_{DESIGN}}{1 - Dmax_{DESIGN}} \times \frac{Vflyback_{MIN} - Vdrop_{PRIMARY}}{Vbias_{NOM} + Vdrop_{BIAS}} = 2.26$$

$\hspace{13cm}$ (16)

2.6.4 Target Peak Primary Current

For a continuous conduction mode (CCM) flyback converter, a good rule is to choose the primary ripple current to be < 50% of the peak primary current. Doing this yields the following equation.

$$N_{P\text{-}S} = 7(N_{P\_S} \text{ rounded to integer})$$

$$I_{peak} = \frac{4}{3} \times \left(\frac{Iout_{MAX}}{N_{P\text{-}S}} \times \frac{1}{1 - Dmax_{DESIGN}} \right) = 1.036A$$

$\hspace{13cm}$ (17)

2.6.5 Primary Inductance

The following equation yields a minimum primary inductance required to keep the peak current below that in Equation 17.

$$Lprim = \frac{Dmax_{DESIGN}}{freq_{NOM}} \times \frac{Vflyback_{MIN} - Vdrop_{PRIMARY}}{0.5 \times I_{peak}} = 87.6 \; \mu H$$

$\hspace{13cm}$ (18)

2.6.6 Select the Transformer

Several readily available 7-W choices exist for this PoE transformer. Significant data sheet parameters follow.

Primary Inductance, L_P = 155 μH
Primary-to-secondary turns ratio, N_{PS} = 5.26
Primary-to-bias turns ratio, N_{PB} = 1.5

2.6.7 Actual Duty Cycle at Voltage Using Selected Transformer

$$Dmax_{ACTUAL} = \frac{(Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}}{(Vflyback_{MIN} - Vdrop_{PRIMARY}) + (Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}} = 50.4\%$$

$$Dmin_{ACTUAL} = \frac{(Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}}{(Vflyback_{MAX} - Vdrop_{PRIMARY}) + (Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}} = 25.7\%$$

$$Dmax_{12V} = \frac{(Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}}{(10.1\ V - Vdrop_{PRIMARY}) + (Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS}} = 67.7\%$$

(19)

2.6.8 Calculate Primary Currents

An example of the primary current waveform is shown in Figure 2.
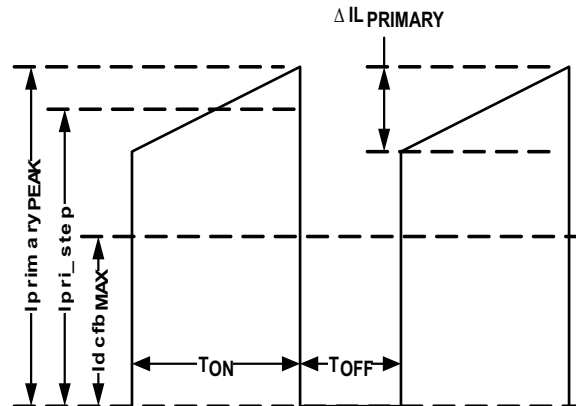
Figure 2. Example Primary Current Waveform

Low line average DC input current:

$$Idcfb_{MAX} = \frac{Pout_{MAX}}{Vflyback_{MIN} \times \eta_{FB}} = 0.45A$$

On-state step current:

$$Ipri\_step = \frac{Idcfb_{MAX}}{Dmax_{ACTUAL}} = 0.89A$$

Ramp current:

$$\Delta IL_{PRIMARY} = \frac{Vflyback_{MIN} - Vdrop_{PRIMARY}}{L_P} \times \frac{Dmax_{ACTUAL}}{freq} = 0.25A$$

Peak current:

$$Iprimary_{PEAK} = Ipri\_step + \frac{\Delta IL_{PRIMARY}}{2} = 1.0A$$

2.7   Power Train

2.7.1   Primary Switching MOSFET, M1

Determine drain-to-source voltage rating. The snubber limits the actual voltage excursion.

Snubber to limit Vleakage to $\approx 25\text{V}$

$$Vds_{PRIMARY} = Vflyback_{MAX} + Vleakage + (Vout_{NOM} + Vdrop_{SECONDARY}) \times N_{PS} \approx 101\text{V}$$

(20)

Choose a MOSFET with a 150-V, drain-to-source rating. A small package device such as SOT-23 is suitable for this power level. Drain current of at least 1.5 A and RDSon of 500 mΩ is sufficient. Choose a MOSFET with a fairly low gate charge (10–20 nC) due to the potentially low operating voltage conditions that may be encountered in a shorted output condition. The TPS23753 can operate down to about 6.5 V; so, this requires that the MOSFET adequately switch on during these conditions.

2.7.2   Current Sense Resistor, R_{CS}

From TPS23753 datasheet, $V_{CSMAX} = 0.55\text{V}$ typical

$$Rcs_{MIN} = \frac{V_{CSMAX}}{Iprimary_{PEAK}} = 0.55\Omega$$

Choose $R_{CS}0 = 0.56\Omega$, 0.25W

(21)

2.7.3   Snubber, R_{SN} , C_{SN}, D_{SN}

Without a snubber, the stored energy in the leakage inductance rings with the transformer interwinding (C_{WDG}) and MOSFET output capacitance (C_{OSS_M1}) at MOSFET turnoff. The transformer leakage inductance, L_{LKG}, may be 2%-3% of the primary inductance and the MOSFET and transformer winding capacitance can be several hundred picofarads.

$$Vspike = Iprimary_{PEAK} \times \sqrt{\frac{L_{LKG}}{C_{WDG} + C_{OSS\_M1}}} = 1.0\text{A} \times \sqrt{\frac{4\ \mu\text{H}}{200\ \text{pF}}} = 141\text{V}$$

We need $Vspike_{NEW} \approx 25\text{V}$ so C_{SN} should be $\approx \left(\dfrac{Vspike}{Vspike_{NEW}}\right)^2 \times \left(C_{WDG} + C_{OSS\_M1}\right) = 6\text{nF}$

Choose $C_{SN} = 10\text{nF}$

(22)

Choose R_{SN} so that the snubber time constant is much larger (say 200x) than the switching period. Choose D_{SN} for the input filter; L_{IN}, C_{IN1}, C_{IN2} required reverse voltage and leakage inductance charging current.

$$R_{SN} \approx \frac{200}{freq \times C_{SN}} = 80\ \text{k}\Omega$$

(23)

Alternatively, an RC snubber from the primary FET drain to RTN can be employed to limit the spike and slow down the turnoff rise time. This may be preferred for an application where reduced conducted emissions are required. The RC combination should be chosen to minimize the effect on efficiency while reducing the spike to an acceptable safe level. Typical values are 80 Ω, 1/2 W, 330 pF, and 200 V for this application.

2.7.4   Input filter; L_{IN}, C_{IN1}, C_{IN2}

The input capacitance (C_{IN1} and C_{IN2}) must furnish the transient switching current. An inductor, L_{IN}, provides another layer of filtering and reduces the requirements on C_{IN2}. C_{IN1} provides bulk filtering, whereas C_{IN2} provides switching energy absorption.

Target input ripple voltage, $Vin_{RIPPLE} \approx 1V$

$$Cin_{MIN} = \frac{(Ipri\_step - Idcfb_{MAX}) \times Dmax_{ACTUAL}}{freq \times Vin_{RIPPLE}} = 0.89 \; \mu F$$

Choose C_{IN2} = 1µF, X7R ceramic, 100V, 10mΩ ESR at 100 + kHz

2ARMS ripple current rating

$$\Delta Vin_{CIN2} = \frac{(Ipri\_step - Idcfb_{MAX}) \times Dmax_{ACTUAL}}{freq \times C_{IN2}} + Ipri\_step \times ESR_{CIN2} = 0.9V$$

(24)

Select a common-type aluminum electrolytic capacitor for C_{IN1}, and then size the inductor to achieve the additional attenuation of the ripple voltage.

Choose C1 = 22 µF, aluminum electrolytic, 100V, 1.3Ω ESR at 100 kHz,

130 mA RMS ripple current rating.

Target $\Delta I_{CIN1} < 0.13A$ so $\Delta V_{CIN1} = \Delta I_{CIN1} \times ESR_{CIN1} = 170mV$

$$L_{IN} \approx \frac{\Delta V_{CIN1} + \Delta V_{CIN2}}{Ipri\_step - Idcfb_{MAX} - \Delta I_{CIN1}} \times \frac{Dmax_{ACTUAL}}{freq} = 5.5 \; \mu H$$

(25)

Choose a 4.7-µH, 1.5 A_{RMS}, 90-mΩ inductor.

2.7.5 Calculate Secondary Currents

An example of the secondary current waveform is shown in Figure 3.
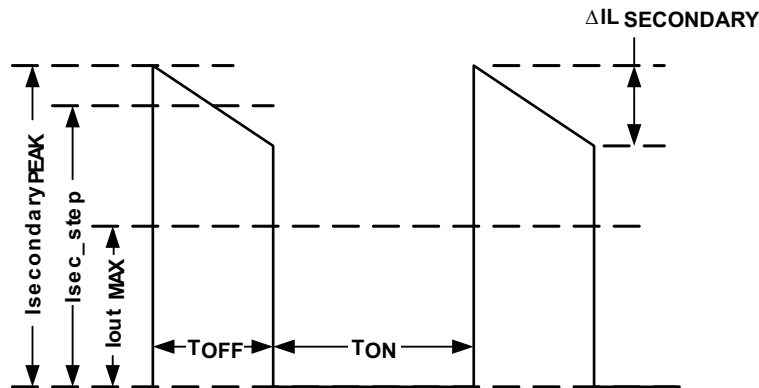
Figure 3. Example Secondary Current Waveform

Off-state step current:

$$\text{Isec\_step} = \frac{\text{Iout}_{\text{MAX}}}{1 - \text{Dmax}_{\text{ACTUAL}}} = 4.34A$$

Ramp current:

$$\Delta IL_{\text{SECONDARY}} = 2 \times (N_{\text{PS}} \times \text{Iprimary}_{\text{PEAK}} - \text{Isec\_step}) = 2.00A$$

Peak current:

$$\text{Isecondary}_{\text{PEAK}} = N_{\text{PS}} \times \text{Iprimary}_{\text{PEAK}} = 5.34A$$

2.7.6 Output Filter; C_{OUT1}, C_{OUT2}

The output capacitance (C_{OUT1} and C_{OUT2}) must furnish the transient load current. C_{OUT1} provides bulk filtering, whereas C_{OUT2} provides switching energy absorption.

Target output ripple voltage, $\text{Vout}_{\text{RIPPLE}} \approx 50mV$

$$\text{Cout}_{\text{MIN}} = \frac{(\text{Isec\_step} - \text{Iout}_{\text{MAX}}) \times (1 - \text{Dmax}_{\text{ACTUAL}})}{\text{freq} \times \text{Vout}_{\text{RIPPLE}}} = 90.4 \ \mu F$$

Choose C_{OUT2} = 2x47µF, X5R ceramics, 6.3V, 2mΩ ESR at 100+kHz

(26)

4ARMS ripple current rating

$$\Delta \text{Vout}_{\text{COUT2}} = \frac{(\text{Isec\_step} - \text{Iout}_{\text{MAX}}) \times (1 - \text{Dmax}_{\text{ACTUAL}})}{\text{freq} \times C_{\text{OUT2}}} + (\text{Isec\_step} - \text{Iout}_{\text{MAX}}) \times \text{ESR}_{\text{COUT2}} = 51 \ mV$$

(27)

Add C_{OUT1} = 47 µF, aluminum electrolytic, 6.3-V, 1.25-Ω ESR at 100-kHz, 90-mA RMS ripple current rating.

The low-ESR ceramics effectively shunt the ESR of the aluminum electrolytic. The additional ripple attenuation due to the aluminum electrolytic is minimal due to the larger ESR.

2.7.7 Output Rectifier; D_S

The output rectifier diode must provide low forward voltage drop at the secondary peak current. Consideration must also be given to a safe operating area during output overload conditions. For this case, the converter goes to a constant output power condition with low-primary and high-secondary duty cycle. D_S must withstand these conditions reliably. Choose D_S to be a MBRS540T3 in a SMC package (40-V reverse voltage, 5-A continuous current max, Vf = 0.5 V max at 5 A).

2.7.8 Thermal Considerations

Consideration must be given to the power dissipation in M1, R_{CS}, and D_S. Both conduction and switching losses must be considered.

2.8 Feedback Control

2.8.1 Shunt Regulator, U3

For this 3.3-V application, a low-voltage reference shunt regulator is required. Choose the TLV431A with a 1.24-V, 1% internal reference.

2.8.2 Output Voltage Setpoint Resistors: R_{FBU}, R_{FBL}

Choose R_{FBU} based on expected integrator midband gain and zero location. Estimate the integrator zero location to be approximately 1 kHz, integrator zero capacitors are from 1 nF–10 nF, and low integrator gain.

$$R_{IZE} \approx \frac{1}{2 \times \pi \times 4.7nF \times 1kHz} = 33.9k\Omega$$

$$R_{FBUE} \approx R_{IZE}$$

Choose R_{FBU} = 41.2 kΩ

Vref = 1.24V (28)

$$R_{FBL} = \frac{Vref \times R_{FBU}}{Vout_{NOM} - Vref} = 24.8 \text{ k}\Omega$$

Choose R_{FBL} = 24.3 kΩ (29)

Choosing R_{FBL} a little smaller than calculated ensures an output voltage a bit higher than nominal to compensate for the DC drops from the power supply to the load.

2.8.3 Opto-Isolator, U2 Biasing

Choose the opto-isolator to provide a fairly low but stable current transfer ratio characteristic when the LED is driven with a 1- to 2-mA current bias. Typical parameters for an opto-isolator of this sort are:

CTR_{5mA} = 80−160%,

$CTR_{2mA} = 0.7 \times CTR_{5mA} \approx 0.85$ from device data sheet curves

$Vled_{OPTO} \approx 1.1V$ at $Iled_{OPTO}$ = 2mA (30)

2.8.4 Opto-Isolator LED Bias Current

Start with bias at zero duty cycle (ZDC)

$Vled_{OPTO-K}$ = Vref + 150mV

$$R_{OB} = \frac{Vout_{NOM} - Vled_{OPTO} - Vled_{OPTO-K}}{Iled_{OPTO}} = 405\Omega$$

Choose R_{OB} = 402Ω (31)

2.8.5 Opto-Isolator Transistor Bias Current

Start with bias at zero duty cycle (ZDC)

TPS23753 $Vzdc_{MAX}$ = 1.7V

TPS23753 Vcs_{MAX} = 0.55V, V_B = 5V

$Vctl_{MAX} = Vzdc_{MAX} + 2 \times Vcs_{MAX}$

$$Vctl_{NOM} = \frac{Vzdc_{MAX} + Vctl_{MAX}}{2} = 2.25V$$

$$R_{CTL} = \frac{Vb - Vzdc_{MAX}}{Iled_{OPTO} \times CTR_{2mA}} = 1.94k\Omega$$

Choose R_{CTL} = 2 kΩ (32)

2.8.6 Secondary Side Soft Start

Place an RC network on the shunt regulator output for soft start. Typical values are R_{SS} = 10 kΩ and C_{SS} = 0.1 μF. A blocking diode, D_{SS}, isolates the outer loop from R_{SS} and C_{SS}.

2.9 Frequency Characteristics

2.9.1 Modulator-Power Stage (MPS) Gain and Right-Half Plane Zero (RHPZ)

The MPS gain, K_{MPS} is the ratio of modulator output current to CS pin voltage, V_{CS}. K_{MPS} and RHPZ are derived below in Equation 33.

$$\text{Gain, } K_{MPS} = \frac{(1 - Dmax_{ACTUAL}) \times N_{PS}}{R_{CS}} = 4.66 \frac{A}{V}$$

$$Rload = \frac{Vout_{NOM}^2}{Pout_{MAX}} = 1.56\Omega$$

Current mode control yields right half plane zero, RHPZ

$$RHPZ = Rload \times \frac{[N_{PS}(1 - Dmax_{ACTUAL})]^2}{2 \times \pi \times Dmax_{ACTUAL} \times L_P} = 21.6 \text{ kHz}$$

(33)

2.9.2 MPS Current

The MPS current, $I_{MPS}(\omega)$, is the product of K_{MPS} and RHPZ.

$$\omega_{RHPZ} = 2 \times \pi \times RHPZ$$

$$I_{MPS}(\omega) = K_{MPS} \times (1 - \frac{j\omega}{\omega_{RHPZ}})$$

(34)

2.9.3 Output Filter (Plus Load) Frequency Characteristics

The output impedance is simply the parallel combination of the output capacitors (including each capacitor's equivalent series resistance or ESR) and the load.

$$Zout(\omega) = Z_{COUT1}(\omega)||Z_{COUT2}(\omega)||Rload$$

(35)

2.9.4 MPS Plus Filter and Load (MPF) Transfer Function

The MPF transfer function is shown in Equation 36

$$\omega_{RHPZ} = 2 \times \pi \times RHPZ$$

$$MPF(\omega) = I_{MPS}(\omega) \times Zout(\omega)$$

(36)

2.10 Loop Compensation

The following discussion relies on the use of a mathematics program like MathCAD™ or Excel™ to perform the calculations. Some iteration is involved, but the end results are close to actual performance.

2.10.1 Choose Desired Loop Crossover Frequency, F0 = 5.5 kHz

The inner control loop consists of the opto-isolator and associated components. The outer control loop consists of the integrator. It can be shown that the overall transfer function from V_{OUT} to V_{CTL} is:

$-OPTO(\omega) \times [INT(\omega) + 1]$

where $OPTO(\omega)$ is the opto-isolator transfer function and $INT(\omega)$ is the integrator transfer function

2.10.2 Overall Transfer Function

$FB(\omega) = - MPF(\omega) \times OPTO(\omega) \times (INT(\omega)+1)$

where $FB(\omega)$ is the flyback overall transfer function.

Simplified $OPTO_S(\omega) = \dfrac{R_{CTL}}{R_{OB}} \times CTR_{2mA} \times \dfrac{1}{1+j\omega \times R_{CTL} \times C_{CTL}} \times \dfrac{1}{K_{CTL}}$

TPS23753 internal CTL divider, $K_{CTL} = 2$

Simplified $INT_S(\omega) = \dfrac{1}{j\omega \times R_{FBU} \times C_{IZ}}$

Modulator/opto transfer function, $G_{MO}(\omega) = - MPF(\omega) \times OPTO_S(\omega)$

$$|G_{MO}(2 \times \pi \times F_0)| = |MPF(2 \times \pi \times F_0)| \times |OPTO_S(\omega)| \tag{37}$$

2.10.3 Compensate Opto-Isolator or Inner Loop

Select C_{CTL} to achieve a gain sufficiently below unity at the crossover frequency. Start by assuming the simple integrator $INT_S(\omega)$ with no midband gain ($R_{IZ} = 0$). Target an initial $|G_{MO}(2 \times \pi \times F_0)| > 0.5$–$0.8$ to estimate C_{CTL}. C_{CTL} must be limited to 47 nF or less.

Choose $|G_{MO}(2 \times \pi \times F_0)| = 0.75$

$$C_{CTL} = \dfrac{\sqrt{1 - \left[\dfrac{R_{CTL}}{R_{OB}} \times \dfrac{CTR_{2mA}}{K_{CTL}} \times \dfrac{|MPF(2 \times \pi \times F_0)|}{G_{MO}}\right]^2}}{2 \times \pi \times F_0 \times R_{CTL}} = 50.3nF$$

Choose $C_{CTL} = 47nF$

$$\tag{38}$$

2.10.4 Inner Loop Control Zero Resistor, R_{ZCTL}

For lower output power and voltage designs, a resistor in series with C_{CTL} can provide phase boost for stability. Target $R_{ZCTL} \sim R_{CTL} /10$).

Choose $R_{ZCTL} = 249\ \Omega$

2.10.5 Inner Loop Transfer Function

$$OPTO(\omega) = \dfrac{R_{CTL}}{R_{OB}} \times CTR_{2mA} \times \dfrac{1+j\omega \times R_{ZCTL} \times C_{CTL}}{1+j\omega \times (R_{CTL} + R_{ZCTL}) \times C_{CTL}} \times \dfrac{1}{K_{CTL}} \tag{39}$$

2.10.6 Outer Loop Compensation

Now that the inner loop is first-pass compensated, design an integrator with midband gain to yield the desired crossover. First calculate the new G_{MO} including R_{ZCTL}.

$$|G_{MO}(2 \times \pi \times F_0)| = |MPF(2 \times \pi \times F_0)| \times |OPTO_S(2 \times \pi \times F_0)| = 0.772 \tag{40}$$

Solve for the integrator midband gain (R_{IZ}/R_{FBU}), which causes the overall transfer function to be unity at F_0.

$INT_{MB} = \dfrac{R_{IZ}}{R_{FBU}}$

$|G_{MO}(2 \times \pi \times F_0)| \times (INT_{MB}+1) = 1$

$INT_{MB} = \dfrac{R_{IZ}}{R_{FBU}} = \dfrac{1}{|G_{MO}(2 \times \pi \times F_0)|} - 1$

$R_{IZ} = R_{FBU} \times \left[\dfrac{1}{|G_{MO}(2 \times \pi \times F_0)|} - 1\right] = 12.16\ k\Omega$

Choose $R_{IZ} = 12.1\ k\Omega$

$$\tag{41}$$

Select the integrator zero capacitor, C_{IZ}, by choosing an integrator zero 4 to 5 times below F_0. Note that once the bode plot is mathematically generated, some shaping of the response curves can be performed to optimize the desired response.

$$C_{IZ} = \frac{5}{2 \times \pi \times R_{IZ} \times F_0} = 11.9 \text{ nF}$$

(42)

Select the integrator pole capacitor, C_{IP}, by choosing an integrator zero 10 times above F_0.

$$C_{IP} = \frac{1}{20 \times \pi \times R_{IZ} \times F_0} = 240 \text{ pF}$$

Choose $C_{IP} = 100\text{pF}$

(43)

2.10.7 Integrator Transfer Function

$$INT(\omega) = \frac{R_{IZ}}{R_{FBU}} \times \frac{1 + \frac{1}{j\omega \times R_{IZ} \times C_{IZ}}}{1 + j\omega \times R_{IZ} \times C_{IP}}$$

(44)

2.10.8 Stability Check

For loop-stability analysis, break the feedback loop between the output load and the input to the shunt regulator feedback network and inject a noise source. The shunt regulator/integrator shifts phase by 270 degrees (180 due to inversion and 90 due to integrator). So, the output load phase leads the input phase by 90 degrees. Instability occurs as the phase difference approaches 0 degrees (or in-phase input and output signals).

From Mathcad, $FB(2 \times \pi \times F_0) = 0.790 + 0.612i$

$$\text{Phase} = \tan^{-1}\left(\frac{0.612}{0.790}\right) = 37.8° \text{ or Phase} = \arg(FB(2 \times \pi \times F_0)) \times \frac{180}{\pi}$$

$$20 \times \log(|FB(2 \times \pi \times F_0)|) = -0.1 \text{ dB}$$

(45)

The phase margin is inadequate. Increase R_{ZCTL}, then recompute R_{IZ}.

Choose new $R_{ZCTL} = 402\Omega$

New $|G_{MO}(2 \times \pi \times F_0)| = 0.804$

New $R_{IZ} = R_{FBU} \times \left[\frac{1}{|G_{MO}(2 \times \pi \times F_0)|} - 1\right] = 10 \text{ k}\Omega$

Choose $R_{IZ} = 7.15\text{k}\Omega$

(46)

Recompute the new phase margin.

From Mathcad, $FB(2 \times \pi \times F_0) = 0.609 + 0.719i$

$$\text{Phase} = \tan^{-1}\left(\frac{0.719}{0.609}\right) = 49.8°$$

$$20 \times \log(|FB(2 \times \pi \times F_0)|) = -0.5 \text{ dB}$$

(47)

The new phase margin is now acceptable.

The modeled bode plot is shown in Figure 4 and the modeled crossover is at 5.3 kHz with phase margin of 50 degrees. Figure 5 and Figure 6 show the circuit response using a network analyzer. The actual results correlate closely with the modeled results.

Gain and Phase
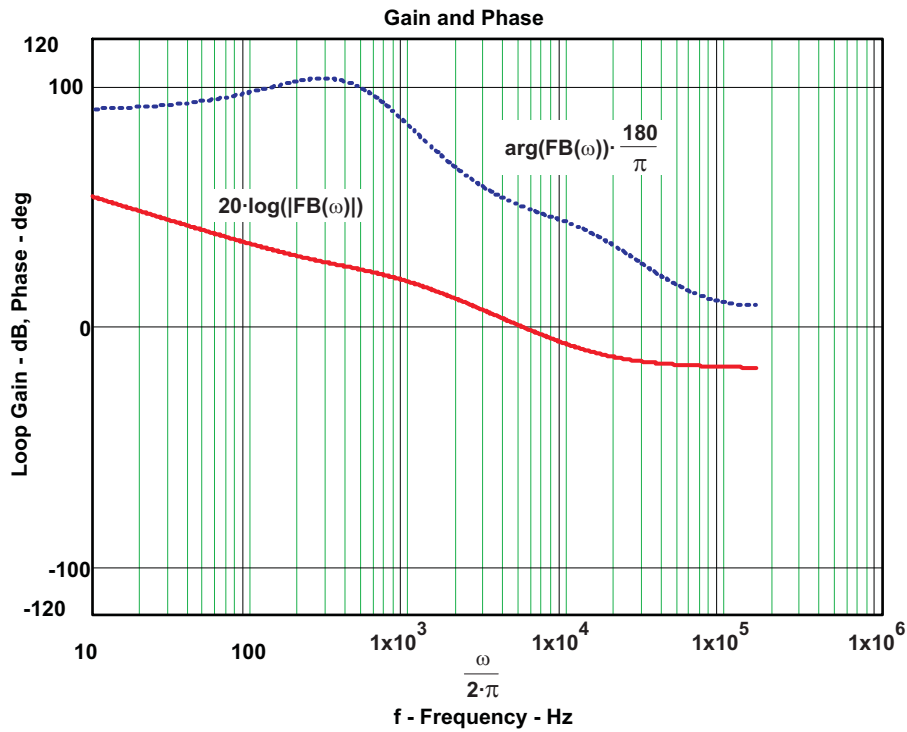
Figure 4. Mathcad Bode Plot (Minimum Input/2-A Output)
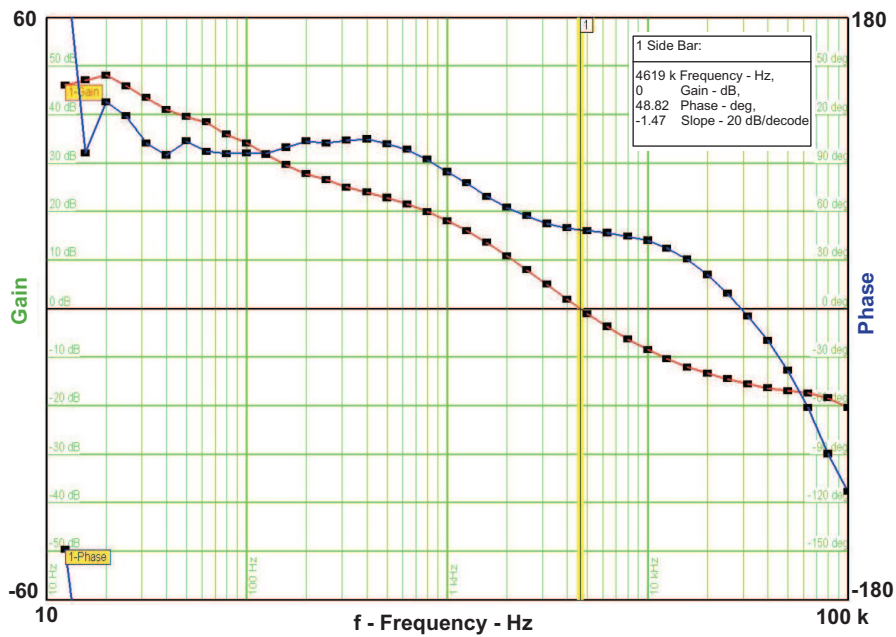
Figure 5. TPS23753EVM-002 Network Analyzer Plot (24-V Input/2-A Output)
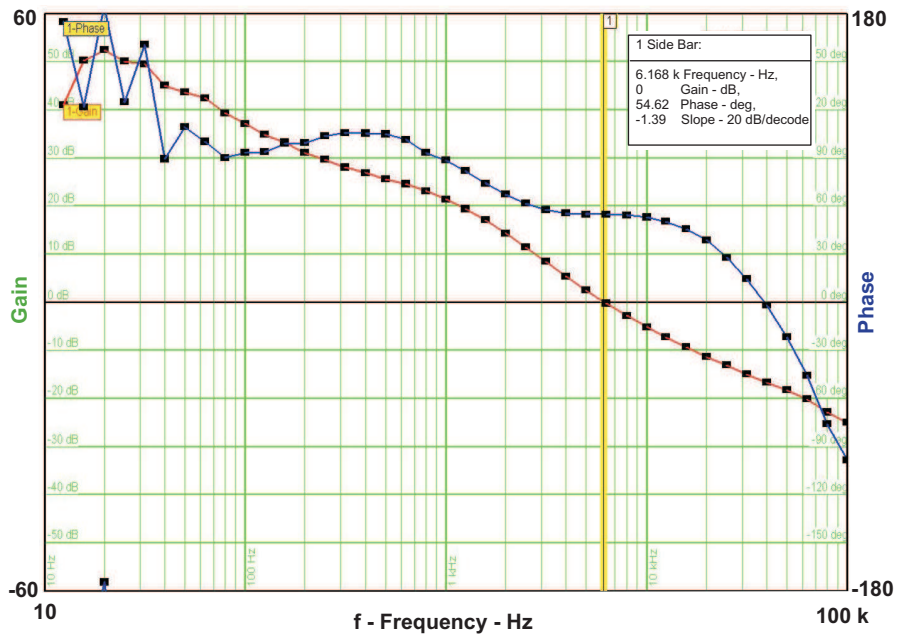
Figure 6. TPS23753EVM-002 Network Analyzer Plot (48-V Input/2.2-A Output)

3   PCB Layout Guidelines

The layout of the PoE front end must follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1-µF capacitor, and TPS23753 converter input bulk capacitor.
- All leads must be as short as possible with wide power traces and paired signal and return.
- Signals must not cross over one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS23753 must be located over split, local ground planes referenced to VSS for the PoE input and to RTN for the converter. Whereas the PoE side may operate without a ground plane, the converter side must have one. Logic ground and power layers must not be present under the Ethernet input or the converter primary side.

The DC/DC converter layout can benefit from basic rules such as:

- Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses which include the power semiconductors and magnetics.
- Minimize trace length of high current, power semiconductors, and magnetic components.
- Where possible, use vertical signal pairing.
- Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
- Pay special attention to spacing around the high-voltage sections of the converter.

4   PCB EMI Control

Refer to *Designing an EMI Compliant PoE With Isolated Flyback* UNPUBLISHED application report (SLUA469) for detailed EMI recommendations. A short list of recommendations follows.

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives).
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods).
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup).
- Hide copper associated with switching nodes under shielded magnetics where possible.
- Heat sink the "quiet side" of components instead of the "switching side" where possible (like the output side of inductor).
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground)
- Use LC filter at DC/DC input to suppress high-frequency ringing on the switching nodes.
- Control rise times with gate drive resistors and drain snubbers.
- Use an EMI bridge capacitor across isolation boundary (isolated topologies).
- Observe the polarity dot on inductors (embed noisy end).
- Use common-mode inductors or ferrite beads in a common-mode filter fashion on the input.
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line).
- Balance efficiency vs acceptable noise margin.
- Consider the end-product enclosure and shielding with respect to input signal routing and filtering.

5   Conclusion

This application report outlines the steps to design a simple flyback converter using the TPS23753. The design procedure outlined along with the included layout guidelines allows easy and accurate circuit design using the TPS23753.

6   References

1. *TPS23753, IEEE 802.3-2005 PoE Interface and Isolated Converter Controller* data sheet (SLVS853)
2. *TPS23753EVM-001 Evaluation Module for TPS23753 User's Guide* (SLVU246)
3. *Compensating the (often missed) Inner and Outer Control Loops using the TL431* by Robert Kollman and John Betten. Power Electronic Technology Conference, Power Systems World 2002, Chicago
4. *Practical Guidelines to Designing an EMI Compliant PoE Powered Device with Non-Isolated DC/DC* application report (SLUA454)
5. *Designing an EMI Compliant PoE Powered Device with Isolated Flyback* application report (SLUA469)