

# Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator

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## ABSTRACT

This application report demonstrates a unique method of generating a positive and negative output power supply using a standard buck regulator – one that maintains good regulation, has excellent cross regulation, and can regulate the positive output from a lower input voltage (i.e., boost). The popular method of creating positive and negative voltages from a buck power supply using a coupled inductor or “over-winding” has the disadvantage of needing a minimum load current to have a reasonably regulated auxiliary output [1] - [4].

This document outlines a step-by-step method for designing the split rail power supply. The split rail power supply uses a wide input voltage step-down regulator as an inverting power supply to create the negative supply rail. The positive supply rail is created from a standard, off-the-shelf coupled inductor from Coilcraft [5]. This document builds on the procedure outlined in the *Creating an Inverting Power Supply from a Step-Down Regulator* application note calculator tool [6].

The design procedure is written so that the guide is applicable to designing a split-rail power supply with symmetrical loads. The procedure is also applicable to other step-down, peak-current-mode control regulators and must be used with the *Creating a Split Rail Power Supply from a Step-Down Regulator*, application note calculator tool [7].

Because the negative output of the split-rail power supply is the device ground, the feedback resistors can be connected across both the positive and negative outputs (see [Figure 1](#)). The design example uses the TPS54160A regulator to demonstrate the design procedure. The TPS54160A is a 1.5-A switching regulator that has a wide switching frequency range of 300 kHz to 2500 kHz and an input operating voltage of 3.5 V to 60 V. For higher power designs, devices with a higher current limit can be used, such as the TPS54360.

The power supply was designed using the specifications shown in [Table 1](#).

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## 1 Key Design Guidelines

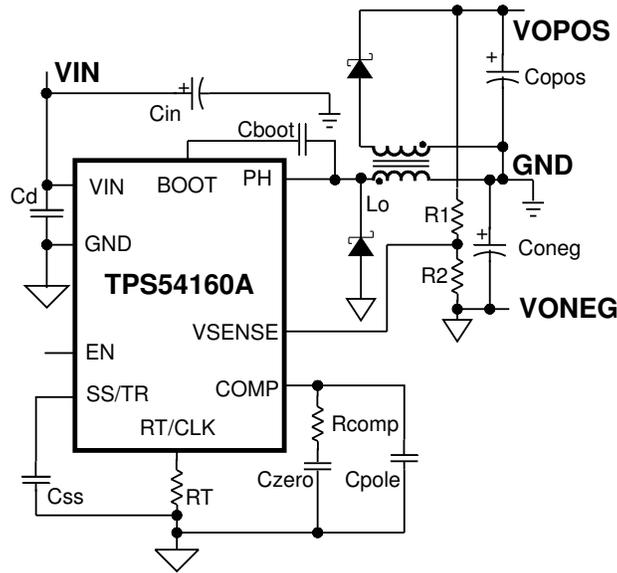


Figure 1. Split-Rail Power Supply Schematic Using the Inverting Method

Table 1. Split-Rail Power Supply Requirement.

Input Voltage, Vin	24 V nominal, 18 V to 30 V
Input Voltage Ripple	<1%
Output Voltage, Vopos	+12 V
Output Voltage Ripple, dVrpos	<0.5%
Output Voltage, Voneg	-12 V
Output Voltage Ripple, dVrneg	<0.5%
Positive Output Current, Iopos	0.3 A
Negative Output Current, Ioneg	0.3 A
Switching Frequency, fsw	300 kHz

### 1.1 Output Voltage

The difference in the maximum input voltage,  $V_{inmax}$ , and the output voltage,  $V_{oneg}$  must not exceed the maximum operating device voltage of the regulator. For the TPS54160A, the maximum operating device voltage,  $V_{devmax}$ , is 60 V.

$$V_{in\ max} \leq V_{devmax} + V_{oneg} \quad (1)$$

$$R1 = R2 \times \left( \frac{V_{opos} - V_{oneg}}{V_{ref}} - 1 \right) \quad (2)$$

Assuming  $V_{oneg}$  is -12 V and using Equation 1, the maximum input voltage for the power supply can be as high as 48 V, easily supporting the 30-V maximum input requirement in the table. Use Equation 2 to determine R1 for the output desired voltage, set R2 equal to 1 kΩ, and  $V_{ref}$  to 0.8 V for the TPS54160A. R1 is equal 29 kΩ. A 29.4 kΩ is used to regulate to slightly below and above -12 V and +12 V.

### 1.2 Input Voltage Range

The operating input voltage,  $V_{inmin}$  of the power supply must be greater than the minimum device voltage,  $V_{devmin}$ . For the TPS54160A, the  $V_{devmin}$  is 3.5 V. The minimum input voltage requirement for the power supply is 18 V, thus, satisfying Equation 3.

$$V_{inmin} \geq V_{devmin} \quad (3)$$

### 1.3 Duty Cycle

The ideal duty cycle for the inverting power supply is shown in the [Equation 4](#), neglecting the losses of the power switching, inductor, and diode drop. The output voltage,  $V_{out}$ , is negative and the input voltage,  $V_{in}$ , is positive yielding a positive result for [Equation 4](#).

$$D = \frac{-V_{oneg}}{V_{in} - V_{oneg}} \quad (4)$$

The maximum duty cycle,  $D_{max}$ , can be calculated by using the minimum input voltage,  $V_{inmin}$ , which is substituted for input voltage,  $V_{in}$ , in [Equation 4](#). Assuming 18 V for  $V_{in}$  and a  $V_{oneg}$  of -12 V, the maximum duty cycle,  $D_{max}$ , is 0.40.

### 1.4 Output Current

To estimate whether the selected switching regulator will be capable of delivering the desired output current, use [Equation 5](#). The designer must know the device's minimum current limit,  $I_{CLmin}$ , maximum duty cycle,  $D_{max}$ , and use a 25% rule of thumb to estimate the inductor ripple current value,  $I_{Lripple}$ .

$$I_{opos\ max} + I_{oneg\ max} \leq (I_{CL\ min} - \frac{I_{Lripple}}{2}) \times (1 - D_{max}) \quad (5)$$

Assuming the minimum current limit is 1.8 A and the  $I_{Lripple}$  is 25% of the minimum current limit, the maximum output current ( $I_{opos} + I_{oneg}$ ) that can be supported by the TPS54160A is estimated to be 0.945 A.

Because the input voltage range and maximum output current is supported by the selected regulator, the next steps are to calculate the inductor value, switching frequency, and output capacitor value.

The maximum switching frequency must be calculated using the minimum controllable on-time, maximum input voltage, and some of the losses in the supply. If the maximum frequency calculated is greater than the 2500 kHz supported by the TPS54160A, limit the  $f_{skipmax}$  to 2500 kHz.

$$f_{skip\ max} \leq \frac{(-V_{oneg} + R_{dc} \times (I_{opos} + I_{oneg}) + V_{fd})}{t_{on\ min} \times (V_{in\ max} - R_{hs} \times (I_{opos} + I_{oneg}) + V_{fd} - V_{oneg})} \quad (6)$$

A consideration specifically for the TPS54160A device is the frequency shift that occurs to prevent overcurrent runaway during an output short circuit.

$$f_{shift\ max} \leq \frac{f_{div}}{t_{on\ min}} \times \frac{(-V_{onegsc} + R_{dc} \times (I_{opos} + I_{oneg}) + V_{fd})}{(V_{in\ max} - R_{hs} \times (I_{opos} + I_{oneg}) + V_{fd} - V_{onegsc})} \quad (7)$$

The maximum switching frequency is the lower frequency of  $f_{shiftmax}$  or  $f_{skipmax}$ . The  $V_{onegsc}$  term in [Equation 7](#) is the output voltage during the output fault. The  $f_{div}$  is the frequency division.  $F_{div}$  is 8 when  $V_{outsc}$  is less than 25% of the regulation voltage. See the *Selecting the Switching Frequency* section of TPS54160A data sheet ([SLVS795](#)) for more details on the frequency shift. The minimum on-time,  $t_{onmin}$ , is 130 ns, and the maximum MOSFET on resistance,  $R_{hs}$ , is 400 m $\Omega$  for the TPS54160A. Assuming diode voltage drop,  $V_{fd}$ , is 0.5 V, inductor resistance,  $R_{dc}$ , is 0.476  $\Omega$ , the maximum frequency calculated is 2327 kHz and 1598 kHz, using [Equation 6](#) and [Equation 7](#), respectively. The maximum switching frequency selected must not be greater than 1598 kHz. Because the power supply specification requirement for the switching frequency is 300 kHz and is lower than the 1598 kHz, no design changes are necessary.

### 1.5 Coupled Inductor

To determine the inductor value, it is necessary to calculate the switch current,  $I_{swavg}$ , at the maximum output current ( $I_{opos} + I_{oneg}$ ) and maximum input voltage.

Use the maximum input voltage as a variable in [Equation 4](#) to calculate minimum duty cycle,  $D_{min}$ . Assuming  $V_{inmax}$  is 30 V,  $D_{min}$  is approximately 0.286 and  $I_{swavg}$  is 0.84 A from [Equation 8](#).

The inductor value is calculated, [Equation 9](#), using a ripple current that is 25% of the average switch current. Using the  $D_{min}$  to calculate the minimum inductance value gives the largest inductance. Assuming  $V_{inmax}$  of 30 V,  $I_{opos}$  of 0.3 A,  $I_{oneg}$  of 0.3 A and a  $f_{sw}$  of 300 kHz, the  $L_o$  is calculated as 136  $\mu$ H.

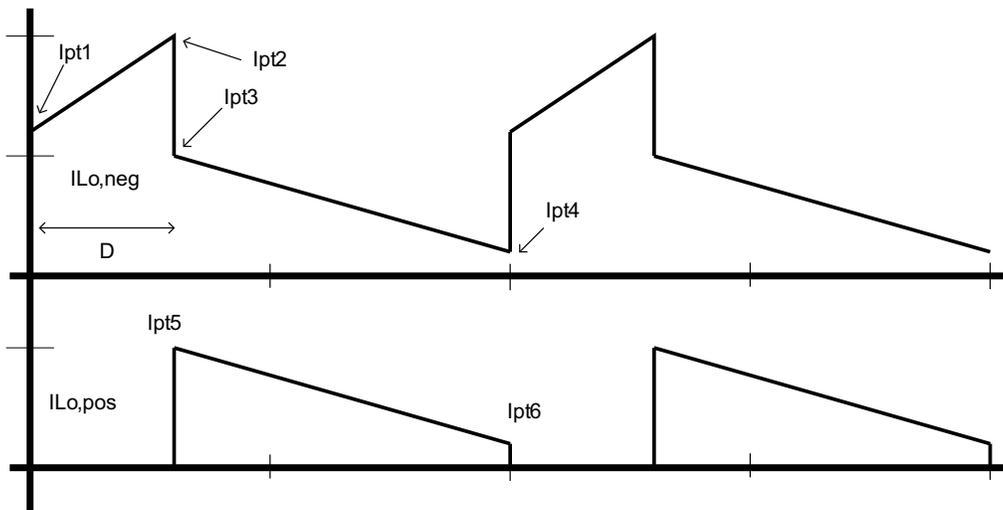
The nearest standard inductance of 150  $\mu\text{H}$  is used for the coupled inductor. The inductor saturation current must be greater than the 1.08 A of peak current calculated in Equation 11.

The MSD1260-154ML inductor from Coilcraft is selected for the coupled inductor.

The saturation current is 1.82 A and the rms current rating is 0.82 A when using both windings. Coilcraft offers many other off-the-shelf coupled inductors in a variety of standard values, saturation currents, and sizes, e.g., MSD1278, MSD7243, LPD3015, and LPD4012.

$$I_{\text{swavg}} = \frac{I_{\text{opos}} + I_{\text{oneg}}}{1 - D_{\text{min}}} \quad (8)$$

$$L_o \geq \frac{V_{\text{inmax}} \times D_{\text{min}}}{f_{\text{sw}} \times I_{\text{swavg}} \times 0.25} \quad (9)$$



**Figure 2. Current in  $L_o$  Primary and Secondary**

Figure 2 shows the primary ( $I_{L_o,\text{neg}}$ ) and secondary ( $I_{L_o,\text{pos}}$ ) currents in the coupled inductor during continuous conduction mode (CCM) when assuming an ideal coupling coefficient and is used to calculate the rms current.

To estimate the rms current for the inductor, calculate  $I_{\text{pt1}}$  to  $I_{\text{pt6}}$  using Equation 10 to Equation 15, and substitute into and solve Equation 16 and Equation 17.

$I_{\text{pt2}}$  must be less than the minimum current limit of the device's power switch. Equation 11 yields 1.08 A, which is less than the 1.8-A current limit of the TPS54160A. The  $D_{\text{neg}}$  diode must be capable of handling the output current,  $I_{\text{oneg}}$ , which is 0.54 A from Equation 12. The difference between Equation 11 and Equation 10 is the inductor ripple current which is 0.160 A. The rms currents for the inductor windings from Equation 16 and Equation 17 are 0.742 A and 0.388 A, respectively. These currents are lower than the 0.82 A current rating in the inductor data sheet. Use the rms currents to estimate the power loss in the inductor using the Coilcraft ac loss estimator found on its Web site ([www.coilcraft.com](http://www.coilcraft.com)).

$$I_{\text{pt1}} = \frac{I_{\text{opos}} + I_{\text{oneg}}}{1 - D_{\text{max}}} - \frac{V_{\text{inmin}} \times D_{\text{max}}}{2 \times f_{\text{sw}} \times L_o} \quad (10)$$

$$I_{\text{pt2}} = I_{\text{pt1}} + \frac{V_{\text{inmin}} \times D_{\text{max}}}{f_{\text{sw}} \times L_o} \quad (11)$$

$$I_{\text{pt3}} = \frac{I_{\text{pt2}}}{2} \quad (12)$$

$$I_{\text{pt4}} = I_{\text{pt3}} - \frac{1}{2} \times \left( \frac{V_{\text{inmin}} \times D_{\text{max}}}{2 \times f_{\text{sw}} \times L_o} \right) \quad (13)$$

$$I_{\text{pt5}} = I_{\text{pt3}} \quad (14)$$

$$I_{pt6} = I_{pt5} - \frac{1}{2} \times \left( \frac{V_{inmin} \times D_{max}}{2 \times f_{sw} \times L_o} \right) \quad (15)$$

$$I_{L_o, negrms} = \sqrt{\frac{D}{3} \times (I_{pt1}^2 + I_{pt1} \times I_{pt2} + I_{pt2}^2) + \frac{1-D}{3} \times (I_{pt3}^2 + I_{pt3} \times I_{pt4} + I_{pt4}^2)} \quad (16)$$

$$I_{L_o, posrms} = \sqrt{\frac{1-D}{3} \times (I_{pt5}^2 + I_{pt5} \times I_{pt6} + I_{pt6}^2)} \quad (17)$$

## 1.6 Output Capacitor

The output capacitors must supply the current when the high-side switch is on. Use the minimum input voltage to calculate the output capacitance needed. This is when the duty cycle and the peak-to-peak current in the output capacitor is the maximum. Using the 0.5% voltage ripple specification,  $dV_{out}$ , and Equation 18,  $C_{onegmin}$  is 6.67  $\mu F$ . Assuming the 0.5% voltage ripple and maximum duty cycle, the ESR (equivalent series resistance) must be less than 103 m $\Omega$ , using Equation 19. The rms current for the output capacitor is 0.245 A, using Equation 20. Two 22- $\mu F$ /25-V X5R ceramic capacitors are used in parallel for the output capacitor because of the low ESR and size. Use the same output capacitance for the positive rail.

$$C_{onegmin} \geq \frac{I_{onegmax} \times D_{max}}{f_{sw} \times dV_{rneg}} \quad (18)$$

$$ESR \leq \frac{dV_{rneg}}{\frac{I_{onegmax}}{1-D_{max}} + \frac{1}{2} \times \frac{V_{inmin} \times D_{max}}{f_{sw} \times L_o}} \quad (19)$$

$$I_{conegrms} = I_{onegmax} \times \left( \frac{D_{max}}{1-D_{max}} \right)^{0.5} \quad (20)$$

## 1.7 Diode Selection

The diode voltage needs to be greater than the difference of the maximum input voltage and output voltage. For the example design, the diode needs to support a voltage greater than 42 V.

Using Equation 21, the power dissipation is calculated using the diode forward voltage drop,  $V_{fd}$ , at the maximum input voltage and the average diode current. Assuming  $V_{fd}$  of 0.5 V,  $P_{diode}$  is 0.150 W. The peak current in the diode is the same as the inductor, Equation 12. Select a diode which has a power rating greater than 0.150 W and supports the inductor current. Use a diode with the same requirements for the positive supply rail.

$$P_{diodeneg} = V_{fd} \times I_{oneg} \quad (21)$$

## 1.8 Power Dissipation in Package

The power dissipation in the package is dominated by the conduction losses and switching losses of the power switch and must not exceed the limitations of the package. The conduction and switching losses can be calculated using Equation 16. The conduction losses are a function of the duty cycle,  $D$ , inductor rms current,  $I_{Lrms}$ , and on resistance,  $R_{hs}$ . The switching losses are a function of the turnon,  $t_r$ , and turnoff,  $t_f$ , times, switching frequency, output current, and input and output voltages.

$$I_{swrms} = \left( D_{nom} \times \left( \left( \frac{I_{opos} + I_{oneg}}{1-D_{nom}} \right)^2 + \frac{1}{12} \times \left( \frac{V_{in} \times D_{nom}}{f_{sw} \times L_o} \right)^2 \right) \right)^{0.5} \quad (22)$$

$$P_{device} = I_{swrms}^2 \times R_{hs} + \frac{1}{2} \times (V_{in} - V_{oneg}) \times \left( \frac{I_{opos} + I_{oneg}}{1-D} \right) \times (t_r + t_f) \times f_{sw} \quad (23)$$

$I_{swrms}$  is calculated to be 0.522 A at nominal duty cycle.  $P_{device}$  is 0.279 W assuming a  $t_r$  and  $t_f$  of 25 ns.

## 1.9 Frequency Response of the Positive/Negative Regulator

The single-output inverting power supply transfer function is discussed in the application report [4], and the following equations are formed in a similar manner, because the positive/negative regulator uses the inverting power supply as the base converter.

The equations are very similar, but need modifying because of the dual output and the feedback network is across both outputs.

The ESR zero, fz1, is calculated using Equation 25 and is a function of the output capacitor and its ESR. Because the feedback is connected to the positive output, the effective output capacitance is one-half of the Co and the effective ESR is two times the ESR of the Co capacitor. The one-half Co and the two ESR cancel to have the same ESR zero location as the single-output inverting power supply [4].

The other zero is a right half plane zero, fz2. The frequency response of the fz2 results in an increasing gain and a decreasing phase. The fz2 frequency is a function of the duty cycle, load resistance, and the inductor. Equation 26 calculates the minimum frequency of the fz2 which is used to determine the crossover frequency. Similar to the ESR zero equation, the RHP zero equation is written with modifications because of a dual output; the end-result yields the same as the single-output equation.

The dominant pole, fpole, is a function of the load resistance, output capacitor, and duty cycle (see Equation 27). The effective load resistance is two times the single-output resistance, and the effective capacitance is one-half the single-output capacitance; the end-result for the dominant pole is the same as the single output.

Kpna is the dc gain and is used to calculate the frequency compensation components. The gm<sub>ps</sub> variable is the transconductance of the power stage, which is 6 A/V for the TPS54160A. The fz1 is estimated to be 1033 kHz. The output capacitor is derated by 30% because of the dc voltage and the ESR is assumed to be 5 mΩ. The fz2 is estimated to be 38.5 kHz. Assuming resistance of the inductor, R<sub>dc</sub> is 0.476 Ω. The fp1 is estimated to be 166 Hz, assuming a nominal duty cycle. Kpna is approximately 240 V/V assuming nominal input voltage, no slope compensation, and high modulation gain.

$$T(s) = K_{pna} \times \frac{\left(1 + \frac{s}{2 \times \pi \times fz1}\right) \times \left(1 - \frac{s}{2 \times \pi \times fz2}\right)}{1 + \frac{s}{2 \times \pi \times fp1}} \quad (24)$$

$$fz1 = \frac{1}{2 \times R_c \times \frac{C_o}{2} \times 2 \times \pi} \quad (25)$$

$$fz2 = \frac{(1 - D_{max})^2 \times \left(\frac{-V_{oneg}}{l_o} \times 2\right) + (R_{dc} \times 2) \times ((1 - D_{max}) - D_{max})}{D_{max} \times (L_o \times 2) \times 2 \times \pi} \quad (26)$$

$$fp1 = \frac{(1 + D_{min})}{\left(\frac{-V_{oneg}}{l_o} \times 2\right) \times \left(\frac{C_o}{2}\right) \times 2 \times \pi} \quad (27)$$

$$K_{pna} \approx \frac{V_{in} \times \left(\frac{-V_{oneg}}{l_o} \times 2\right)}{V_{in} + 2 \times (-V_{oneg})} \times gm_{ps} \quad (28)$$

The crossover of the power supply must be set between the fp1 and 1/3 of fz2 frequencies. It is recommended to start with the crossover frequency, f<sub>co</sub>, given by Equation 29. The f<sub>co</sub> is estimated to be 1459 Hz.

$$f_{co} = \left(fp1 \times \frac{fz2}{3}\right)^{0.5} \quad (29)$$

The compensation resistor, R<sub>comp</sub>, needed to set the compensation gain at the f<sub>co</sub> frequency, is calculated using . The V<sub>ref</sub> is 0.8 V and gm<sub>ea</sub> is 92 μA/V for the TPS54160A.

$$R_{\text{comp}} = \left( \frac{f_{\text{co}}}{K_{\text{pna}} \times f_{\text{p1}}} \right) \times \left( \frac{V_{\text{opos}} - V_{\text{oneg}}}{V_{\text{ref}} \times g_{\text{mea}}} \right) \quad (30)$$

Substitute  $f_{\text{co}}$  into Equation 30, to calculate  $R_{\text{comp}}$ .  $R_{\text{comp}}$  is equal to 11.9 k $\Omega$ . Use the nearest standard value of 11.7 k $\Omega$ . The compensation zero is set to one-half of the dominant pole,  $f_{\text{p1}}$ . To calculate the compensation zero capacitor,  $C_{\text{zero}}$ , use Equation 31. Equation 31 gives 163 nF; use the next larger standard value which is 160 nF. The compensation pole is set to equal the RHP zero,  $f_{\text{z2}}$ . Use Equation 32, to calculate the frequency compensation pole,  $C_{\text{pole}}$ , which gives 354 pF. The next standard value is 359 pF.

$$C_{\text{zero}} = \frac{1}{\frac{f_{\text{p1}}}{2} \times 2\pi \times R_{\text{comp}}} \quad (31)$$

$$C_{\text{pole}} = \frac{1}{f_{\text{z2}} \times 2\pi \times R_{\text{comp}}} \quad (32)$$

### 1.10 Input Capacitors

The TPS54160A needs a tightly coupled bypass capacitor,  $C_{\text{d}}$ , in Figure 1, connected to the VIN and GND pins of the device. Because the device GND is the power supply output voltage, the voltage rating of the capacitor must be greater than the difference in the maximum input and output voltage of the power supply. Equation 33 to Equation 36 are used to estimate the capacitance, maximum ESR, and current rating for the input capacitor,  $C_{\text{in}}$ .

$$I_{\text{inavg}} = \frac{(I_{\text{opos}} + I_{\text{oneg}}) \times D_{\text{max}}}{1 - D_{\text{max}}} \quad (33)$$

$$C_{\text{in}} = \frac{I_{\text{inavg}}}{f_{\text{sw}} \times 0.01 \times V_{\text{inmin}}} \quad (34)$$

$$\text{ESR}_{\text{cin}} \leq \frac{0.01 \times V_{\text{inmin}}}{I_{\text{inavg}}} \quad (35)$$

$$I_{\text{cinrms}} = \left( \left( I_{\text{pt2}} - I_{\text{inavg}} \right)^2 + \frac{\left( \frac{V_{\text{inmin}} \times D_{\text{max}}}{L_{\text{o}} \times f_{\text{sw}}} \right)^2}{12} \right) \times D_{\text{max}} + I_{\text{inavg}}^2 \times (1 - D_{\text{max}}) \quad (36)$$

### 1.11 Slow-Start Time

Placing a small ceramic capacitor on the SS/TR to the chip GND (i.e., system  $V_{\text{out}}$ ) adjusts the slow-start time on the TPS54160A. The slow-start capacitor is calculated using Equation 30. The equation assumes a 2- $\mu\text{A}$  pullup and 10% to 90% measurement for time.

$$C_{\text{ss}} = \frac{t_{\text{ss}}(\text{s}) \times 2 \times 10^{-6}}{V_{\text{ref}}(\text{V}) \times 0.8} \quad (37)$$

### 1.12 Frequency Set Resistor

The switching frequency is set with a resistor,  $R_{\text{T}}$ , from the RT/CLK pin to the GND of the TPS54160A device. Use Equation 31 to estimate the frequency set resistor.

$$R_{\text{T}}(\text{k}\Omega) = \frac{206033}{f_{\text{sw}}(\text{kHz})^{1.0888}} \quad (38)$$

### 1.13 Synchronizing to an External Clock

The TPS54160A has a CLK pin that can be used to synchronize the power supply switching frequency to an external system clock. But a level shift circuit needs to be used to translate a system ground reference clock signal to the device's ground.

### 1.14 Start Voltage

When used as a step-down regulator, the TPS54160A has an adjustable start and stop voltage when using the resistors on the EN pin. The stop voltage is lower than the start voltage. When used as an inverting power supply, only the start voltage can be useful. After the inverting power supply starts up, the effective input voltage the TPS54160A device experiences rises as the output voltage reaches full regulation. Therefore, it is recommended to use a lower value resistor on the high side to minimize the hysteresis voltage. The input voltage has to drop by the output voltage and the hysteresis voltage to shut down the supply. See the *Enable and Adjusting Undervoltage Lockout* section of the TPS54160A data sheet ([SLVSB56A](#)) for the equation.

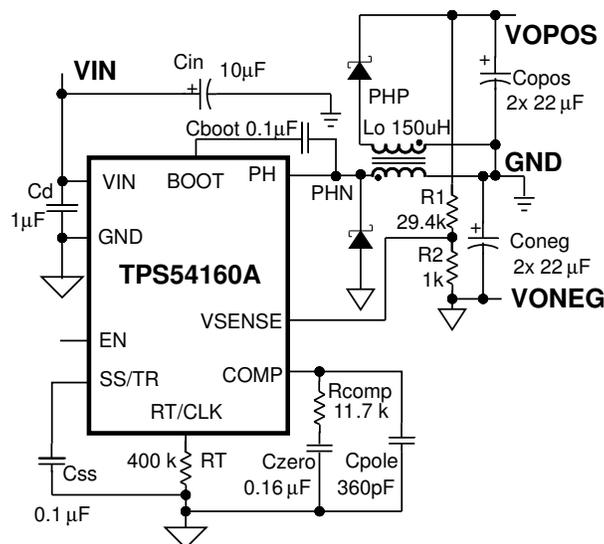


Figure 3. 24-V to ±12-V/0.3-A Power Supply

### 1.15 Experimental Results

The Figure 4 to Figure 23 show the experimental test results of the Figure 3 design. The discontinuous conduction mode (DCM) to continuous conduction mode (CCM) boundary is at an output current of 24 mA. The pulse skip mode (PSM) boundary is at an output current of 2.5 mA. The input current draw at no load at 24-V input voltage is 2.53 mA.

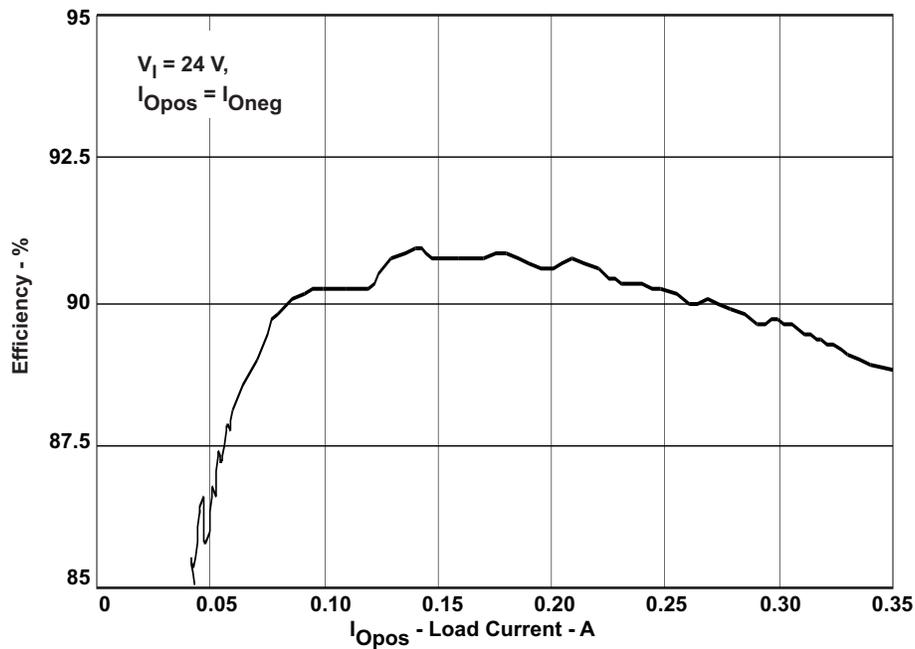


Figure 4. Efficiency vs  $I_{Opos}$  Load Current

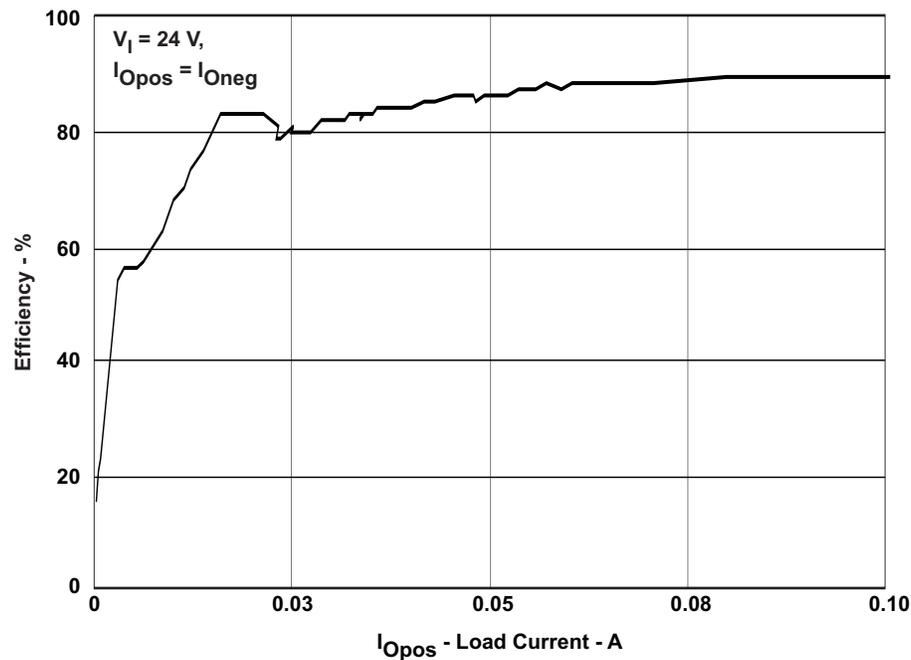


Figure 5. Efficiency vs  $I_{Opos}$  Load Current

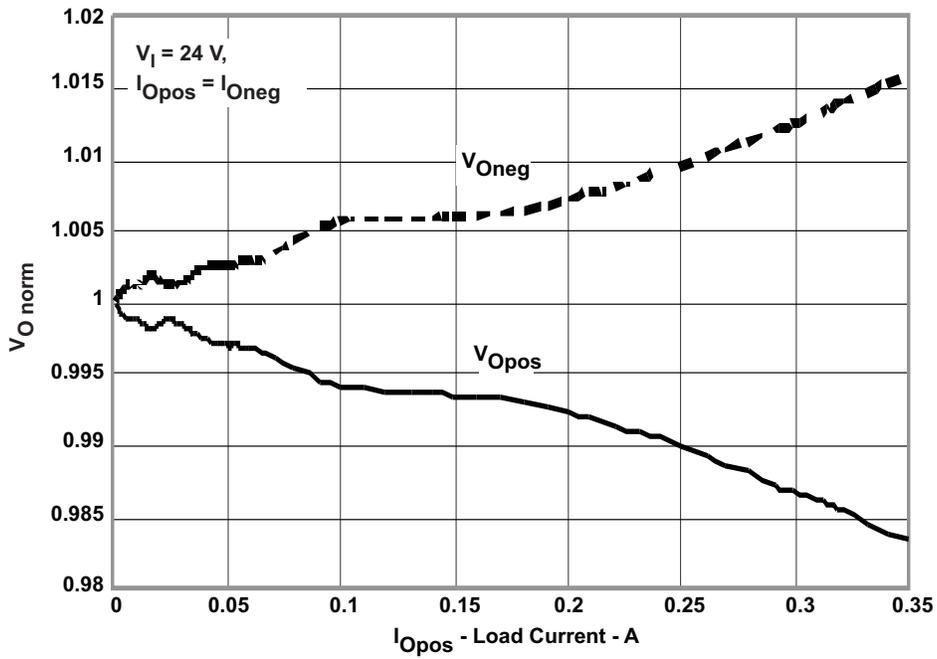


Figure 6. Output Regulation vs Load Current

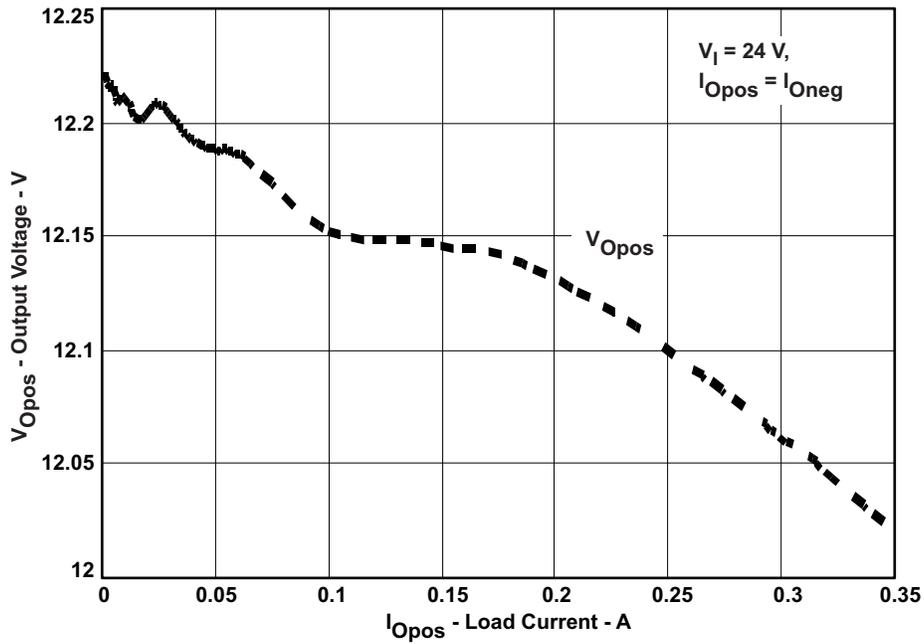


Figure 7. V<sub>Opos</sub> Regulation vs Load Current

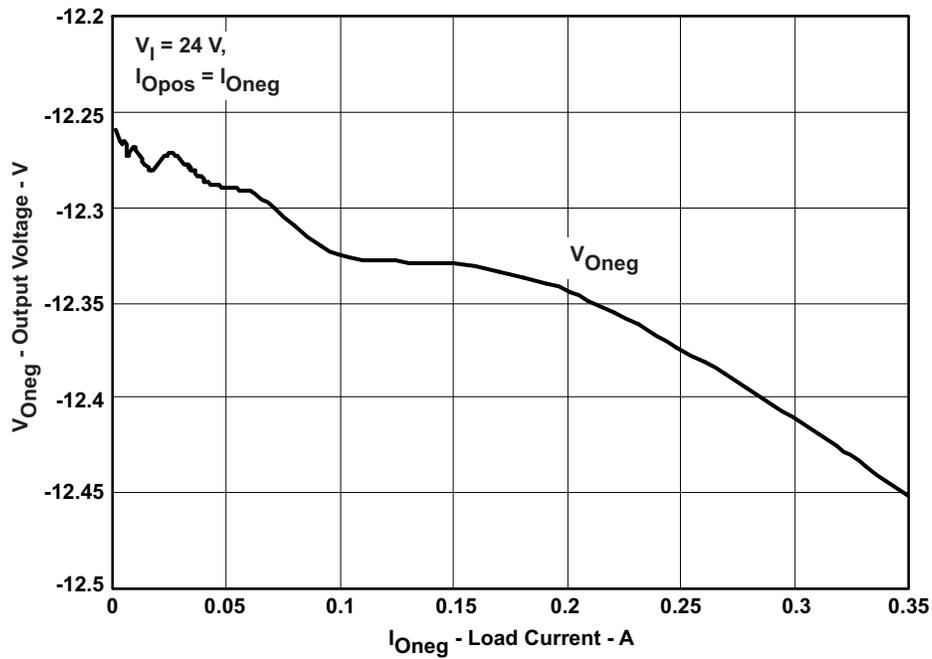


Figure 8.  $V_{Oneg}$  Regulation vs Load Current

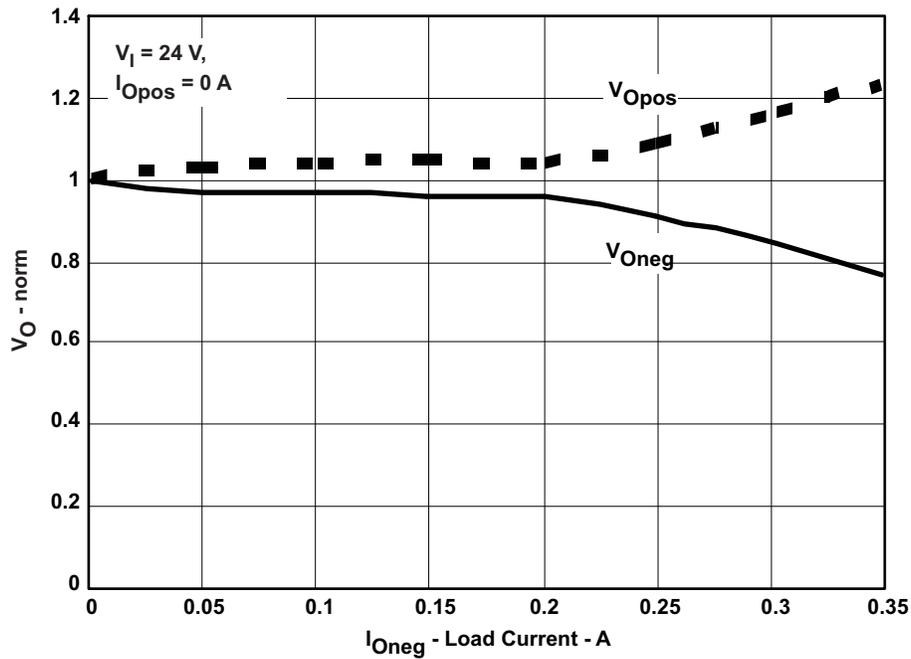


Figure 9. Cross Regulation

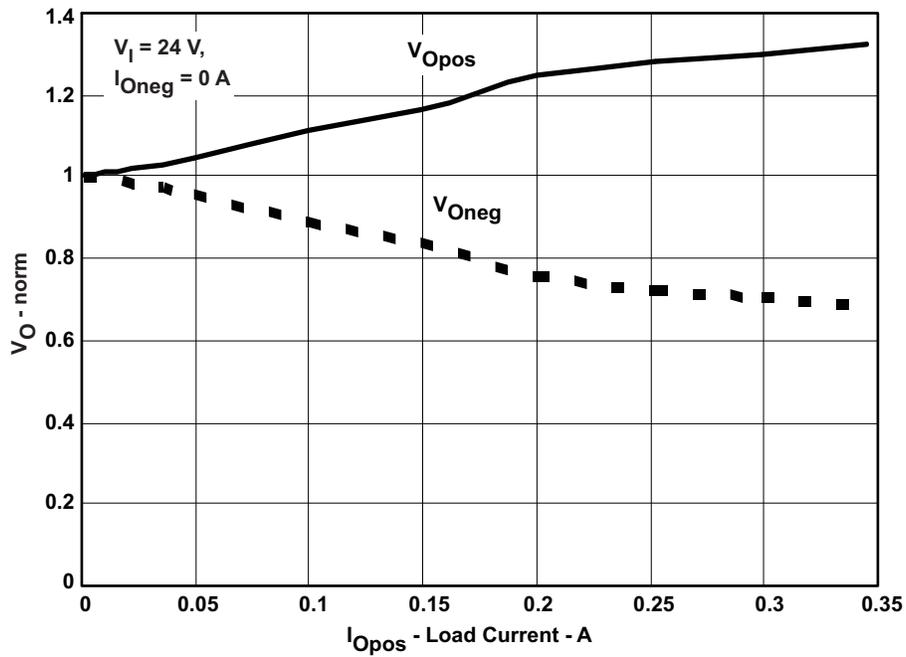


Figure 10. Cross Regulation

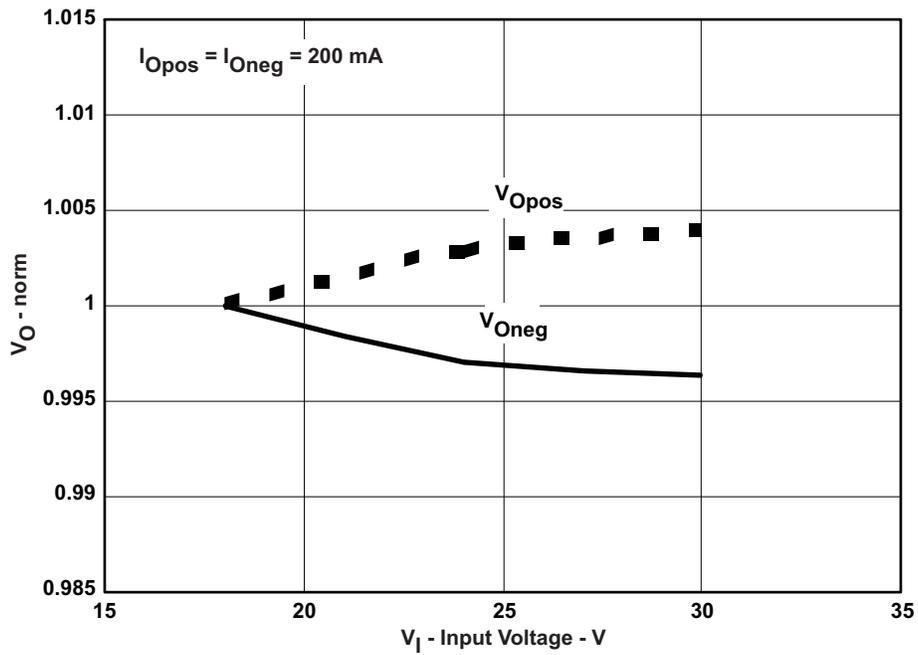


Figure 11. Output Regulation vs Input Voltage

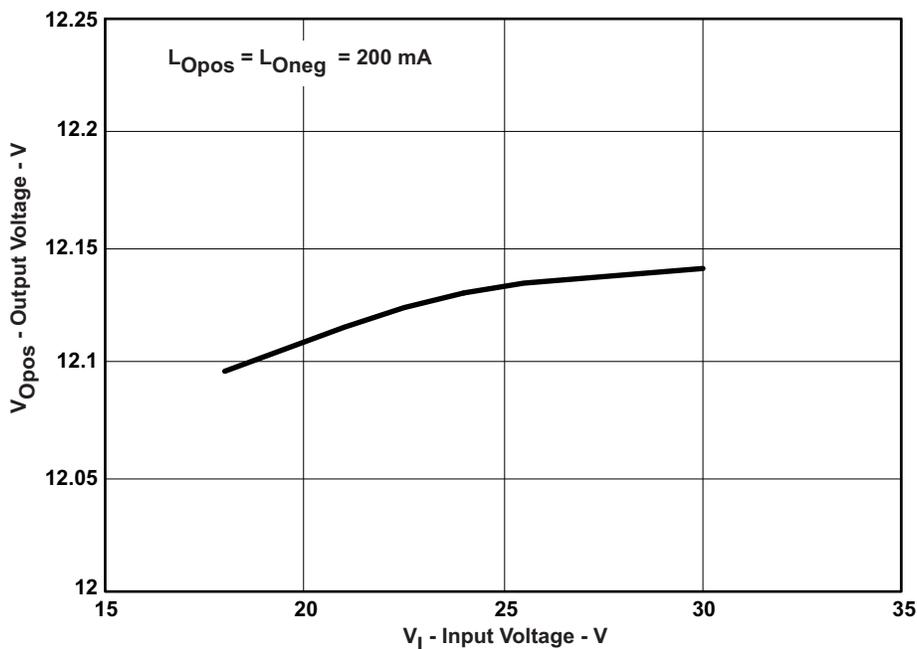


Figure 12.  $V_{Opos}$  Regulation vs Input Voltage

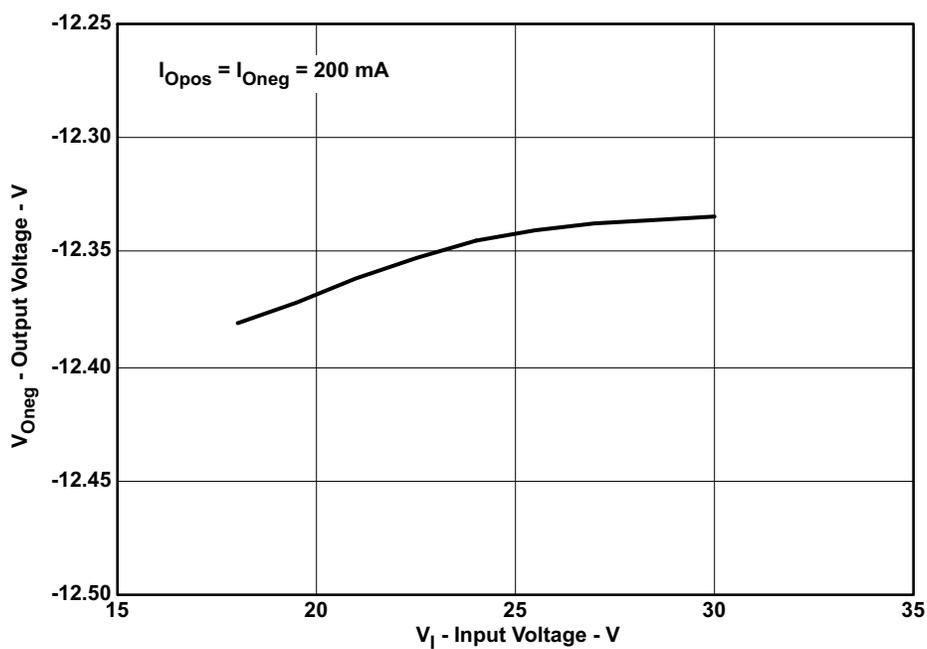


Figure 13.  $V_{Oneg}$  Regulation vs Input Voltage

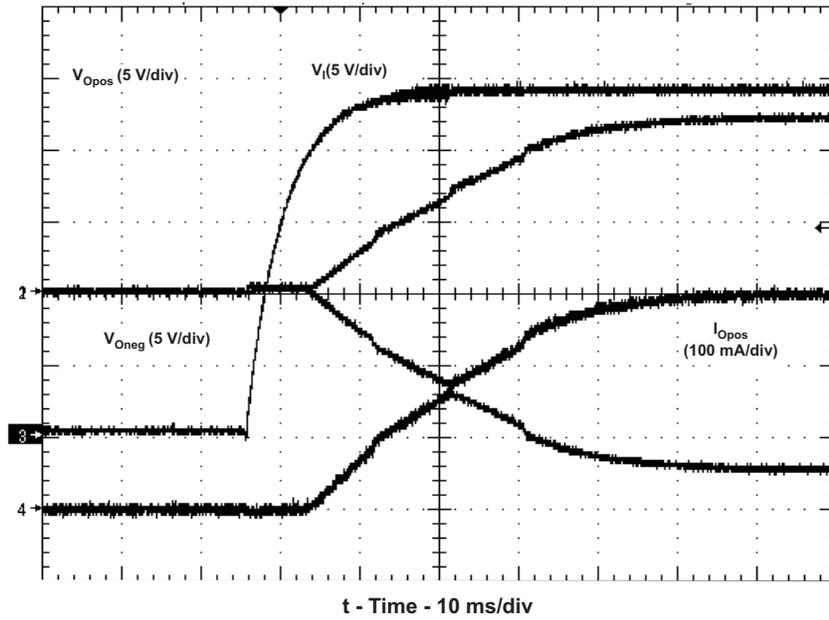


Figure 14. Power Up in 300-mA Load

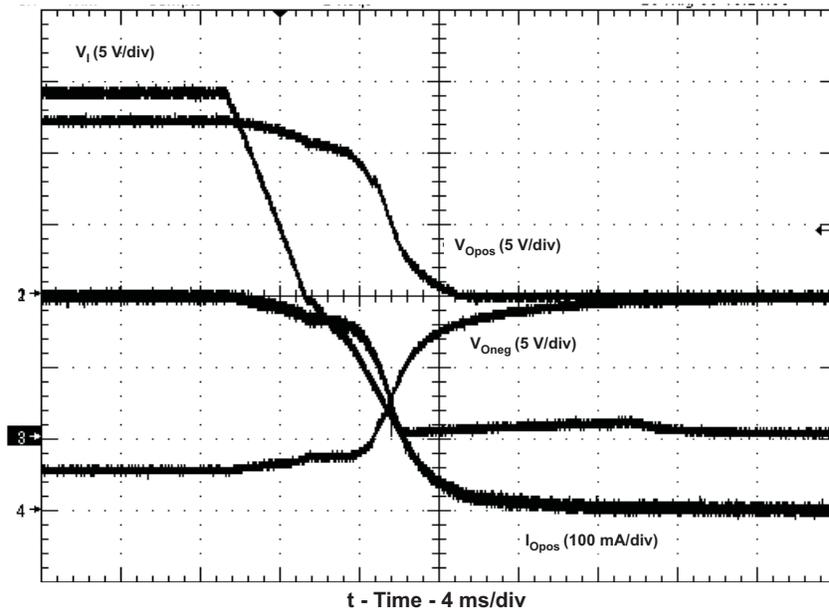


Figure 15. Power Down With 300-mA Load

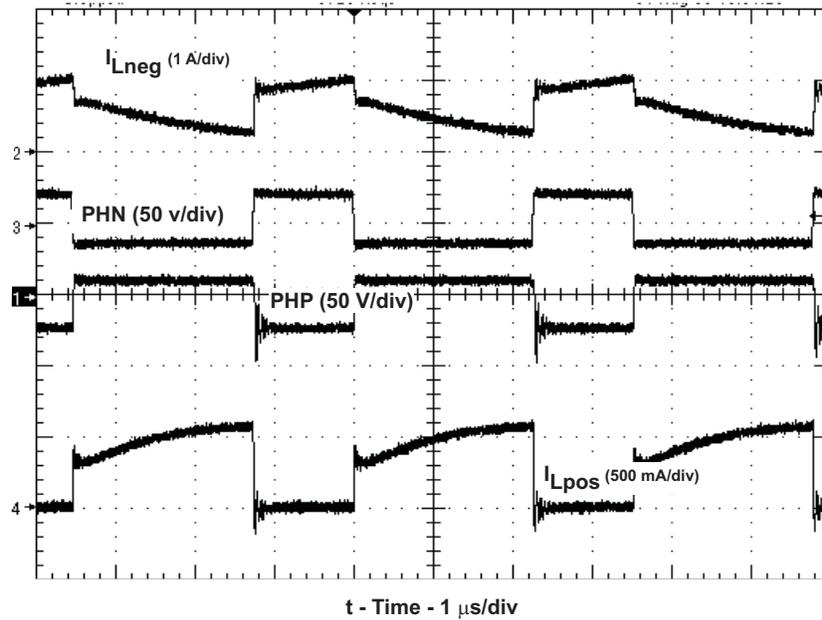


Figure 16. Switch Node and Current Waveforms in CCM Operation

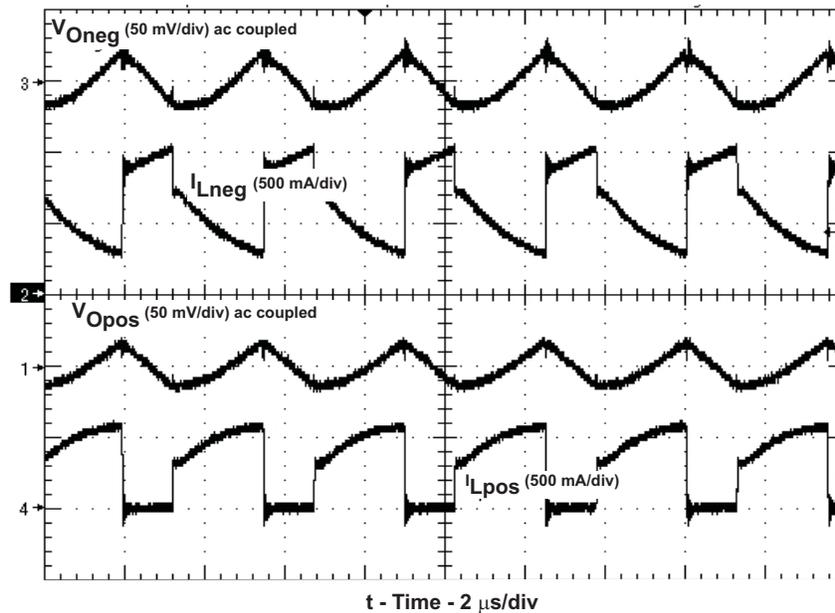


Figure 17. Output Voltage Ripple at 300-mA Output Current

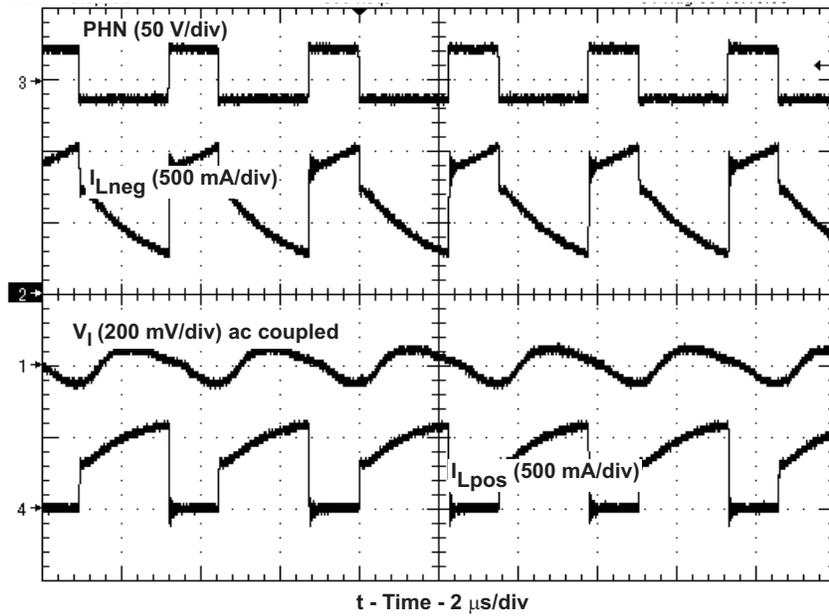


Figure 18. Output Voltage Ripple at 300-mA Output Current

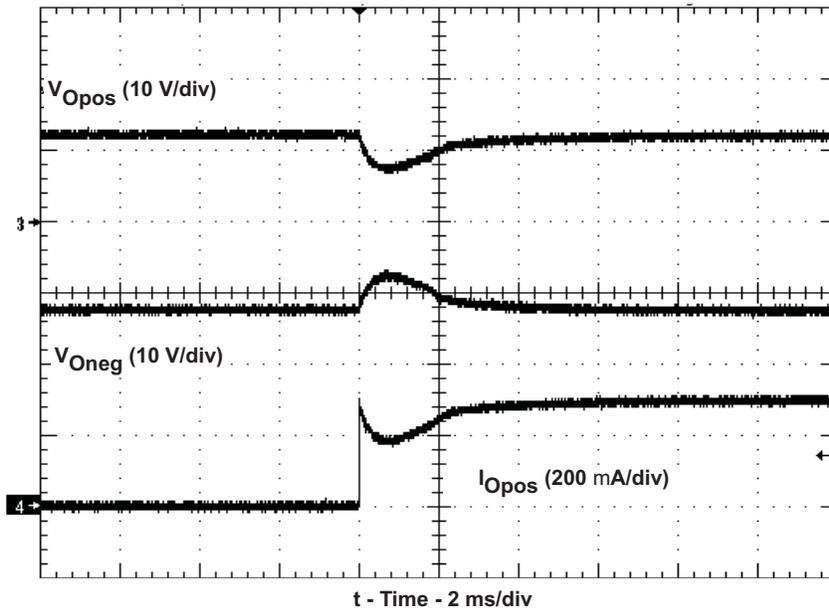


Figure 19. Load Step Response 0 mA to 300 mA at 24 V

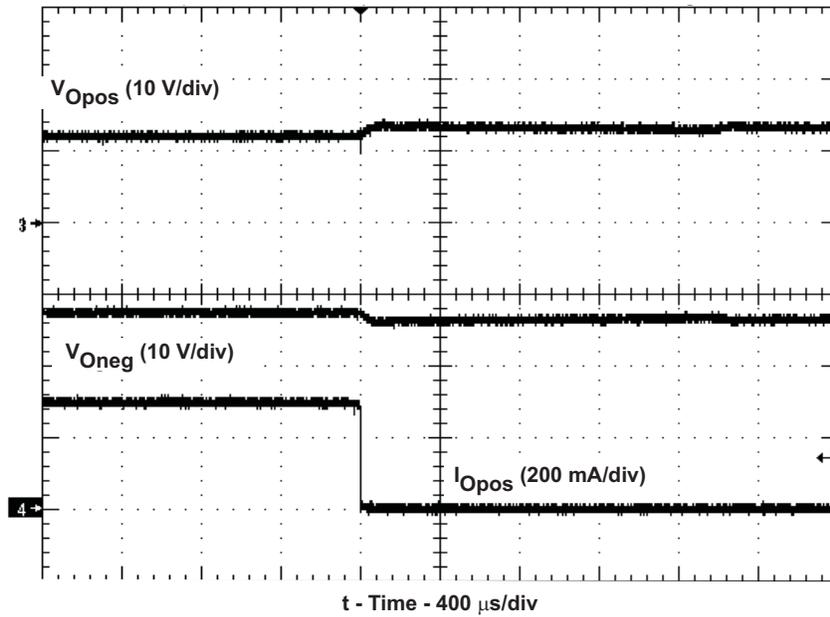


Figure 20. Unload Step Response 300 mA to 0 mA at 24 V

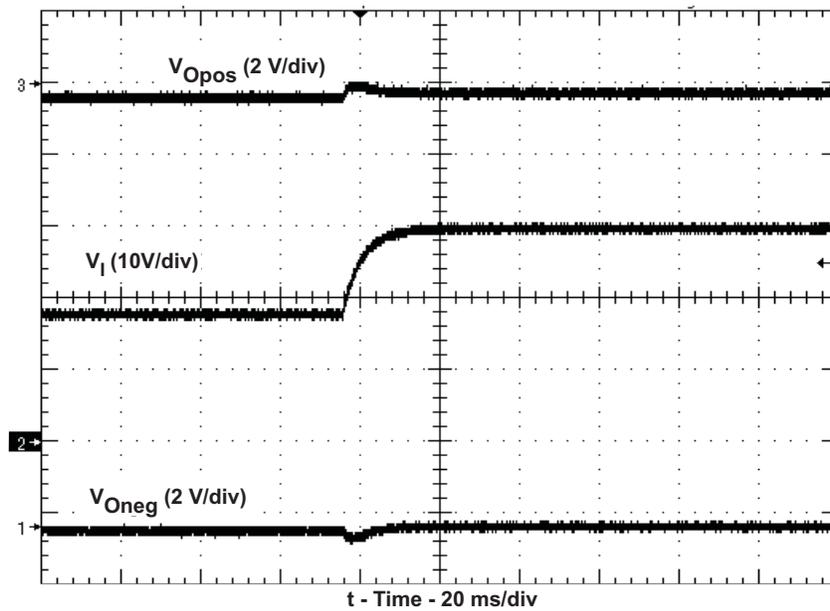


Figure 21. Line Step Response 18 V to 30 V at 300 mA

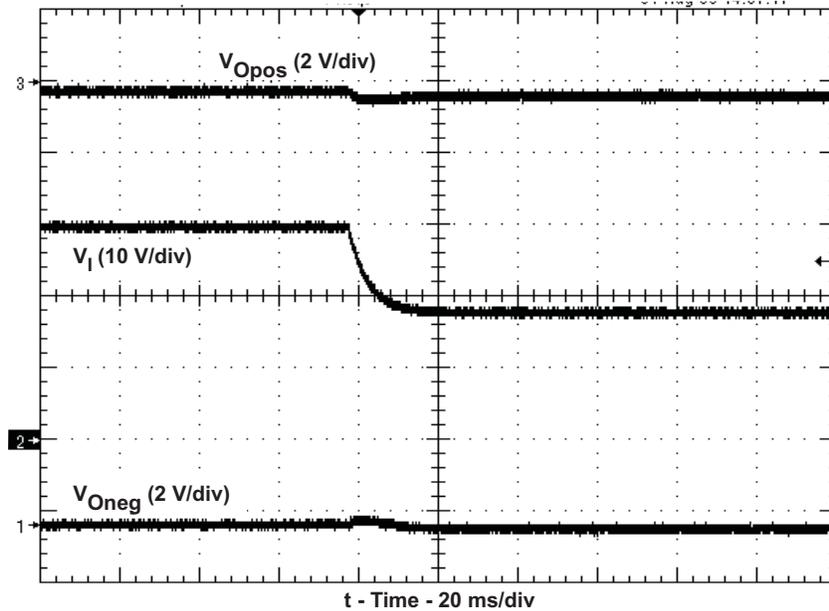


Figure 22. Line Step Response 30 V to 18 V at 300-mA

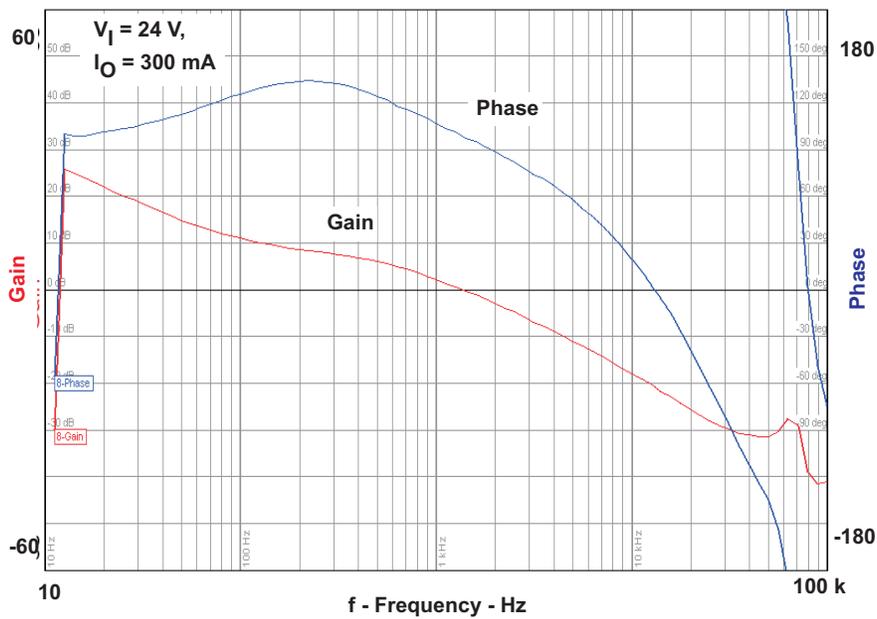


Figure 23. Frequency Response  $V_{IN} = 24$  V and  $I_{out} = 300$  mA

## 2 References

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