Application Report

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TPS54160 60-V, Step-Down LED Driver Design Guide

Daniel Acevedo and John Tucker

PMP-DC/DC SWIFT Converters

ABSTRACT

The TPS54160 is normally used as a buck voltage regulator. In these applications, a lower dc voltage is derived from a higher input voltage. The output voltage is regulated by the internal current mode control circuitry to maintain a constant voltage over varying line and load conditions. The TPS54160 is not limited to use in the standard buck topology. This application report demonstrates the TPS54160 used as a high-brightness LED driver. Rather than maintaining the constant regulated voltage of the buck converter, a current-regulated source is desired. The circuit must maintain a constant current with an output voltage that varies with changes in the LED forward voltage drop due to variation in the number of LEDs and temperature. To achieve current regulation, the voltage across a known resistance (R_4) is regulated. R_4 is connected from the voltage feedback pin (VSENSE) to GND. The LEDs are connected from the output of the inductor to VSENSE. In addition to these design modifications, the output capacitor must be connected across the LEDs (load), from the output of the inductor to VSENSE.

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1 Schematic Diagram

The schematic diagram of the LED driver circuit is shown in Figure 1. The input voltage source is a nominal 24 V. The circuit is designed to drive four LEDs in series with a drive current of 700 mA. When driving these four LEDs, the nominal output voltage relative to ground is approximately 14.8 V. Provisions for both analog and PWM dimming of the LED string are provided.

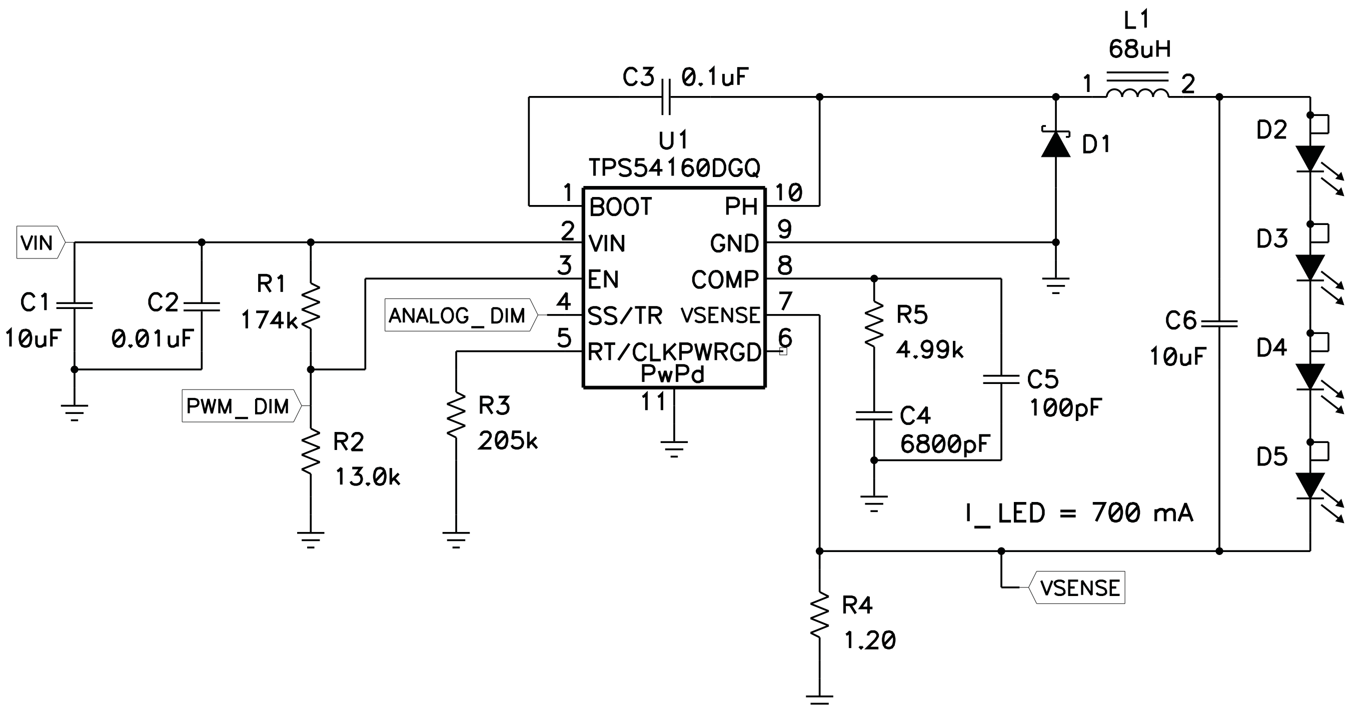


Figure 1. LED Driver Circuit

2 Design Procedure

2.1 Output Current Set Point

The output current can be set by changing the value of the current sense resistor, R_4. The sense resistor is

$$R_4 = \frac{V_{REF}}{I_O} \tag{1}$$

Note: the power dissipation of this resistor must be considered for package size and is

$$\frac{V_{REF}^2}{R_4} = P_{DIS} \tag{2}$$

This resistor R_4 is considered part of the supply, not the load. For this design example, V_{REF} = 0.8 V and I_O = 700 mA. Using Equation 1, R_4 = 1.14 Ω. A standard 1-W resistor value of 1.2 Ω is used for R_4. The calculated power dissipation using Equation 2 is 0.53 W.

2.2 Output Voltage

The supplied output voltage of the LED driver circuit is approximated by:

$$V_{OLED} = N_{LED} \times V_{LED} + V_{REF} \tag{3}$$

Where:

N_{LED} = number of LEDs
V_{LED} = forward voltage drop of each LED

V_{REF} = the TPS54160 reference voltage

Using Equation 3, the approximate LED supply voltage is 14.8 V.

2.3 Enable and Adjusting Undervoltage Lockout

The voltage on the EN pin sets the status of the device, on or off. The EN pin has an internal pullup current source, I_1, of 0.9 µA that provides the default condition of the TPS54160 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 µA of hysteresis, I_{hys}, is added. This additional current facilitates input voltage hysteresis. A resistor divider from VIN to EN to GND must be implemented to ensure that the TPS54160 does not turn on until the input voltage is approximately 3 V above the desired output voltage. Use the undervoltage lockout (UVLO) adjust resistors to provide consistent power-up behavior. Use Equation 4 and Equation 5 to calculate the two external resistors for UVLO.

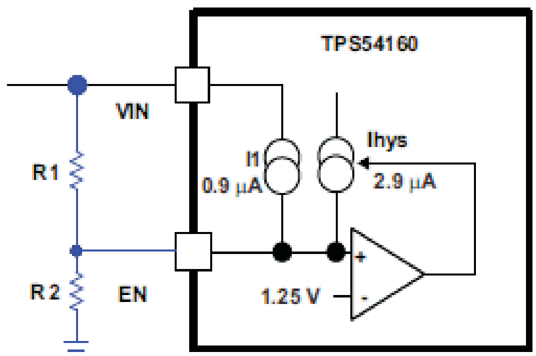


Figure 2. Adjustable Undervoltage Lockout

$$R_1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{4}$$

$$R_2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \tag{5}$$

For this design, the desired start voltage must be 14.8 V + 3 V = 17.8 V, and the stop voltage must be 17.8 V – 0.5 V = 17.3 V. Using Equation 4 and Equation 5 , the required values for R_1 and R_2 are 172 kΩ and 12.9 kΩ. The closest standard values of 174 kΩ and 13.0 kΩ are used for R_1 and R_2.

2.4 Switching Frequency

The response time of the converter depends both on the closed-loop bandwidth of the circuit and the switching frequency. Because this circuit is designed to run under a constant load condition, response time is not a high priority. Higher switching frequencies enable the use of smaller output filter components whereas lower switching frequencies tend to have higher efficiencies. The TPS54160 can be operated at switching frequencies from 300 kHz to 2500 kHz.

The switching frequency has additional limitations. As the frequency is increased, the on time for a given duty cycle is decreased. For consistent switching action without pulse skipping, the on time must be greater than the minimum controllable on time. For the TPS54160, this minimum controllable on time is typically 130 ns. The TPS54160 also features frequency foldback. During overcurrent conditions, the output voltage decreases as the overcurrent protection is activated. As the foldback voltage at VSENSE decreases below 0.6 V, the switching frequency is reduced by 50% of the nominal value. At a VSENSE voltage of 0.4 V, the switching frequency is reduced to 25%, and finally when the VSENSE voltage falls below 0.2 V, the switching frequency is reduced to 12.5% of the nominal set frequency. This is done so that in any individual switching cycle, sufficient time is available for the inductor current to ramp below the overcurrent threshold. So, the set switching frequency must be less than $f_{SW(max\ skip)}$ and $f_{SW(max\ shift)}$.

$$f\text{sw(maxskip)} = \frac{1}{t_{ONmin}}\left(\frac{I_L \times R_{DC} + V_{OLED} + V_D}{V_{INMAX} - I_L \times R_{DS} + V_D}\right) \tag{6}$$

$$f\text{sw(maxshift)} = \frac{f\text{div}}{t_{ONmin}}\left(\frac{I_{OUTSC} \times R_{DC} + V_{OUTSC} + V_D}{V_{INMAX} - I_{OUTSC} \times R_{DS} + V_D}\right) \tag{7}$$

I_L	inductor current
R_{DC}	inductor resistance
V_{INMAX}	maximum input voltage
V_{OUT}	output voltage
V_{OUTSC}	output voltage during short
I_{OUTSC}	output short circuit current
Vd	diode voltage drop
$R_{DS(on)}$	switch on resistance
t_{ONmin}	minimum controllable on time
$f$div	frequency division factor (1, 2, 4, or 8)

Using Equation 6 and Equation 7, the maximum skip and shift frequencies are 3.28 MHz and 1.83 MHz. Both of these frequencies are beyond the operating range of the TPS54160.

This design uses a nominal switching frequency of 570 kHz to allow for high efficiency while still providing reasonably sized components. The switching frequency is set by placing a resistor, R_3, from the RT/CLK pin to ground. The value of the R_3 is calculated by:

$$R_3\,(\text{k}\Omega) = \frac{206033}{f\text{sw}(\text{kHz})^{1.0888}} \tag{8}$$

For 570 kHz, the switching frequency, R_3 must be 205 kΩ.

2.5 Power Dissipation in Low-Side Diode

During the converter on time, the output current is provided by the internal switching FET. During the off time, the output current flows through the catch diode. The average power in the diode is given by:

$$\text{Pdiode} = \left(1 - \frac{V_{OLED}}{V_{IN}}\right) \times Vf\text{d} \times \text{Io} \tag{9}$$

For this design, the catch diode must dissipate 0.187 W.

2.6 Input Capacitor

The TPS54160 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3 mF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54160. The rms input ripple current can be calculated using:

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{V_{OLED} \times (\text{Vinmin} - \text{Vout})}{\text{Vinmin} \times \text{Vinmin}}} \tag{10}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using:

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{11}$$

For this circuit, the rms current is 340 mA, and the input voltage ripple is 31 mV.

2.7 Output Inductor

The output inductor must be selected so that the peak-to-peak ripple current is 30% of the output current. Verify that the RMS and saturation current ratings for the inductor exceed application specifications.

$$Lo >= \frac{V_{OLED} \times (Vinmax - V_{OLED})}{Vinmax \times f sw \times Io \times 0.30} \tag{12}$$

Once the inductor is chosen, the peak-to-peak inductor current can be calculated using Equation 13.

$$I_{LPP} = \frac{V_{OLED} \times (Vinmax - V_{OLED})}{Vinmax \times f sw \times L_O} \tag{13}$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{V_{OLED} \times (Vinmax - Vout)}{Vinmax \times L_O \times f sw}\right)^2} \tag{14}$$

$$ILpeak = Io + \frac{1}{2} \times \left(\frac{Voled \times (Vinmax - Vout)}{Vinmax \times L_O \times f sw}\right) \tag{15}$$

The required minimum inductor is calculated to be 72 µH. The nearest standard value inductor is 68 µH. The calculated peak-to-peak, rms, and peak currents are 224.8 mA, 703 mA, and 812 mA. For this design, a 68-µH Coilcraft MSS1038-683ML_ is used. The rms current rating is 1.82 A, and the saturation current rating is 1.75 A.

2.8 Output Capacitor

The output capacitor is selected to limit the ripple current in the LED string. First, calculate the dynamic resistance of the LED string using Equation 16.

$$R_{LED} = \frac{\Delta V f}{\Delta I f} \times N_{LED} \tag{16}$$

This can be found on the data sheet for the LED used. For this application, the average forward current is 700 mA, and the average forward voltage is 3.4 V for each LED. The slope of the V/I curve for the LED at that operating point is the LED dynamic resistance. In this case, the dynamic resistance is determined to be 1.25 Ω per LED. For four LEDs, the total is 5 Ω.

The output ripple current of the converter is the output inductor peak-to-peak current (ILPP). This ripple current is shared by the output filter capacitor and the LED string. The impedance of the output capacitor is given by:

$$Zco = R_{ESR} + \frac{1}{2\pi \times f sw \times Co} \tag{17}$$

The ripple current in the LED string is:

$$\Delta I_{LED} = I_{LPP} \times \frac{Z_{CO}}{Z_{CO} + R_{LED}} \tag{18}$$

And the rms ripple current in the output capacitor is

$$Icorms = \frac{I_{LPP} \times R_{LED}}{\sqrt{12} \times (R_{LED} + Z_{CO})} \tag{19}$$

For this design, a ceramic output capacitor is used. To estimate the output capacitor impedance, start with a value of 10 µF for Co. The ESR of this capacitor is small compared to the reactance of the capacitor and is ignored. The design requirement is to limit the LED ripple current to less than 3 mA. The required capacitance can be found from Equation 20.

$$C_O \geq \frac{I_{LPP} - \Delta I_{LED}}{2 \times \pi \times fsw \times R_{LED} \times \Delta I_{LED}} \tag{20}$$

For 3-mA LED ripple current, the output capacitor must be at least 8.48 µF. A 10-µF capacitor is used. For most LED driver applications, the impedance of the output capacitor is small compared to the impedance of the LEDs. Most of the ripple current is shunted through the output capacitor Equation 4 rather than through the LED string.

With 10 µF, the LED ripple current from Equation 18 is 1.47 mA and the output capacitor ripple current from Equation 19 is 224.8 mA.

The output capacitor is connected across the load, from the output of the inductor (V_{oled}) to VSENSE.

The rms current in the output capacitor is 65.5 mA. The ceramic capacitor used has an rms current rating of 3 A.

2.9 Compensation

To stabilize the closed-loop circuit, a compensation network is required. The small signal model for the TPS54160 is rather complex when operating as a current driver. For this design procedure, some simplifying assumptions are made. The compensation components are connected from the COMP pin to GND. Many techniques are used to stabilize closed-loop circuits like the LED driver described here. Stability can be achieved by Type I compensation, which uses a single capacitor from COMP to GND. Improved performance can be achieved using more advanced compensation topologies such as TYPE II or Type III. In any case, to properly compensate the closed-loop circuit, the gain characteristics of the power stage must be determined. In general, the power stage DC gain, the power stage pole, and the power stage zero frequency must be known. These terms are defined as follows:

Gain

$$G_{PS} = \frac{R_{CS} \times V_{IN} \times F_m}{(F_m \times V_{IN} \times R_i) + R_{DC} + R_{LED} + R_{CS}} \quad (21)$$

Pole Frequency

$$f\text{pole} = \frac{1}{2\pi\sqrt{L_O \times C_O}} \times \sqrt{\frac{(Fm \times V_{IN} \times R_i) + R_{DC} + R_{LED} + R_{CS}}{R_{LED} + R_{ESR}}} \quad (22)$$

Zero Frequency

$$f\text{zero} = \frac{1}{2 \times \pi \times C_O(R_{LED} + R_{ESR})} \quad (23)$$

Where:

$R_i = 1 / gm_{PS} = 1/6$

R_{CS} = current sense resistor (R4)

$$Fm = \frac{f\text{sw}}{\left(\frac{V_{IN} - V_{OLED}}{Lo}\right) \times R_i + Se}$$

Se = 250000

For simple Type I compensation, a single capacitor is used to create a pole at the origin. The unity gain frequency of the compensated error amplifier is given by:

$$f_{INT} = \frac{1}{2 \times \pi \times C_5 \times \text{gmea}} \quad (24)$$

The unity gain bandwidth of the compensated error amplifier must be at 1/3 the power stage pole frequency, fpole. The required value of C5 is given by:

$$C_5 = \frac{\text{gmea} \times 3}{2\pi \times f\text{pole}} \quad (25)$$

For the design inputs in this example, the required compensation capacitor is C_5 = 3700 pF. Using the closest standard value of 3900 pF, the measured closed-loop response is shown in Figure 3.

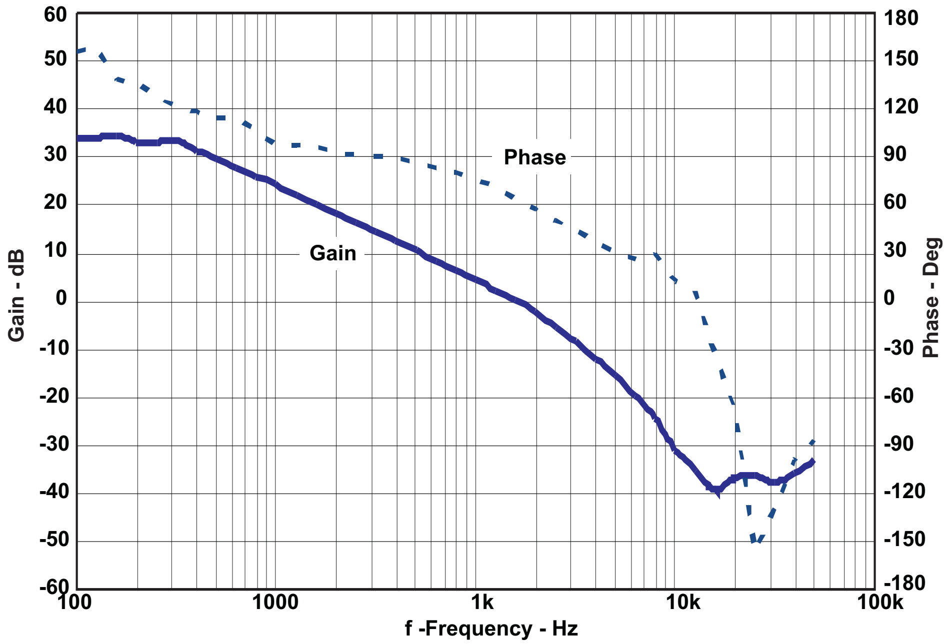


Figure 3. Type I Compensation Closed-Loop Response

The closed-loop crossover frequency is 16 kHz, and the phase margin is 60 degrees. To extend the loop bandwidth and/or increase the phase margin, a Type II compensation scheme can be employed. This is the compensation shown in the schematic of Figure 1. For this Type II compensation, an additional series resistor (R_5) and parallel capacitor (C_4) are added with C_5 as shown. The design goal is to increase the closed-loop bandwidth to 27 kHz.

For this design, the modulator gain is 4.107 and the zero frequency is 3.18 kHz. The pole frequency was previously determined to be 10.4 kHz. By definition, at crossover the gain of the compensated error amplifier plus the gain of power stage must be unity or 0 dB. The gain of the compensated error amplifier at the crossover frequency must be:

$$Gcomp_{FCO} = \frac{Fco^2 \times f zero}{f pole^3 \times G_{PS}} \quad (26)$$

The required compensation components now can be determined. The compensation resistor R5 is selected to provide the required gain at the crossover frequency.

$$R5 = \frac{Gcomp_{FC0}}{gmea} \quad (27)$$

C4 is selected to provide adequate phase boost. The compensation zero formed by C4 and R5 is placed at a frequency 2.5 times lower than the power stage pole frequency. The value of C4 can be calculated using:

$$C4 = \frac{2.5}{2 \times \pi \times R5 \times f pole} \quad (28)$$

C5 is used to roll off the gain of the error amplifier at high frequencies. For ceramic output capacitors, place the pole formed by C5 and R5 at one-half the switching frequency. The value of C5 is given by:

$$C5 = \frac{1}{\pi \times f sw \times R5} \quad (29)$$

For this design, the compensation components are calculated as

R_5 = 5.10 kΩ
C_4 = 7632 pF
C_5 = 112 pF

Using standard values, the actual components are:

R_5 = 4.99 kΩ
C_4 = 6800 pF
C_5 = 100 pF

The measured closed-loop response is shown in Figure 4.

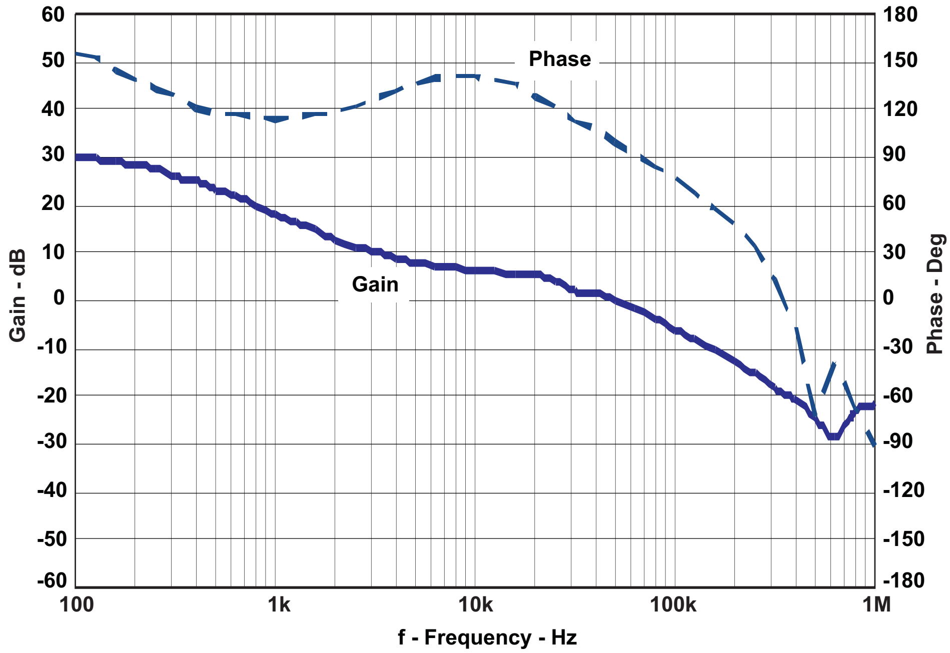


Figure 4. Type II Compensation Closed-Loop Response

The closed-loop bandwidth is 45 kHz with 100 degrees of phase margin.

This procedure works well for a string of approximately four LEDs. As the number of LEDs increases, the peaking of the power stage gain can cause the approximations in this procedure to become less accurate. Choosing a closed-loop crossover frequency well above the power stage pole frequency can minimize these differences.

2.10 Slow-Start Capacitor

The slow-start capacitor must be left (open) unpopulated.

3 Additional Considerations

3.1 Open-Load Condition

Buck converters are inherently not susceptible to open-load conditions. If the LED string is opened or disconnected, no current is in the sense resistor and VSENSE goes to 0 V. The TPS54160 now operates at maximum duty cycle, and the output voltage goes to Vin minus any losses in the converter. Because this design uses a buck converter, VOLED cannot exceed VIN as would be the case when using a boost converter.

3.2 Dimming

3.2.1 PWM Dimming Using EN

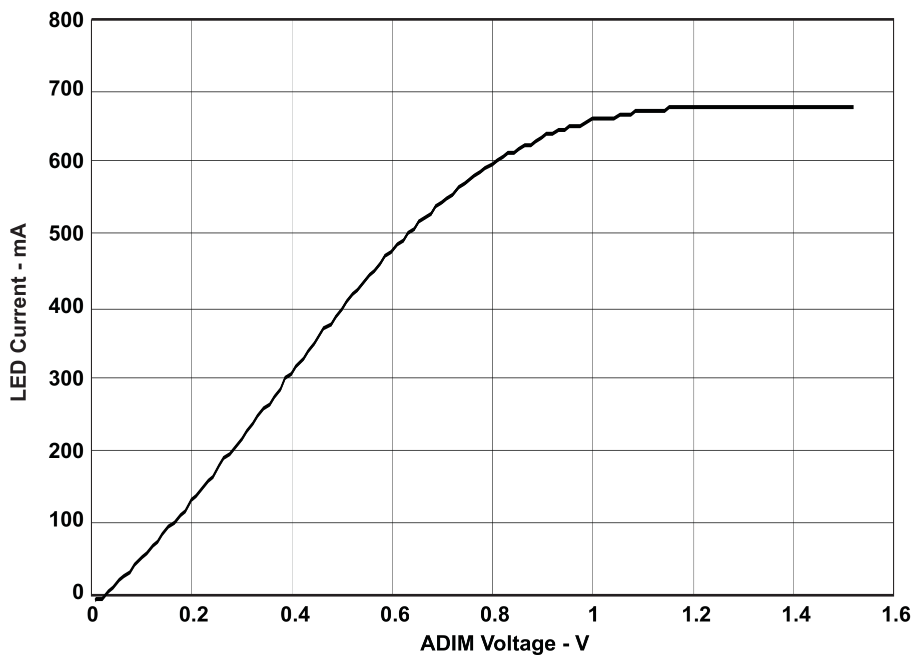
The brightness of the LEDs can be adjusted by applying a PWM signal to the EN pin. The average LED current is proportional to the PWM signal duty cycle. When EN is greater than $V_{turn\ on}$ × R4 / (R4 + R5) the TPS54160 drives current through the LEDs. When less than $V_{turn\ off}$ × R4 / (R4 + R5), the TPS54160 turns off and stops driving current through the LEDs. In this case, $V_{turn\ on}$ is the converter enable voltage, and $V_{turn\ off}$ is the converter disable voltage.

3.2.2 Dimming Using VSENSE

The voltage on VSENSE sets the duty cycle of the converter. Implementing the procedure in SLEA004 allows for dimming on VSENSE. The same method is used to extend battery life by decreasing power dissipation in the current sense resistor as described in Section 3.3.

3.2.3 Dimming Using SS/TR

The voltage applied to this pin is used as reference if it is below the TPS54610 internal voltage reference of 800 mV. The following graph was generated with Vin = 24, Vout = 14.8 V and 700 mA as the nominal output current. Note that the parameters associated with dimming on SS/TR are not characterized, and therefore analog dimming on SS/TR must be configured on an individual basis.



3.3 Extending Battery Life with the TPS54160 High-Brightness LED Driver

Using the method described in SLEA004, the current sense resistor (R_{CS}) can be sized to minimize power dissipation. The same method is used to perform dimming on V_{SENSE} as previously described.

3.4 Evaluation Module

The circuit presented in this application report is available as an evaluation module, TPS54160EVM-535. For additional information, see the TPS54160 product folder.

3.5 Design Calculator

A design calculator is available on line to assist in LED driver designs for the TPS54160. The design calculator is an Excel™ spreadsheet and is available in the TPS54160 product folder.