Simplifying Stability Checks

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ABSTRACT

This application report explains a method for verifying relative stability of a circuit by showing the relationship between phase margin in an AC loop response and ringing in a load-step analysis.

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1 What is Stability and Phase Margin?

When discussing control systems, stability is a term referring to the ability of a controller to regain a constant or decaying output after an input or load disturbance, such as a step function. Stability is an important criterion for control circuits because they have inherent delay in the feedback loop(s). If the output signal lags one full wavelength, it becomes superimposed on the input signal of the controller and the circuit becomes unstable and oscillates.

Phase margin (PM) is a measure of relative stability, in degrees, that indicates the likelihood of a closed-loop control system to oscillate when given a disturbance such as a step function. For systems with a negative angle phase response, the PM is the difference between –180° (due to the inverting nature of most amplifiers) and the phase angle of the frequency response at the same frequency where the magnitude response is 1 or 0 db. For systems with a positive phase response, the phase margin is merely the phase itself at the frequency where the magnitude response is 1 or 0 db. A positive PM technically yields a *stable system* whereas a negative PM yields an unstable system. However, a system with a 3° PM, for example, is not necessarily stable because practical factors make such a small degree of margin unreliable. Thus, a PM of about 45° is considered generally acceptable, but this can vary based on the designer's preference. This classic method of finding the phase margin can be observed in Figure 1.

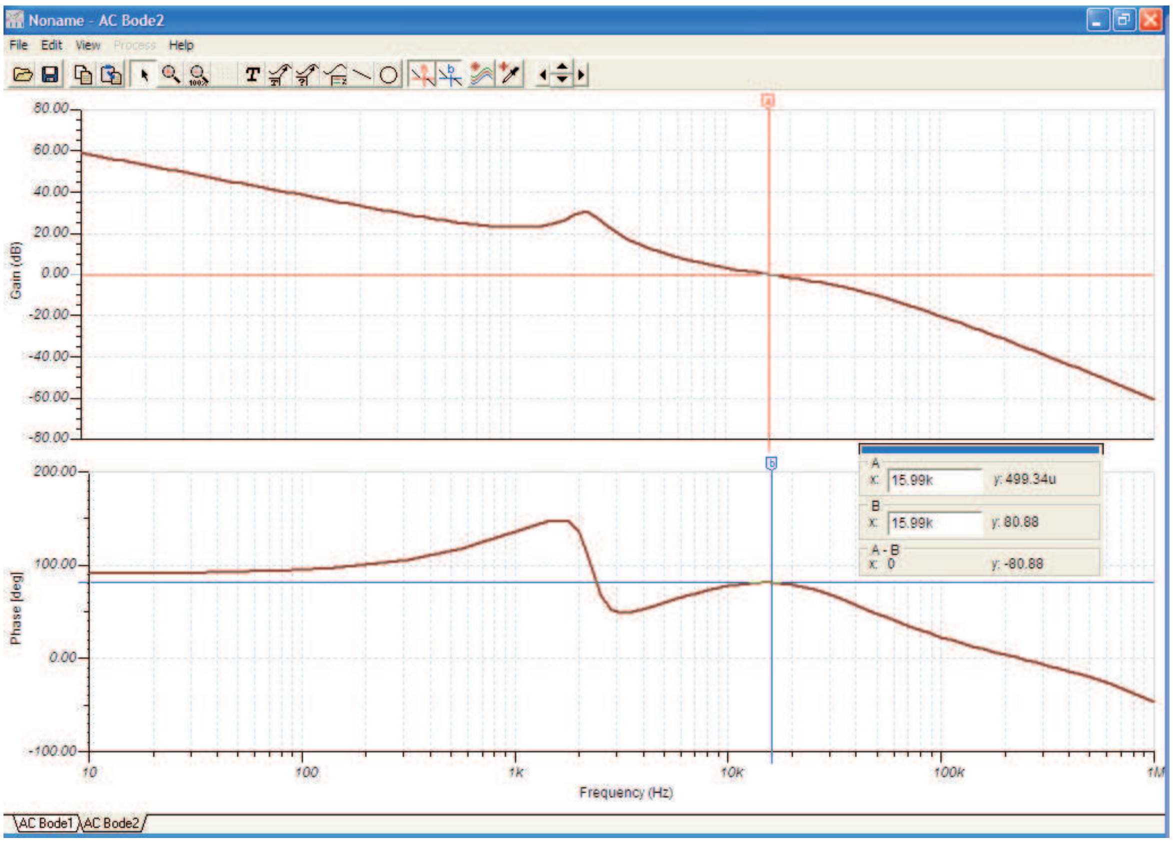


Figure 1. Calculating Phase Margin From a Frequency Response Plot

As can be seen in the plot of Figure 1, an AC response, (Magnitude on top and Phase underneath), is given. The Magnitude Response plot is shown to be 0 db at 15.99 kHz. The phase at 15.99 kHz is 80.88°. Thus, the phase margin of this system is 80.88°.

Although this method is acceptable for simulated devices, in real systems it creates many problems. For example, many devices with control systems cannot tolerate the wide range of frequencies necessary for such an analysis. Further, to conduct such a test requires an isolation of the feedback loop which in some cases is difficult or impossible. Although tools such as network analyzers can test stability directly, the cost sometimes restricts their availability. Therefore, an alternate method to test stability using a common laboratory oscilloscope is now considered.

2 What is Ringing and How Does it Relate to Stability?

Ringing is the unwanted oscillation seen in a voltage or current signal when the input or load is changed very quickly. If the controller cannot correct the output properly, overshoot and/or undershoot can occur, until it is damped out according to the damping factor of the system. In the extreme case, the system becomes unstable and the output oscillates indefinitely at the frequency where the gain = 1 and phase margin is 0°. In a circuit with a positive phase margin, the oscillations decay and are limited in number. Considering this, it can be stated that fewer bumps (peaks) or ripples in the transient load-step response correspond to more damping and a higher phase margin. In Figure 2, this relationship can be observed.

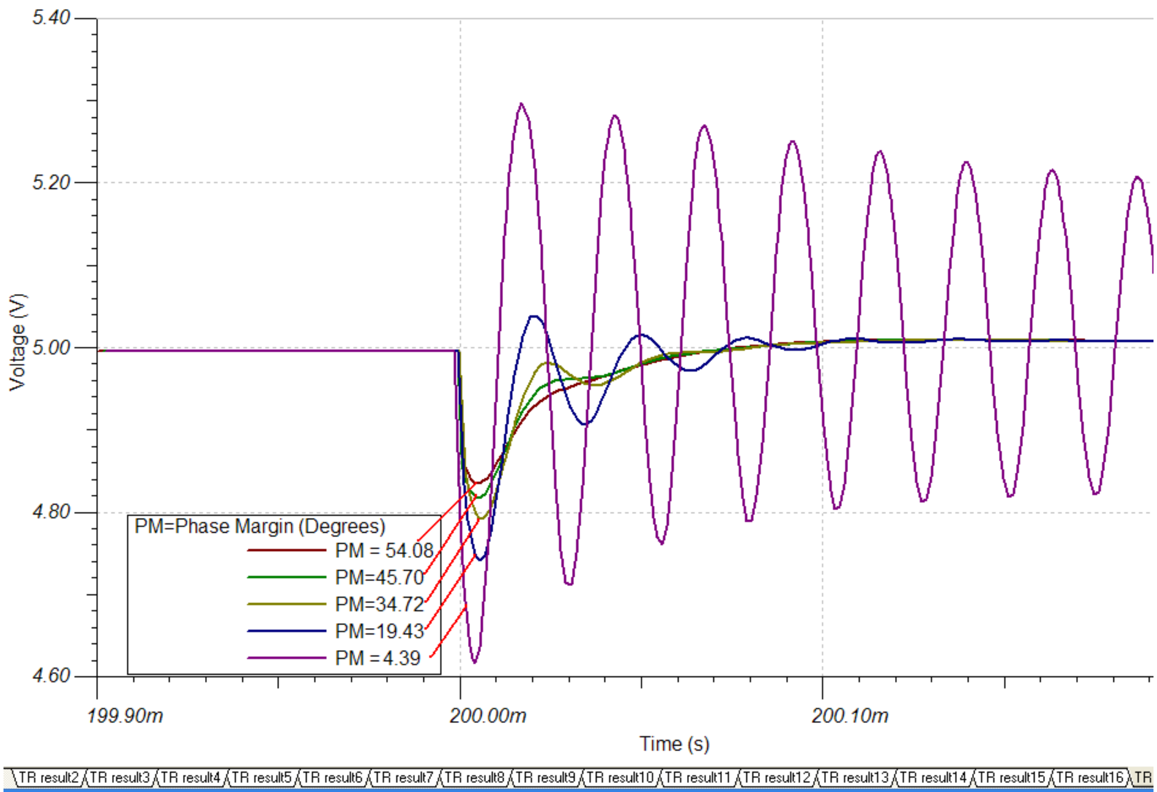


Figure 2. Comparison of Load Step Responses for Varying Phase Margin

As Figure 2 illustrates, the response with the highest PM, 54.08°, (in brown), damps the fastest. As PM decreases, the number of oscillatory peaks increases until eventually, at very low PM, the circuit is in lightly damped oscillation. For a quick reference, see Table 1.

Table 1. Phase Margin vs Ringing in Load-Step Response

Phase Margin (Degrees)	Ringing (Bumps)
80.88	0
60.75	0
57.64	0
54.08	0
50.16	1
45.7	1.5
40.61	2
34.72	3
27.78	4
19.43	6
9.09	17

2.1 Example Test Setup

The device under test (DUT) can be set up as seen in Figure 3

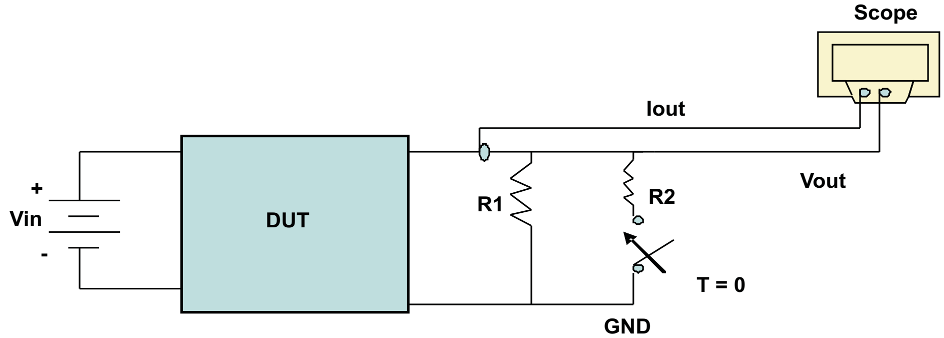


Figure 3. Example Test Setup for Finding Step-Response

2.2 Examples of Load Step Analysis

For a better definition of what an oscillatory *bump* or peak is, see Figure 4, Figure 5, and Figure 6.

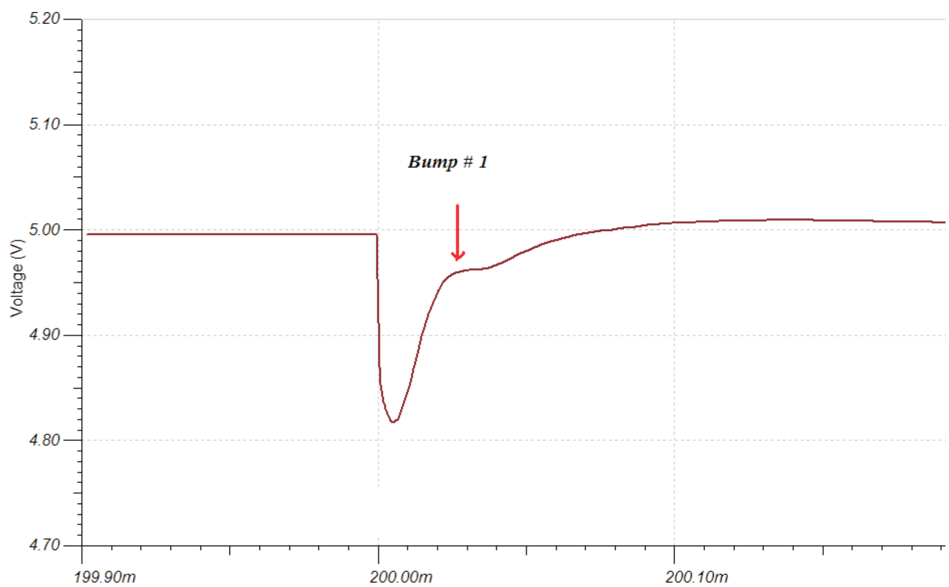


Figure 4. Load Step With Phase Margin = 45.7° (1 Peak)

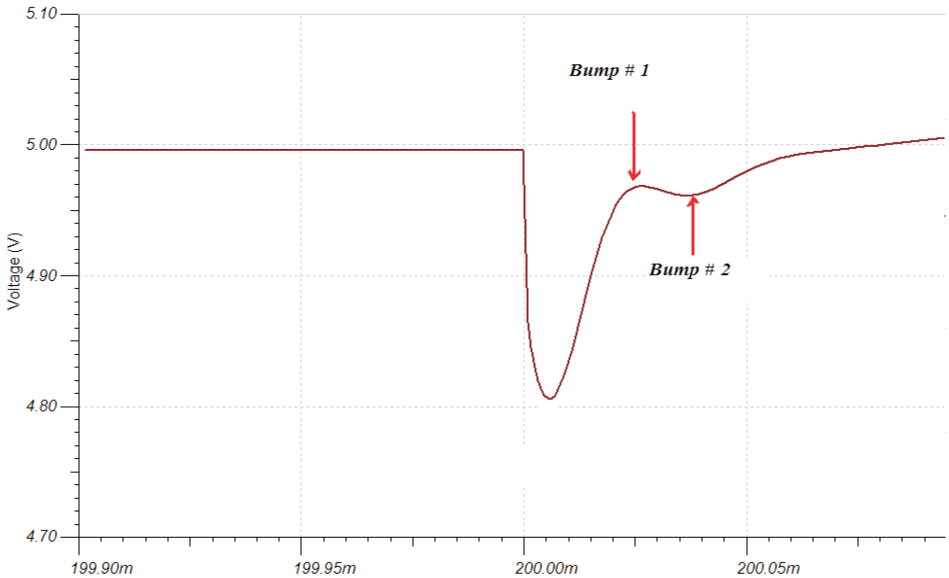


Figure 5. Load Step With Phase Margin = 40.61° (2 Peaks)

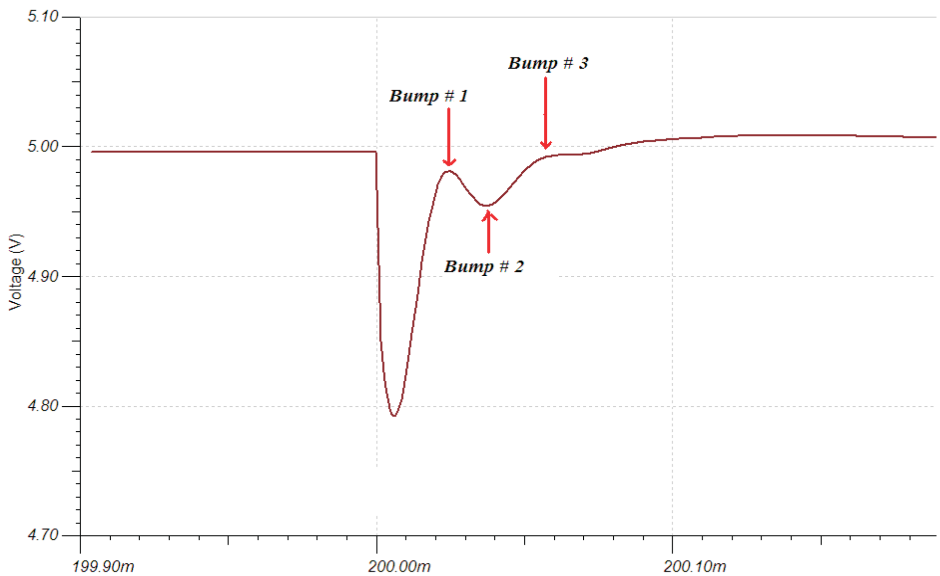


Figure 6. Load Step With Phase Margin = 34.72° (3 Peaks)

2.3 TPS5430 Laboratory Tests

To verify that these simulations produce realistic results, the TPS5430 was tested in a laboratory.

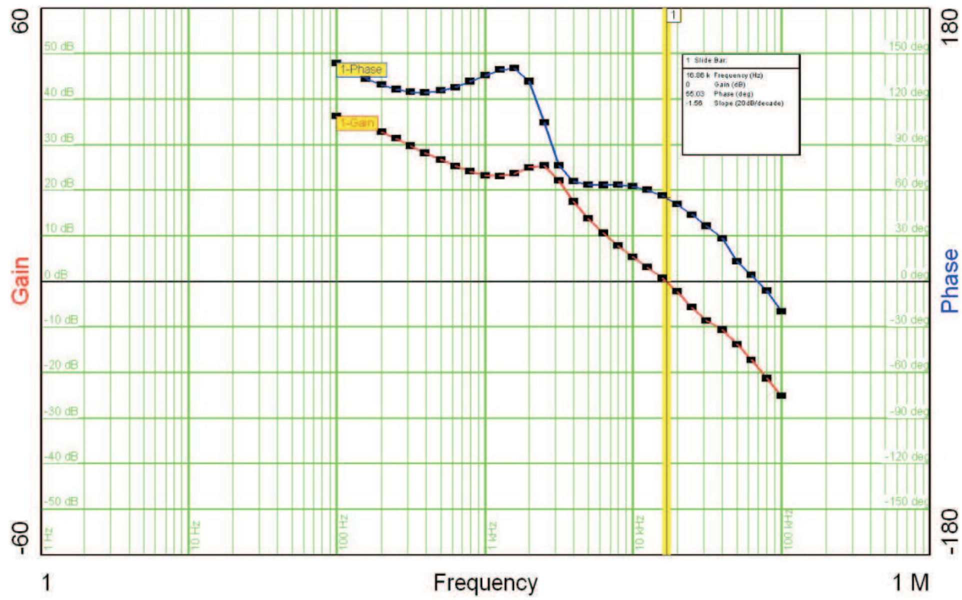
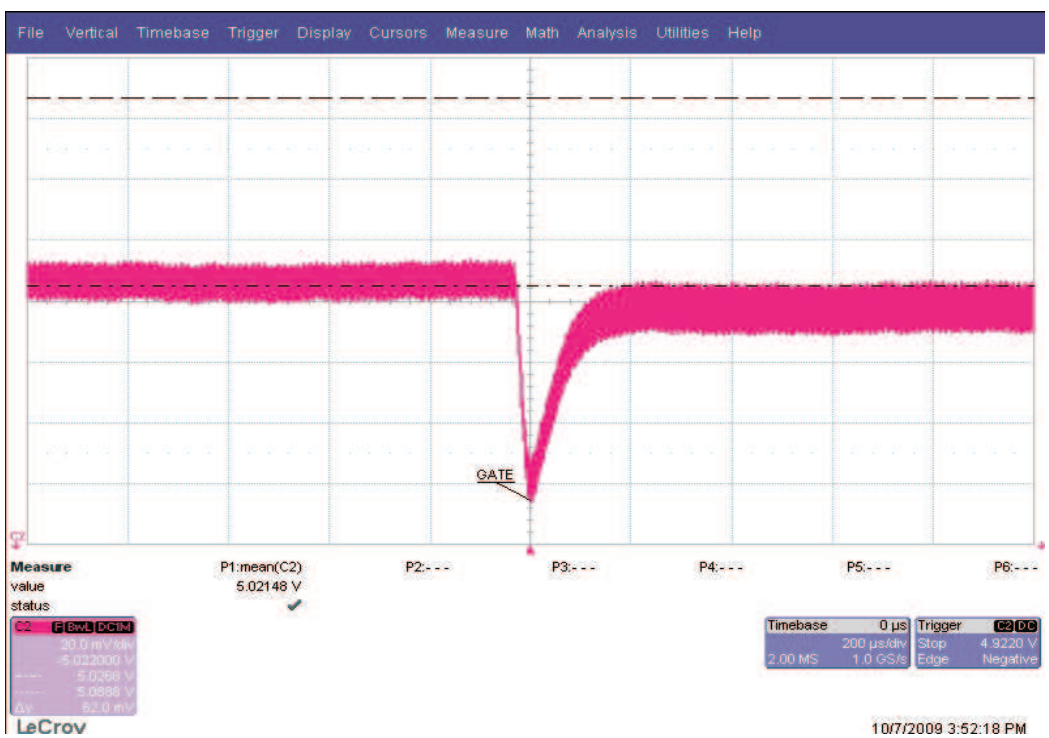


Figure 7. Loop Response of TPS5430 Tested in Laboratory (Phase Margin = 55°)



NOTE: Uses a 50% Load Step at 1-10µs Slew Rate

Figure 8. Load-Step Response of TPS5430 Tested in Laboratory (Phase Margin = 55°)

In the laboratory test of the load-step response in Figure 8, there are no oscillatory peaks. At a phase margin of 55°, this result matches what is found in Table 1.

3 Conclusion

This application report explains the link between the load-step response and the loop response of a given circuit. Based on this relationship, this document provides details to make an estimate at relative stability based on phase margin. The designer must always consider that this measurement requires some interpretation of load-step response and that these measurements can vary.

Revision History

Changes from A Revision (September 2011) to B Revision **Page**

- Changed 0 dB to 0° in 1st paragraph of Section 2 (typo) 3

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.