Application Report
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Providing Continuous Gate Drive Using a Charge Pump

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ABSTRACT

Certain applications require that output voltage regulation be maintained when the input voltage is only slightly higher than the output voltage. For a buck converter, these low headroom operating conditions require high duty cycle operation that may approach 100%. As the converter on-time duration approaches the switching period, the charge on the BOOT capacitor must be maintained in order for the high-side switch to remain on and thus continue the cycle. In some extreme cases, the BOOT capacitor may become discharged below a certain threshold; this discharge may cause high ripple currents to be present on the output. Using the TPS54240 as an example, this application report discusses the various operating modes associated with low headroom operation and outlines the design and implementation of a charge pump that allows the BOOT capacitor to remain charged beyond the time that would normally be achievable.

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1 Introduction

For a buck converter, the ideal duty cycle *D* is equal to V_{OUT}/V_{IN}. For applications where the output voltage is near the input voltage, high duty cycles are required. Many dc/dc converters limit the maximum duty cycle as a result of internal architecture constraints, usually to allow the high-side gate drive circuit to re-charge. These types of converters are not suitable for low headroom applications. Some converters, on the other hand, do not internally limit the duty cycle. As the input voltage decreases towards the output voltage, then, the duty cycle is allowed to increase in order to maintain the output voltage in regulation. As the required duty cycle approaches 100%, the on-time of the high-side switch is extended beyond the switching period time.

Typically, a buck converter uses an N-channel MOSFET as the high-side switching element. This component design requires a floating power supply above the source voltage to ensure proper drive to the gate of the FET. Because of its simplicity and fast switching time, it is common to use a bootstrap circuit to generate the supply voltage for the gate drive of the high-side FET. This method involves connecting a capacitor from the BOOT (that is, the high-side MOSFET gate drive supply) to the switching node or high-side MOSFET source pins. A BOOT regulator keeps the BOOT to switching node voltage constant to provide uniform drive capability. If the input voltage falls below this regulated level, the BOOT to switching node voltage and gate drive capability is reduced.

Although the bootstrap method has many advantages, it imposes significant limitations because of inherent charge time requirements. The capacitor can supply current to keep the high-side MOSFET on for multiple switching cycles; however, once the charge is depleted, the circuit is forced to switch for a brief period of time to recharge the capacitor. To keep the converter from attempting to switch when the gate drive may be too low, many converters include an undervoltage lock-out (UVLO) circuit for the gate drive supply. If the UVLO triggers, the high-side switching element is then prevented from switching until the BOOT charge is restored. This configuration may result in an increased level of ripple on the output voltage.

2 TPS54240 Low Headroom Operation

Consider the TPS54240 as a typical dc/dc converter that features low headroom operation. The TPS54240 is a non-synchronous buck converter that contains an integrated high-side N-channel MOSFET switch and bootstrap charging circuit as described in the introduction. The low-side switching element is an external catch diode. The input voltage range for the TPS54240 is 4.5 V to 40 V, and the rated output current is 2.5 A. The TPS54240 is non-synchronous; therefore, it may operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The TPS54240 circuit used for testing is shown in Figure 1, and the BOOT waveforms are shown in Figure 2 with a 2-A load. No external input voltage UVLO resistors are used, in order to allow operation at low input voltages without the device shutting off.

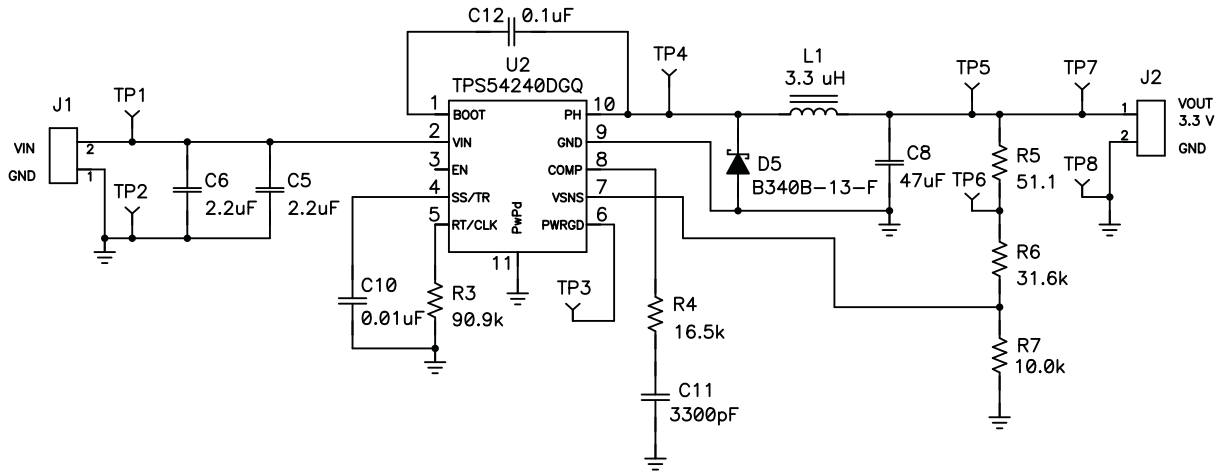

Figure 1. TPS54240 Test Configuration

2.1 Continuous Conduction Mode (CCM) Operation

Figure 2 illustrates the TPS54240 output waveforms at an input voltage of 4.36 V and a 2-A load.

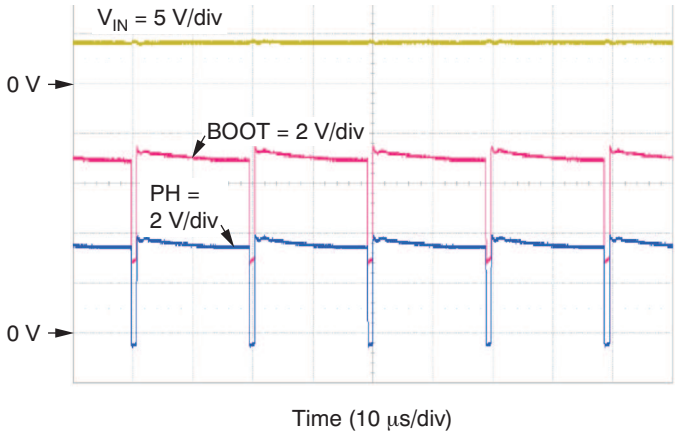

Figure 2. TPS54240 Waveforms at 4.36-V Input Voltage and 2 A

For a buck converter, as noted earlier, the duty cycle $D = V_{OUT}/V_{IN}$. As the input voltage decreases, then, the duty cycle must increase to maintain the output voltage. As the required duty cycle approaches 100%, the on-time of the high-side switch is extended beyond the switching period time. This extended on-time is seen as a decrease in the effective operating frequency. The BOOT capacitor supplies the current required to keep the high-side MOSFET on. In Figure 2, the operating frequency has been reduced to approximately 50 kHz from the nominal of 1.2 MHz. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor.

There is a limitation to maximum continuous on-time, however. The TPS54240 contains a BOOT UVLO circuit. When the BOOT to PH voltage falls below 2.1 V, the high-side switch is forced off to allow the low-side diode to conduct, which refreshes the charge on the BOOT capacitor. In CCM operation, when the high-side switch is turned off, the current in the output inductor must remain continuous. The inductor current continues to flow in the catch diode, and the diode clamps the PH node voltage at one diode drop below ground. The BOOT to PH voltage is V_{IN} + 0.7 V, and the BOOT capacitor is charged to this level. This method allows for low-dropout regulation; however, true 100% duty cycle operation cannot be obtained using this method.

2.2 No-Load Operation

When the converter operates in CCM, the PH voltage is clamped to one diode drop below ground during the high-side switch off-time, allowing the BOOT capacitor to fully charge. In non-synchronous applications operating in DCM, this condition may not be permissible. When the inductor current reaches 0 A during the high-side switch off-time, the PH node voltage is no longer clamped to one diode drop below ground. There is no current flowing in the output inductor, and therefore, there can be no voltage across the inductor. The PH node voltage will now be V_{OUT}, and the BOOT to PH voltage is ($V_{IN} – V_{OUT}$). For light load, low headroom operation, ($V_{IN} – V_{OUT}$) may be significantly less than the BOOT UVLO voltage. If the voltage across the BOOT capacitor is less than 2.1 V (the BOOT UVLO threshold), the device stops switching, and the output voltage decays.

In such a case, the output voltage must decay to (V_{IN} – BOOT UVLO) before the high-side switch can turn on, as seen in Figure 3. This configuration results in a high ripple voltage on the output.

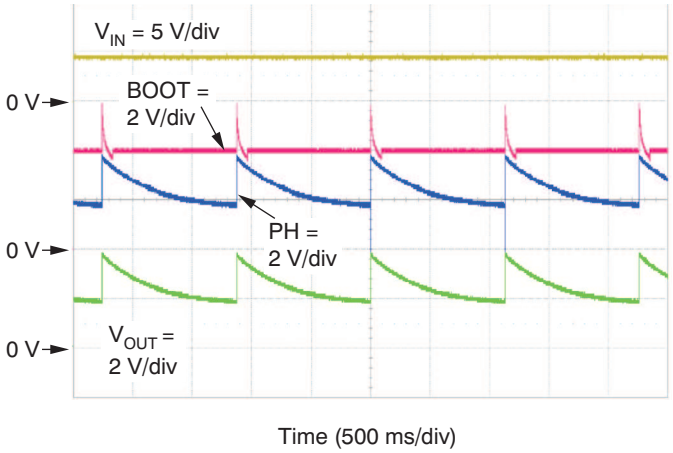

Figure 3. TPS54240 No-Load Waveforms at 4.60-V Input Voltage

The frequency of the oscillation is less than 1 Hz and decreases as the input voltage drops further. This condition persists until the input voltage and/or the load current increases.

3 Charge Pump Circuit

One recommended method to avoid the conditions discussed in Section 2.2 is to use a simple charge pump circuit to keep the BOOT capacitor continually charged. Figure 4 illustrates this type of charge pump circuit using the NE555 timer.

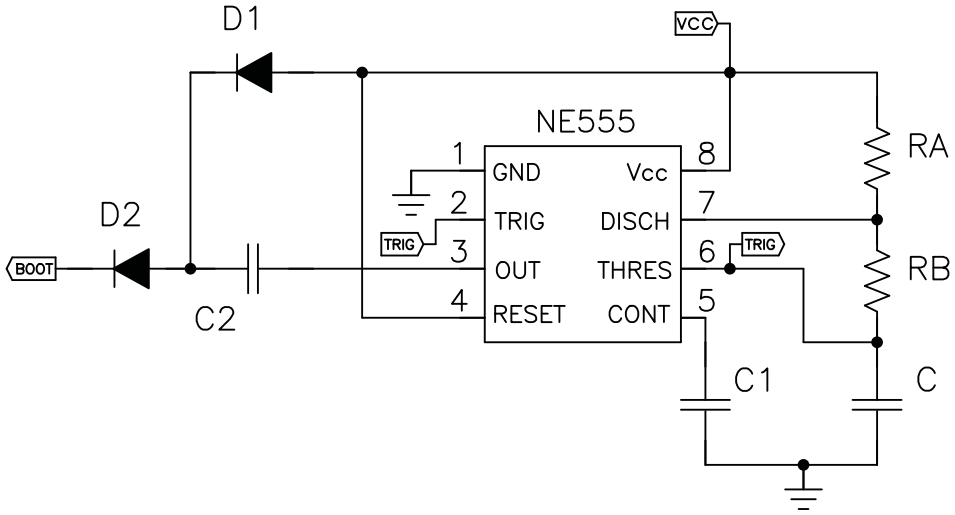

Figure 4. NE555 Charge Pump Circuit

3.1 Theory of Operation

The NE555 is configured for astable operation. The threshold and trigger inputs are tied together, which causes the timer to self-trigger and output a square wave from 0 V to V_{CC}. When the output is low, D1 is forward-biased, and the flying capacitor, C2, is charged to V_{CC} (neglecting the diode voltage drop). As the output switches high, D1 turns off and the other side of C2 is charged to V_{CC}. Because the capacitor retains the voltage that passes across it, the resulting waveform is a square wave that goes from V_{CC} to twice V_{CC} (that is, 2 × V_{CC}).

To implement this circuit into the design of a TPS54240 buck regulator, the cathode of D2 should be connected to the BOOT pin on the SWIFT™ IC. This configuration makes the BOOT capacitor a storage capacitor that smooths out the square wave and provides the current to the high-side MOSFET. Therefore, neglecting losses and diode drop, the output to BOOT is approximately 2 × V_{CC}. Additional capacitor diode stages can be added to achieve further multiples of V_{CC}.

3.2 BOOT Voltage Design

The ideal output voltage of the charge pump is (2 × V_{CC}), but this estimate does not take into account diode drops and circuit losses. Consider the voltage on the flying capacitor C2. When the output of the 555 timer is low, D1 turns on, and C2 charges to the value represented by Equation 1.

$$V_{C2} = V_{CC} - V_{D1} - 2I_{BOOT}ESR_{C2} \quad (1)$$

Where:

- V_{CC} = 555 timer input voltage
- V_{D1} = Voltage drop across diode D1
- I_{BOOT} = Charge pump output current into BOOT
- ESR_{C2} = Equivalent series resistance of flying capacitor C2

When the 555 timer goes high, D1 turns off, and the BOOT capacitor charges to the value given in Equation 2.

$$V_{BOOT} = V_{555} + V_{C2} - V_{D2} - 2I_{BOOT}ESR_{Cboot} \quad (2)$$

Where:

- V_{555} = 555 timer high level output voltage
- V_{D2} = Voltage drop across diode D2
- ESR_{Cboot} = Equivalent series resistance of boot capacitor

Substituting Equation 1 into Equation 2 gives the final equation for the BOOT voltage, shown in Equation 3. The variable *n* has been added to represent the number of charging stages.

$$V_{BOOT} = V_{CC} + n[V_{555} - V_{D1} - V_{D2} - 2I_{BOOT}(ESR_{Cboot} + ESR_{C2})] \quad (3)$$

The BOOT voltage must be greater than the BOOT UVLO threshold of 2.1 V above phase to avoid the output oscillations. However, under no-load conditions, an excessively high voltage can cause the phase voltage to rise. The phase voltage equals the output voltage; therefore, a higher than expected output voltage occurs. As a rule of thumb, the BOOT voltage should be selected based on the formula given in Equation 4.

$$2.1\ V + V_{OUT} < V_{BOOT} < 4\ V + V_{OUT} \quad (4)$$

Where:

- V_{OUT} = Output of the SWIFT dc/dc converter

3.3 Component Selection

3.3.1 Frequency and Duty Cycle

The frequency of the 555 timer can be set using Figure 5 and Equation 5.

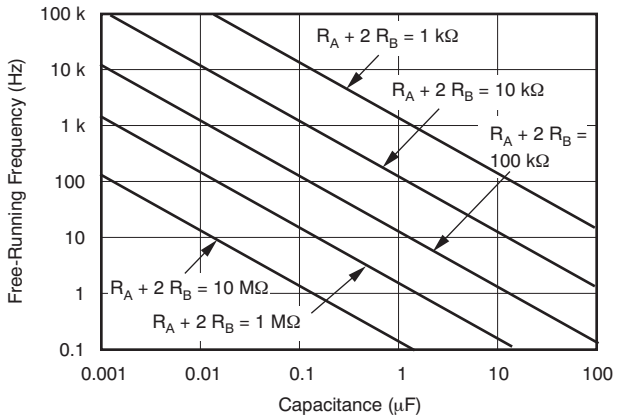

Figure 5. Free-Running Frequency of the 555 Timer

$$f = \frac{1.44}{(R_A + R_2B)C} \quad (5)$$

The optimum running frequency for a charge pump depends on many variables and affects the effective output current. Because the output current is very low, a wide range of frequencies are suitable for this application. Here, a frequency of 7.5 kHz is used because it works for most applications.

Optimum efficiency for a charge pump is achieved when the duty cycle is 50%. This duty cycle allows equal time during the two charging cycles. By setting the value of R_B to be 10 times greater than R_A, the output of the 555 timer runs approximately at 50%. The capacitor value *C* is normally chosen first because there are more standard resistor values than standard capacitor values. After choosing the capacitor, R_A and R_B can be selected by using Equation 6 and Equation 7.

$$R_B = 10R_A \quad (6)$$

$$R_A = \frac{1}{14.6 \bullet f \bullet C} \quad (7)$$

3.3.2 Diode Selection

The forward voltage drop can be minimized for higher efficiency when selecting the diodes, but it also can be selected to achieve the desired output voltage of the charge pump. Additional attention must be given to the reverse voltage rating. Keep in mind that the BOOT regulator maintains the 6.4-V BOOT to PH voltage differential when high input voltages are present. Thus, the diode should be able to withstand reverse voltages up to the input voltage plus 6.4 V.

3.3.3 Capacitor Selection

For normal charge pump applications, the capacitor selection is critical. The flying capacitor is selected based upon the load transient and required output ripple voltage. Equation 8 shows the formula for this specification and is solved for the capacitor value in Equation 9.

$$V_{RIPPLE} = \frac{D \bullet I_{BOOT}}{C \bullet f} + I_{BOOT} \bullet ESR \quad (8)$$

$$C = \frac{D \bullet I_{BOOT}}{f(V_{RIPPLE} - I_{BOOT} \bullet ESR)} \quad (9)$$

Where:

- D = 555 timer duty cycle
- C = Capacitor value
- f = 555 timer frequency

In this application, the current into BOOT is very small, and the ripple specifications minimally affect the performance of the circuit. A value for the flying capacitor C2 of 0.1 µF provides minimal load transient ripple while not being too large to affect efficiency. Additionally, a ceramic capacitor of X5R dielectric or better is recommended to reduce the effects of ESR on the ripple. The BOOT capacitor should be selected as outlined in the product data sheet.

4 Design Example

This example outlines the steps to achieve 100% duty cycle operation by adding a charge pump circuit to the TPS54240 circuit shown in Figure 1. Ideally, a separate rail should be used to power the charge pump, thus providing maximum control of the BOOT input voltage. In most cases, however, a separate rail is not available, and the input voltage must be used. The input voltage of the TPS54240 may be as high as 42 V, which would damage the 555 timer; thus, a different input voltage source for the charge pump must be found. In this example, the output voltage is 3.3 V, which is sufficient to power the 555 timer used in the charge pump.

From Equation 4, the output of the charge pump should be between 5.4 V and 7.3 V. BAV99 diodes are used for this example; these diodes, for low current, have a forward voltage drop of 0.6 V. The BOOT current is very small, and therefore the BOOT current terms in Equation 3 can be neglected. The V_{BOOT} equation may thus be reduced to Equation 10.

$$V_{BOOT} = 3.3\ V + 2[3.20\ V - 0.6\ V - 0.6\ V] = 7.3\ V \quad (10)$$

For this design example, two charge pump stages are required to achieve the required charge pump output voltage.

The frequency of the 555 timer is set to 7.5 kHz, and the capacitor *C* is chosen to be 0.01 µF. From Equation 6 and Equation 7, the values for R_A and R_B are set to 909 Ω and 9.09 kΩ, respectively. 0.1 µF is selected for the flying capacitors C2 and C4, and the additional storage capacitor C3 is chosen based on the BOOT capacitor, which is 0.1 µF.

Figure 6 illustrates the final design.

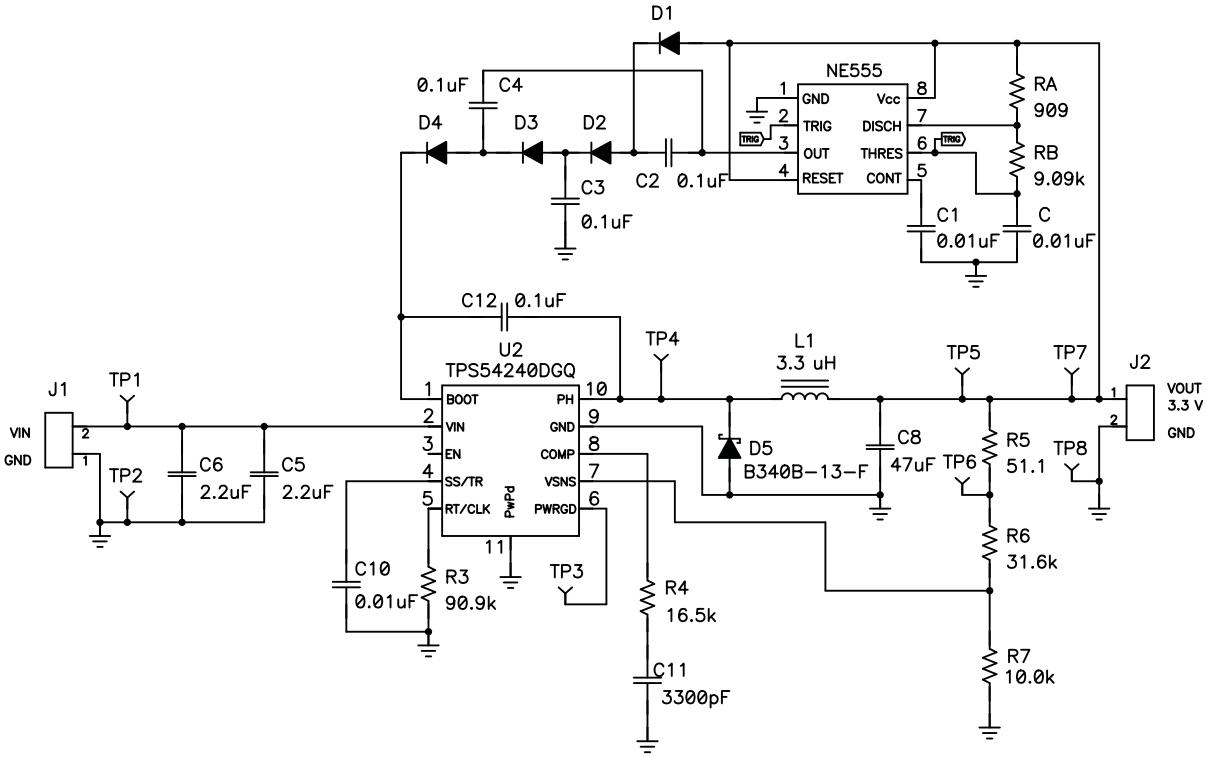

Figure 6. Charge Pump Circuit for TPS54240EVM-605

As Figure 7 shows, the addition of the charge pump circuit eliminates the large output voltage oscillations illustrated in Figure 3.

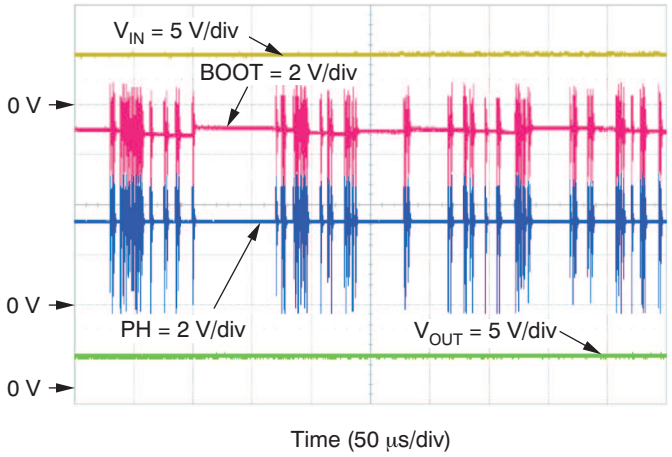

Figure 7. TPS54240 with Charge Pump at 4.6-V Input Voltage

When there is no switching, the BOOT capacitor maintains the voltage at 7.3 V. The observed ripple on BOOT is a result of the capacitor being replenished at 7.5 kHz. Also, notice that the BOOT regulator maintains the 6.4-V BOOT to PH voltage when the device starts switching. Additionally, because the evaluation module now supports 100% duty cycle operation, the input can be lowered to be nearly the same as the output voltage, and the board continues to maintain the 3.3-V output.

5 Conclusion

To allow low headroom operation, some buck converters allow the duty cycle to extend nearly to 100%. As the required on-time exceeds the switching period, the available gate drive to the high-side switch is reduced. Many converters (such as the TPS54240) use an internal BOOT circuit to supply the high-side gate driver. In some cases, with low headroom and light load, the BOOT to switching node voltage drops below the internal BOOT UVLO threshold. This condition may cause unwanted ripple voltage to appear on the output. It is possible to use a simple charge pump circuit to keep the BOOT capacitor continually charged and allow continuous operation without unwanted output voltage dropouts. In addition, the circuit provides 100% duty cycle operation, which allows regulation under extremely low headroom conditions.

6 References

Unless otherwise noted, these documents are available for download from the TI website (www.ti.com).

Johnson, S. (2010). *Design for a discrete charge pump*. Application report SLVA398A.

NE555 product data sheet. Texas Instruments literature number SLFS022H.

TPS54240 product data sheet. Texas Instruments literature number SLVSAA5.

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