Compensating the Current-Mode-Controlled Boost Converter

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ABSTRACT
This application report summarizes one method for compensating a current-mode-controlled boost. A detailed description of both the power stage and the feedback network is provided. The design procedures are explained step by step. A design example using TPS61175 is provided. Similar design steps are used for the TPS61199 as well.

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1  Simplified Small Signal Model

Figure 1 shows a simplified block diagram of a current-mode boost converter with a transconductance amplifier providing the feedback.

Figure 1. Simplified Diagram of a Current-Mode Boost Converter with $g_M$ Amplifier

With inductor current information fed back by $R_{SNS}$ (and possibly gained by factor K) as well as output voltage feedback, this boost converter's inductor and switches effectively combine into a current source driving an RC load. By removing the inductor, the small-signal, control-loop model of the power stage reduces from a two-pole system, created by $L$ and $C_{OUT}$, to a single-pole ($f_P$) system, created by $R_{OUT}$ and $C_{OUT}$. The single-pole system is easily used with Type-II compensation.

The single-pole system only holds true if the slope of the external compensation signal, $S_e$, is not too large in relation to the ramp sensed across $R_{SENSE}$, $S_n$ or the natural slope. If the $S_e$ slope dominates $S_n$, for example, when the inductance is oversized in order to give ripple current much smaller than the recommended 0.2-0.4 times the average input current, then the converter begins behaving more like a voltage-mode converter and the full model, included in Appendix A, must be used.

Regardless of which model is used, the right-half-plane zero ($f_{RHPZ}$), created by lack of continuous current flow to the output, is still present.

Including the slope compensation, the new power stage small-signal model is presented mathematically as follows:

$$G_{FS}(S) = \frac{R_{OUT}}{2} \cdot (1 - D) \cdot \frac{S}{2\pi \cdot f_{ESR}} \cdot \frac{1}{1 + \frac{S^2}{2\pi \cdot f_p}} \cdot \frac{S}{2\pi \cdot f_{RHPZ}} \cdot He(s)$$

(1)

Where $D$ is the duty cycle and the single pole is:

$$f_p = \frac{2}{2\pi \cdot R_{OUT} \cdot C_{out}}$$

(2)

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_{out}}$$

(3)
For a boost converter having multiple, identical output capacitors in parallel, simply combine the capacitors and ESR in parallel and use the result in Equation 2 and Equation 3. For boost converters with ceramic capacitor(s) in parallel with a much larger, high-ESR capacitor, use the total capacitance in parallel for \( C_{OUT} \) in Equation 2 but only use the high-ESR capacitor’s capacitance and ESR for Equation 3.

The right-hand plane zero is:

\[
f_{RHPZ} = \frac{R_{out}}{2\pi \cdot L} \cdot \left( \frac{V_{IN}}{V_{out}} \right)^2
\]

Equation (4)

He(s) models the inductor current sampling effect as well as the slope compensation effect on the small-signal response.

\[
He(s) = \frac{1}{s \cdot [(1 + \frac{Se}{Sn}) \cdot (1 - D) - 0.5] + \frac{s^2}{f_{SW}^2}}
\]

Equation (5)

The equation for Se is unique to each IC and is found in the IC’s datasheet. Equation 6 gives the typical equation for Sn regarding a peak current mode converter.

\[
S_n = \frac{V_{IN}}{L} \cdot R_{SNS}
\]

Equation (6)

The natural slope may change for other types of current mode converters.

Figure 3 in the design example section shows a bode plot of a typical CCM boost converter power stage, assuming the ESR pole is at a very high frequency.

Equation 7 shows the equation for feedback resistor network and the error amplifier.

\[
H_{EA} = G_{EA} \cdot R_{EA} \cdot \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \cdot \frac{1 + \frac{S}{2\pi \cdot f_z}}{(1 + \frac{S}{2\pi \cdot f_{p1}}) \cdot (1 + \frac{S}{2\pi \cdot f_{p2}})}
\]

Equation (7)

Where \( G_{EA} \) and \( R_{EA} \) are the error amplifier’s transconductance and output resistance.

\[
f_{p1} = \frac{1}{2\pi \cdot R_{EA} \cdot C_{C1}}
\]

Equation (8)

\[
f_{p2} = \frac{1}{2\pi \cdot R_{C} \cdot C_{C2}} \text{ (Optional)}
\]

Equation (9)

\( C_{C2} \) is optional and is modeled as 10-pF stray capacitance.

and

\[
f_z = \frac{1}{2\pi \cdot R_{C} \cdot C_{C1}}
\]

Equation (10)

Figure 4 in the design example shows a typical shape of a bode plot for transfer function \( H_{EA}(s) \) with Type-II compensation components.
Design Steps

2 Design Steps

The steps to compensate the loop are as follows:

1. Choose the desired loop crossover frequency, fc

   The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is and, therefore, the lower the output voltage droops during a step load. It is generally recommended that the loop-gain crossover point is no higher than the lower of either 1/5 of the switching frequency, fSW, or 1/3 of the RHPZ frequency, fRHPZ. It is also recommended to cross over at a frequency where the power stage gain is decreasing at approximately a -20 dB/decade slope (after the dominant pole and well before the effects of an RHPZ).

   The size of the output capacitor plays a significant role in how wide the loop bandwidth is. Once the minimum capacitance is met, meeting the output ripple specification, Equation 11 is used to estimate the capacitance needed to meet the application’s load transient requirement for the maximum voltage dip (VTRAN) after a given load step (ΔI.TRAN).

   \[ C_{out} = \frac{\Delta I_{TRAN}}{2\pi \times f_c \times V_{TRAN}} \]  

2. Properly size the compensation resistor, Rc

   By placing fZ below fC, for frequencies above fC, Rc | RREA ≈ RC and so RC \times GEA sets the compensation gain. Setting the compensation gain, KCOMP-dB, at fC, results in the total loop gain, T(s) = Gps(s) \times HEA(s) \times He(s) being zero at fC. Therefore, to approximate a single-pole roll-off up to fP2, rearrange Equation 12 to solve for RC so that the compensation gain, KCOMP-dB, at fC is the negative of the gain, KPW-dB, read at frequency fC for the power stage bode plot or more simply

   \[ K_{COMP-dB}(f_c) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-dB}(f_c) \]  

3. Properly size the compensation capacitor, Cc1

   Compensation capacitor Cc1 is sized so that fZ ≈ fC/10 and optional fP2 > fC × 10

4. Optionally, size the compensation capacitor, Cc2.

   Equation 9 is for a pole produced by RC and Cc2. This pole may be necessary to ensure that the gain continues to roll off after the crossover frequency. Alternatively, for boost circuits with high ESR output capacitors, and therefore a low-frequency ESR zero per Equation 3, this pole is useful for canceling unhelpful effects of the ESR zero.

   The preceding steps lead to a loop with a phase margin near 45 degrees. Lowering RC, while keeping fZ ≈ fSW/10, increases the phase margin without significantly changing the gain and therefore increases the time it takes for the output voltage to settle following a step load.
3 Design Example using the TPS61175

Figure 2 shows the EVM schematic and Table 1 gives the specifications for the design example. In order to meet the transient requirement, the output capacitance value may need to changed.

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<td>µs</td>
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Equation 13 and Equation 14 give $S_n$ and $S_e$ for the TPS61175.

$$S_n = \frac{V_{IN} \cdot R_{SNS}}{L} = \frac{12V \cdot 40m\Omega}{22\mu H}$$ (13)

$$S_e = \frac{0.32V}{16 \cdot (1 - D) \cdot 6 \cdot pF} + \frac{0.5uA}{6 \cdot pF}$$ (14)

Where $R_{SNS}$ is the frequency setting resistor.

1. Choose the desired loop crossover frequency, $f_c$.

One fifth of the switching frequency is
Design Example using the TPS61175

\[
\frac{f_{SW}}{5} = \frac{750kHz}{5} = 150kHz
\]

(15)

\( f_{RHPZ} \) is calculated using Equation 4

Where:

\[
R_{OUT} = \frac{V_{OUT}}{I_{OUT}} = \frac{24V}{1.2A} = 20\Omega
\]

(16)

From Equation 4

\[
f_{RHPZ} = \frac{20}{2\pi * 22\mu H} * \left(\frac{12V}{24V}\right)^2 = 36.2kHz
\]

(17)

one-third of \( f_{RHPZ} \) is

\[
f_{RHPZ} = \frac{36.2kHz}{3} = 12.1kHz
\]

(18)

thus, try \( f_c = 10kHz \).

2. Find the output cap value using Equation 11

\[
C_{out} = \frac{\Delta I_{TRAN}}{2\pi * f_c * V_{TRAN}} = \frac{350mA}{2\pi * 10kHz * 500mV} = 11.14\mu F
\]

(19)

Three 4.7 µF capacitors in parallel yield a total of 14.7 µF for the output capacitance (C8, C9, and C11 in Figure 2)

3. Properly size the compensation resistor, \( R_c \) (R3 in Figure 2). Using MathCAD, plot the power stage, \( G_{PS}(s) \), with \( R_{SENSE} = 40\ m\Omega \) (given in the datasheet)

from Equation 2

\[
f_p = \frac{2}{2\pi * R_{OUT} * C_{out}} = \frac{2}{2\pi * 20\Omega * 3 * 4.7\mu F} = 1.1kHz
\]

(20)

From Equation 4, \( f_{RHPZ} \) is 36.2 kHz. Neglecting the ESR zero produced by the ceramic output capacitors gives the plot found in Figure 3.

3. Properly size the compensation resistor, \( R_c \) (R3 in Figure 2). Using MathCAD, plot the power stage, \( G_{PS}(s) \), with \( R_{SENSE} = 40\ m\Omega \) (given in the datasheet)

\[K_{COMP-db}(f_c) = 20\log(G_{EA} * R_c * \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-db}(f_c) \Rightarrow
\]

(21)

Figure 3. Simulated Bode Plot of Power Stage Gain and Phase

The crossover frequency, \( f_c \), was chosen as 10 kHz and from Figure 3, \( K_{PW} (10kHz) = 22\ dB \). With \( R_{TOP} = 301\ k\Omega \), \( R_{BOT} = 16.2\ k\Omega \) (R1 and R2 respectively in Figure 2), and \( G_{EATYP} = 340\ \mu mho \), solving Equation 12 for \( R_c \) gives:

\[K_{COMP-db}(f_c) = 20\log(G_{EA} * R_c * \frac{R_{BOT}}{R_{BOT} + R_{TOP}}) = -K_{PW-db}(f_c) \Rightarrow
\]
4. Properly size the compensation capacitor, $C_{C1}$ (C4 in Figure 2).

Solving Equation 10 for $C_{C1}$ and setting $f_z = f_c / 10 = 1$ kHz gives

$$C_{C1} = \frac{1}{2\pi * R_C * f_z} = \frac{1}{2\pi * 4.57k\Omega * 1kHz} = 34.82\, nF \Rightarrow 33\, nF$$

(23)

5. Optionally, size the compensation capacitor, $C_{C2}$ (C5 in Figure 2)

A stray capacitance of 10 pF is assumed for C5.

Figure 4 displays the plot for the Type II compensated amplifier and Figure 5 shows $T(s) = G_{PS}(s) \times H_{EA}(s) \times H_e(s)$ with $R_C$ ($R_3$) reduced to 3.09 kΩ, getting closer to the desired 60 degree phase margin.

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**Figure 4. Simulated Bode Plot of the Type II Compensation (Including Feedback Network) for a $g_m$ Error Amplifier**

**Figure 5. Modeled Bode Plot of the Total Open Loop**
As Figure 6 shows, the measured loop compares favorably with the simulated loop.
Appendix A Additional Data

\[ G_{id}(s) = \frac{2V_o^3}{V_{in}^2} \left( 1 + \frac{R_O C_O s}{2} \right) \]
\[ + \frac{V_o^3}{V_{in}^2} \frac{L}{s} + \frac{V_o^3 L C_O}{V_{in}^2} \frac{1}{s^2} \]

Where:

\[ G_{PS}(s) = \frac{V_e}{V_c} = \frac{F_m G_{vd}(s)}{1 + F_m R_{SENSE} H_e(s) G_{id}(s) - F_m K_r G_{vd}(s)} \]

\[ F_m = \frac{1}{(S_e + S_n) T_s} \]

\[ G_{vd}(s) = \frac{V_o^2}{V_{in}^2} \left( 1 - \frac{V_o^2 L}{V_{in}^2 R_O s} \right) \left( 1 + \frac{V_o^2 L}{R_E S C_O s} \right) \]
\[ + \frac{V_o^2 L}{V_{in}^2 R_O} \frac{s}{s^2} + \frac{V_o^2 L C_O}{V_{in}^2} \frac{1}{s^2} \]

\[ H_e(s) = 1 - \frac{T_s}{2} s + \frac{T_s}{\pi^2} s^2 \]

Figure 7. Full Model Diagram

A.1 References


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