

## **Fault Tree Analysis (FTA)**

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Automotive Products

### ABSTRACT

ASIC level FTA used in automotive applications in cabin temperature environment. FTA analysis completed from perspective of fault(s) causing hazard regardless of time when fault(s) occur. This could be from time  $t = 0$  onward.

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**ABBREVIATIONS**

AMP	Amplifier
BG	Bandgap
BVDSS	Drain Source Breakdown Voltage
BW	Bond Wire
COMP	Comparator
EPB	Electronic Park Brake
IDDQ	Quiescent Supply Current
OVST	Over Voltage Stress Test
PT	Production Test
PTAT	Proportional to Absolute Temperature
REF	Reference
REG	Regulator
S/C	Short Circuit
SOA	Safe Operating Area
URA	Unintended Relay Actuation
V5AOV	V5A Regulator Over Voltage
V5OV	V5 Regulator Over Voltage

**1 References**

SLVS726 - 3-V TO 6-V INPUT, 6-A OUTPUT SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™) - January 2007 (<http://www.ti.com/lit/gpn/tps54610-q1>)

## 2 Diagrams

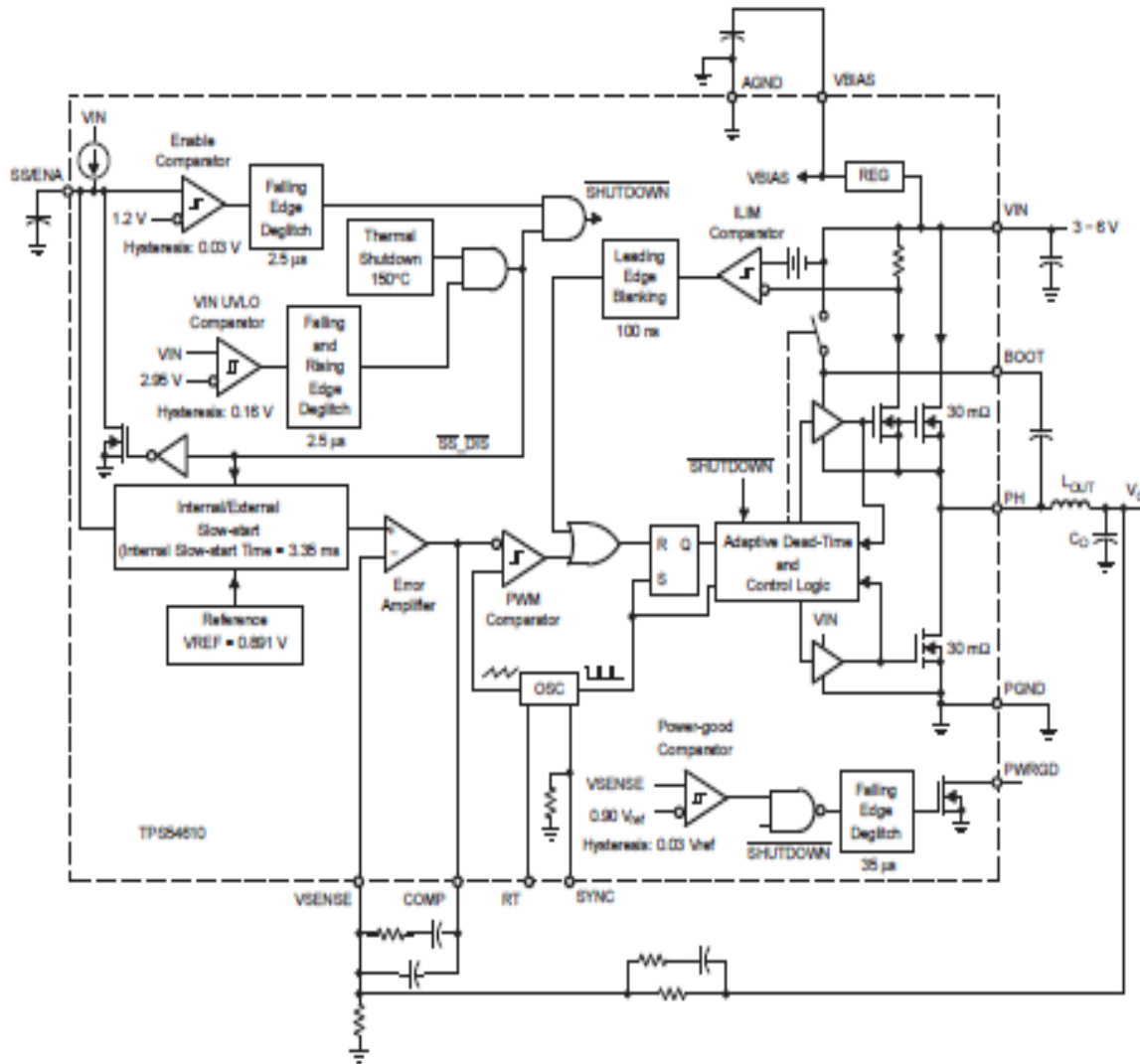


Figure 1. Device Block Diagram

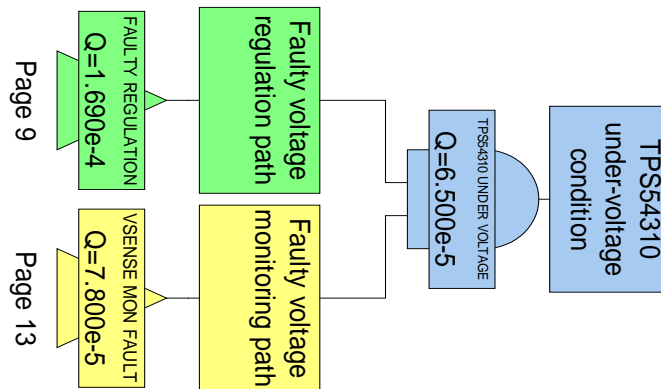


Figure 2. TPS54310-Q1 Undervoltage Fault Tree

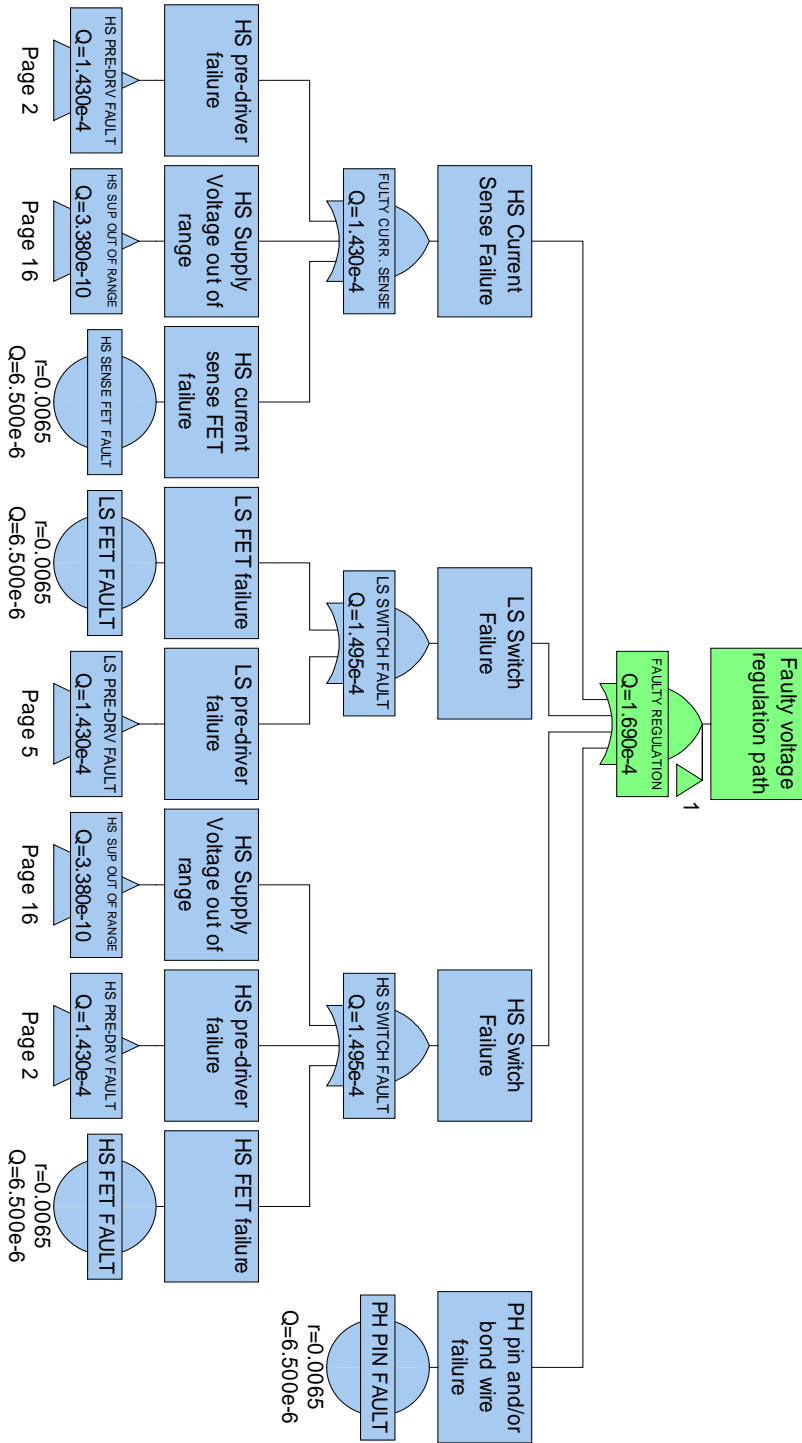


Figure 3. Faulty Regulation Fault Tree

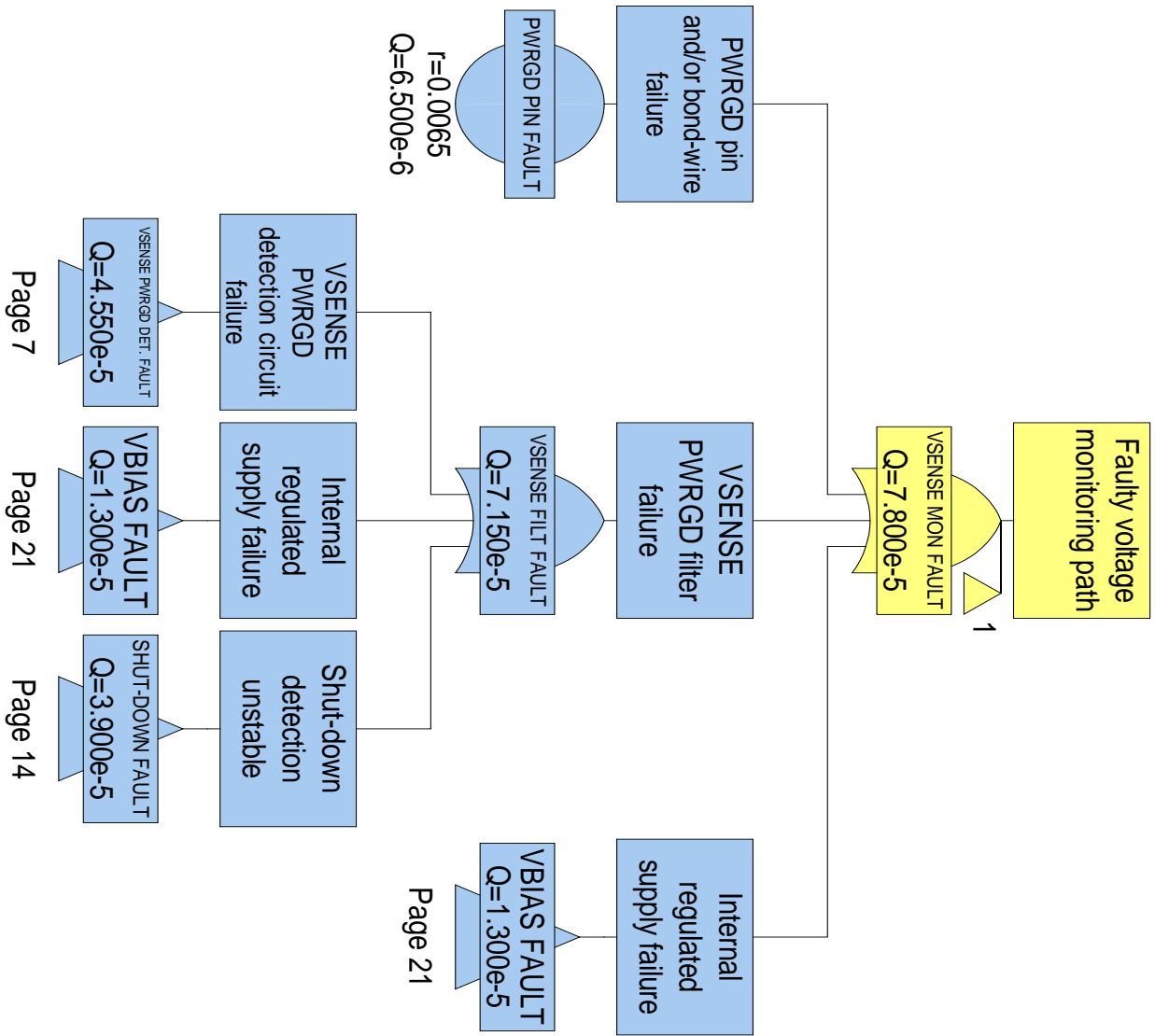


Figure 4. Faulty Voltage Monitoring Fault Tree

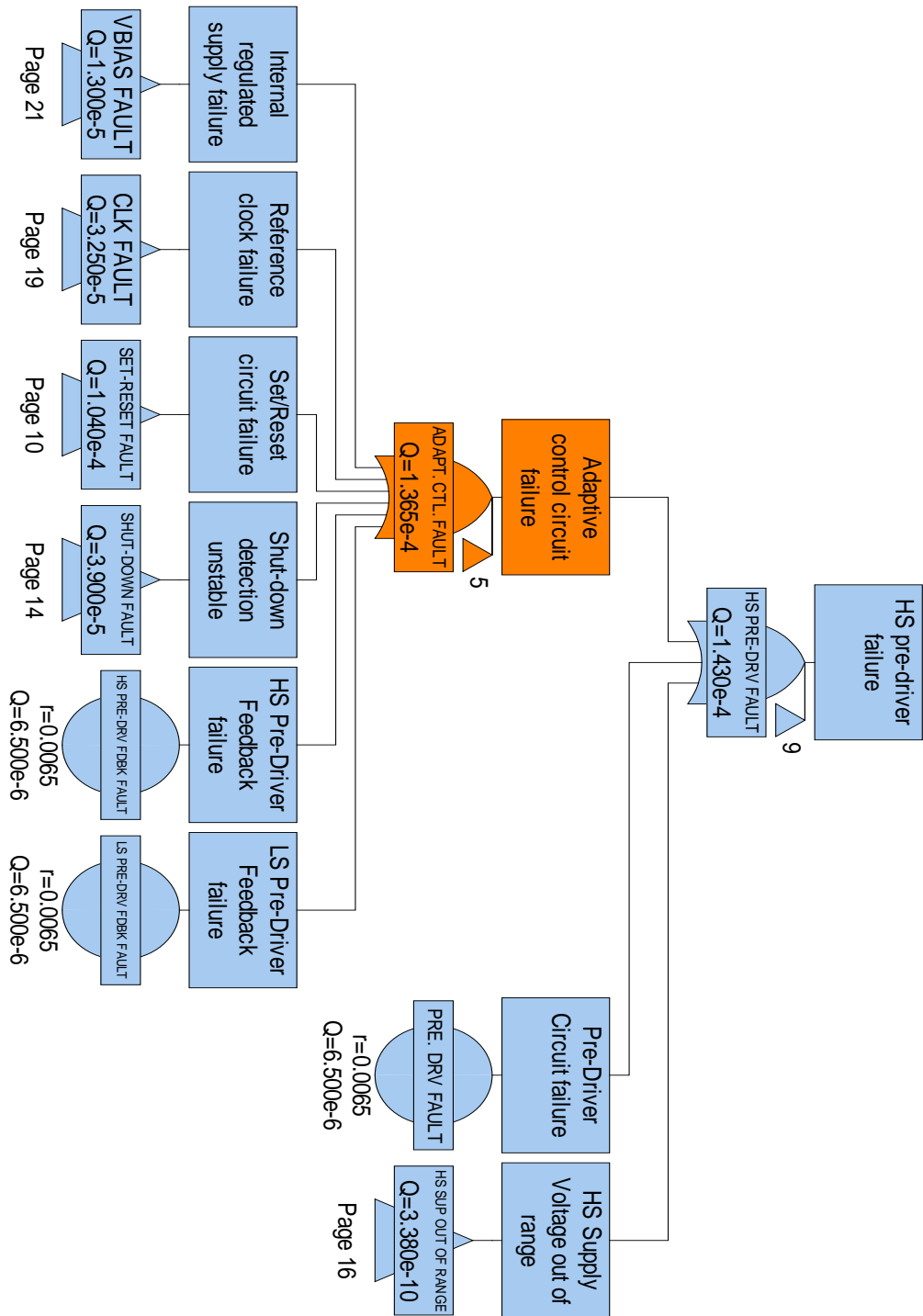


Figure 5. HS Pre-Driver Failure Fault Tree

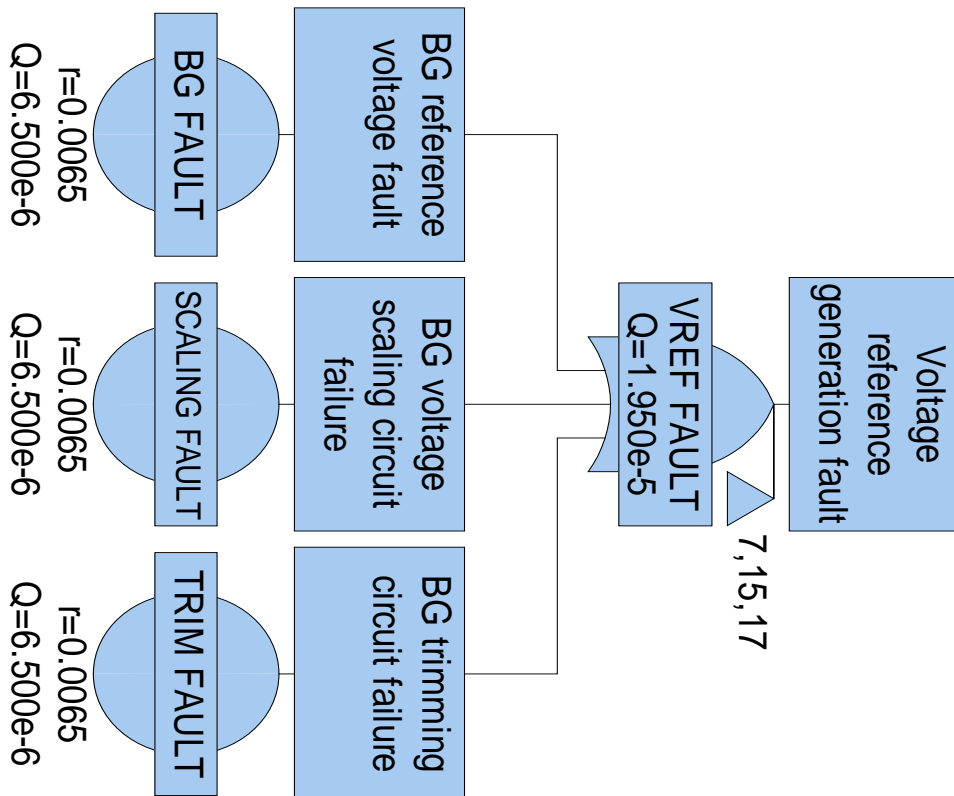


Figure 6. Voltage Reference Failure Fault Tree



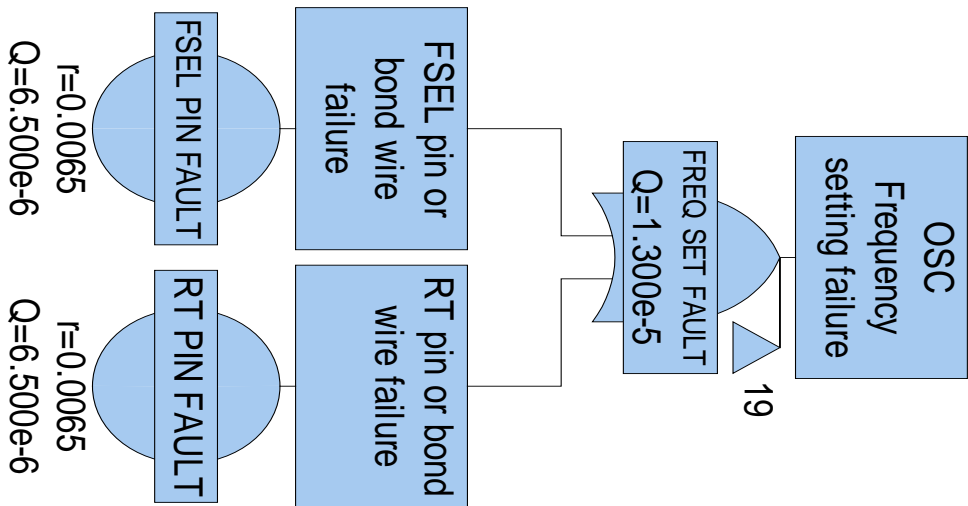


Figure 7. OSC Frequency Setting Failure

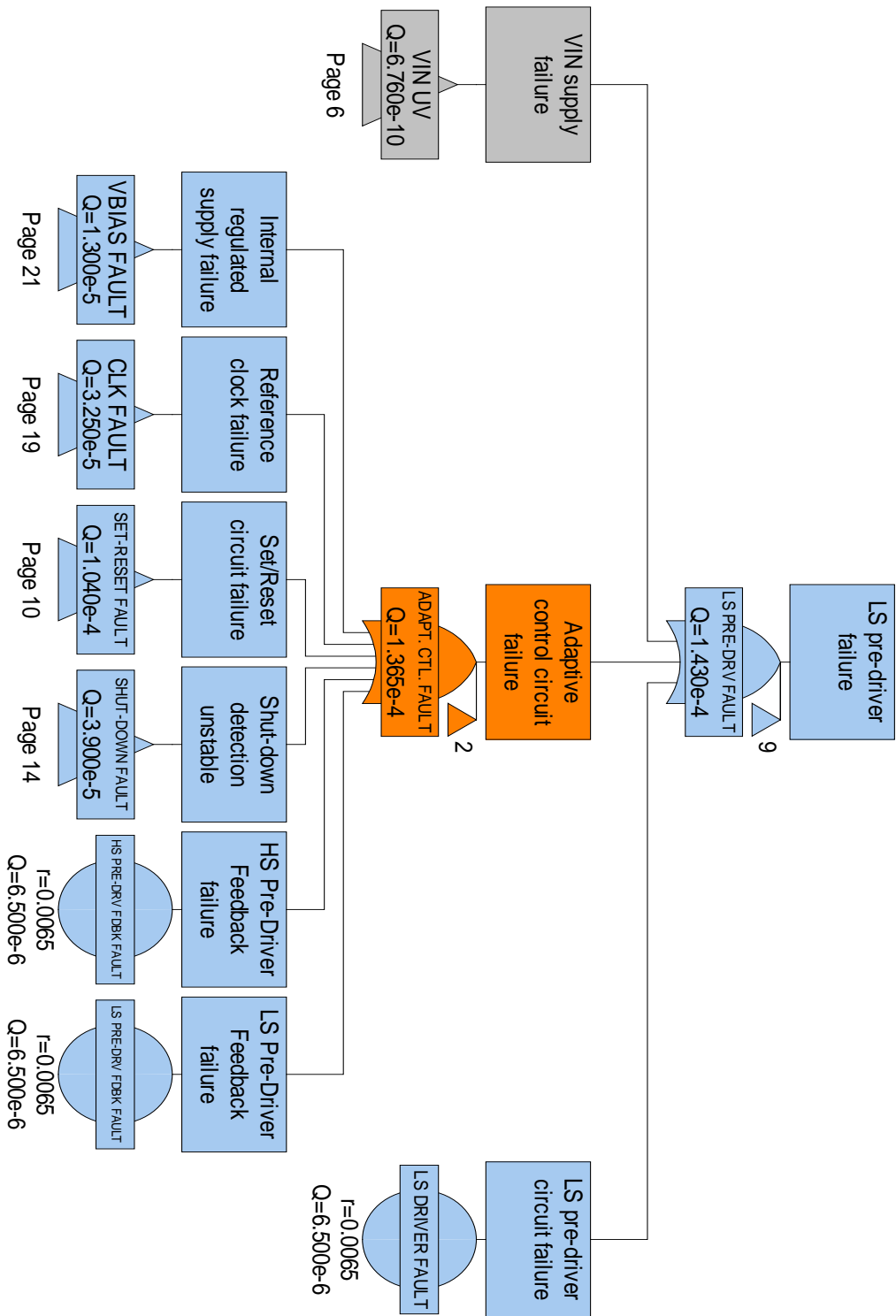
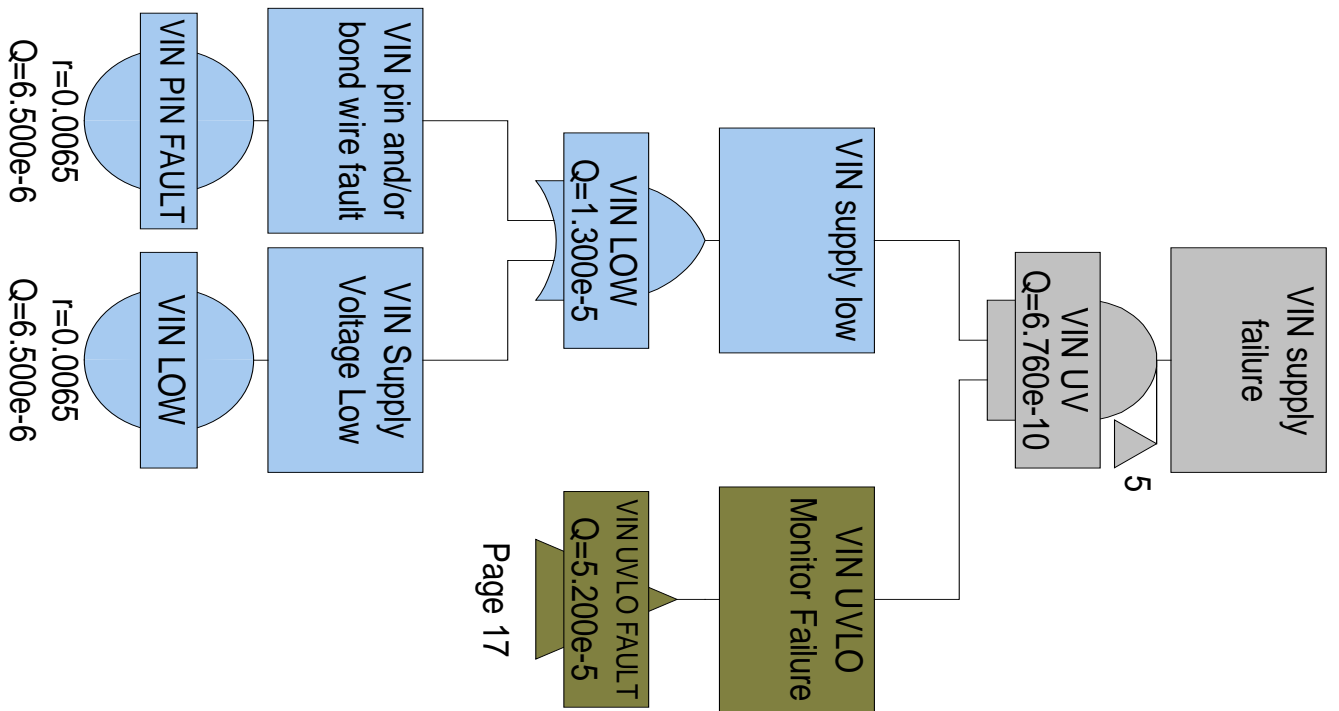


Figure 8. LS Pre-Driver Failure Fault Tree



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Figure 9. VIN Failure Fault Tree

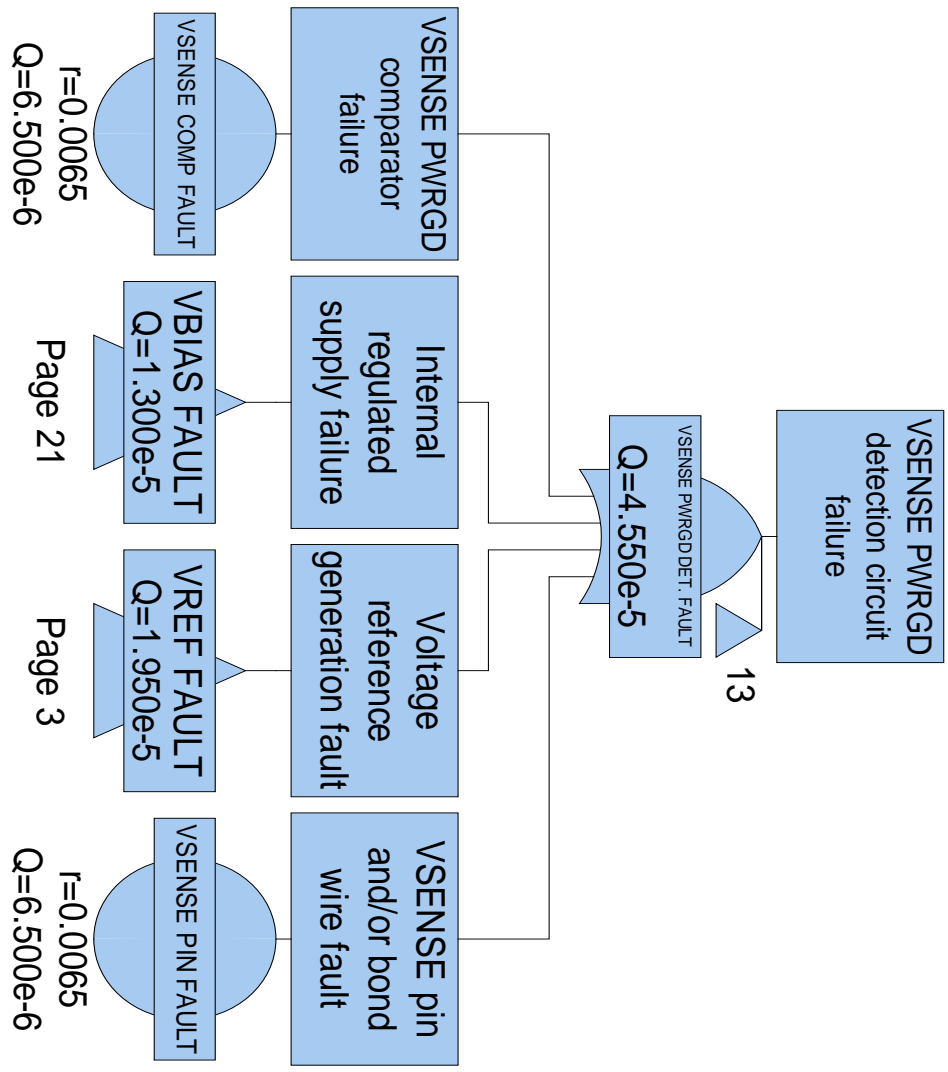


Figure 10. VSENSE Power Good Detection failure fault tree

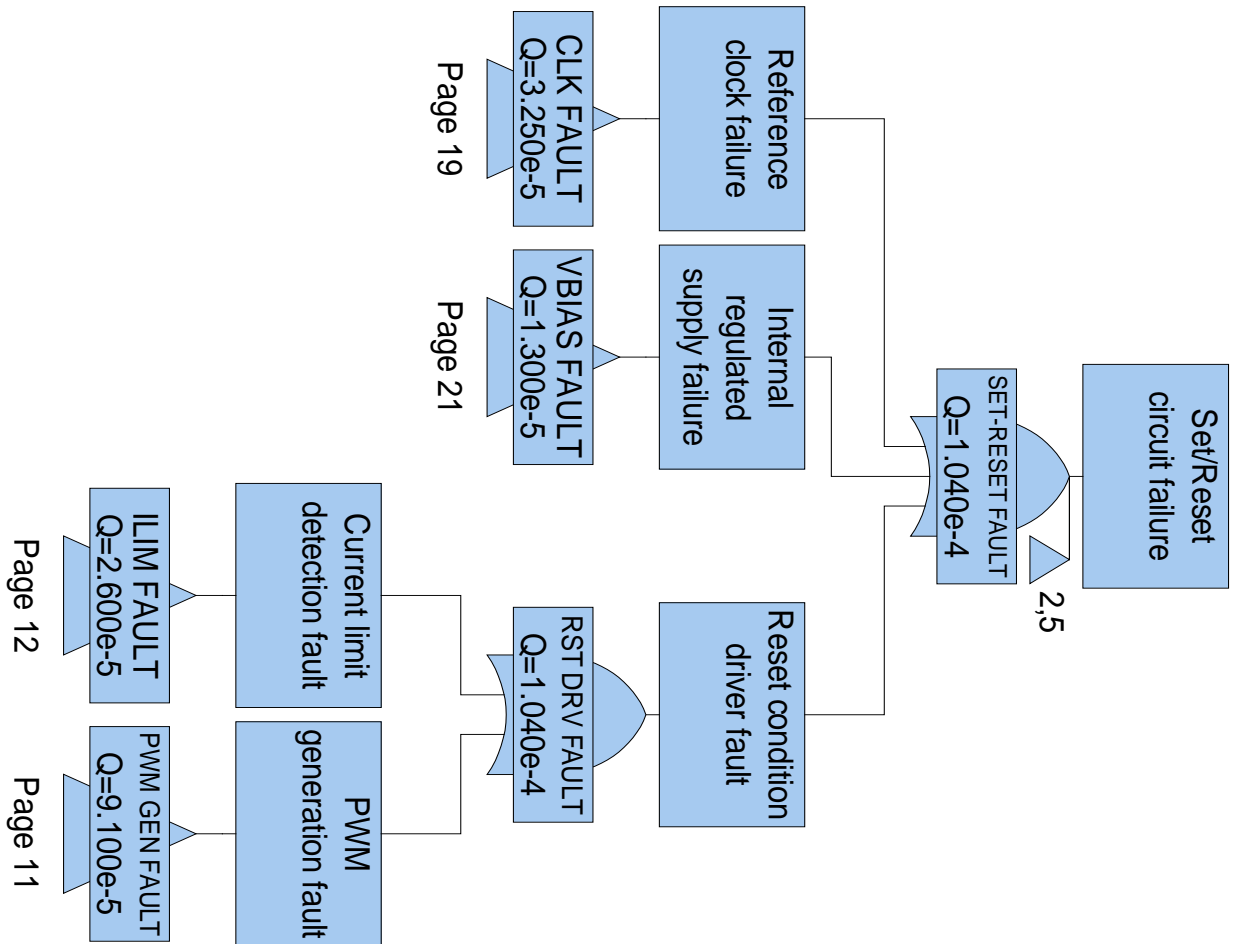


Figure 11. Set/Reset Circuit Failure fault tree

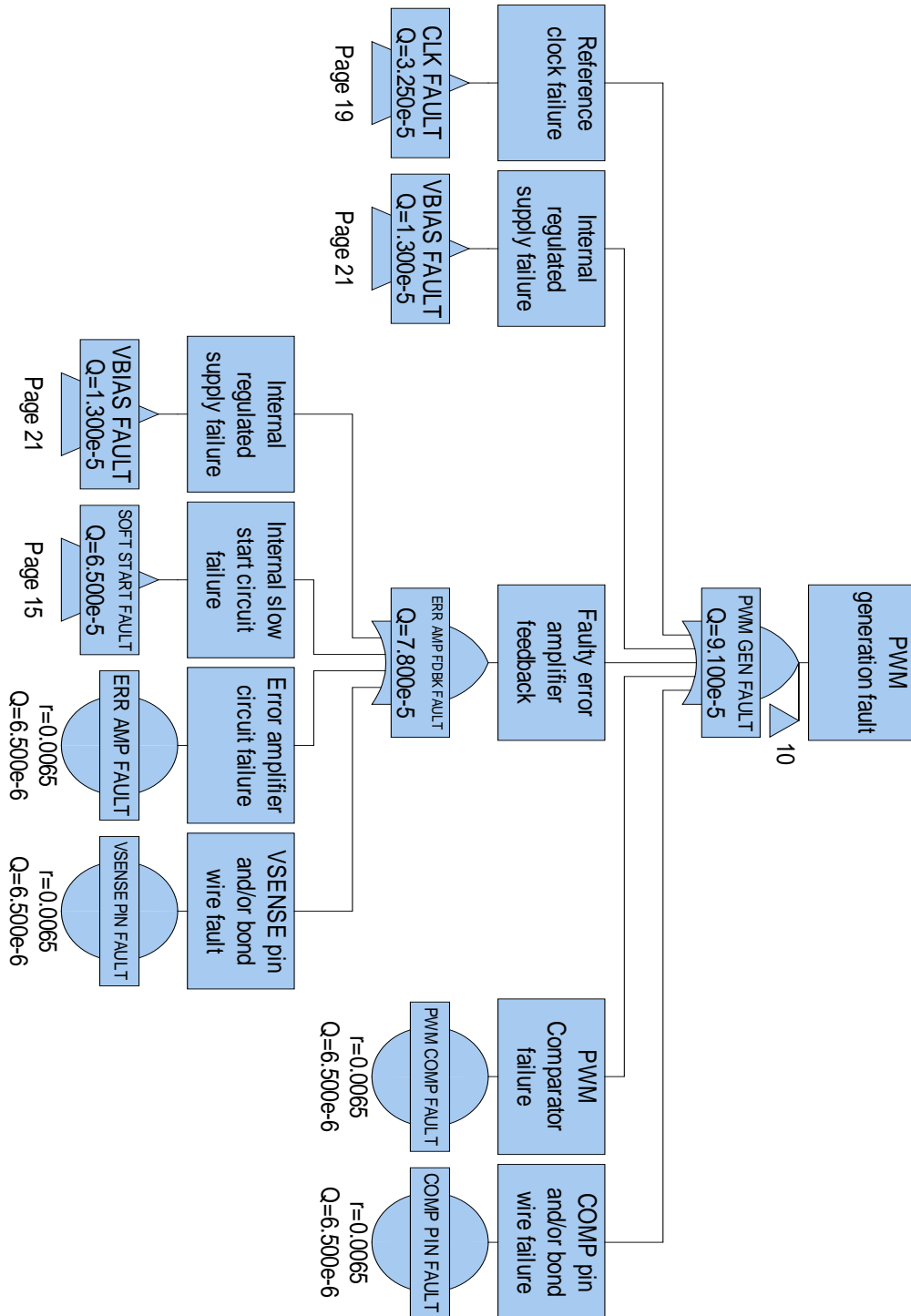


Figure 12. PWM Generation failure fault tree

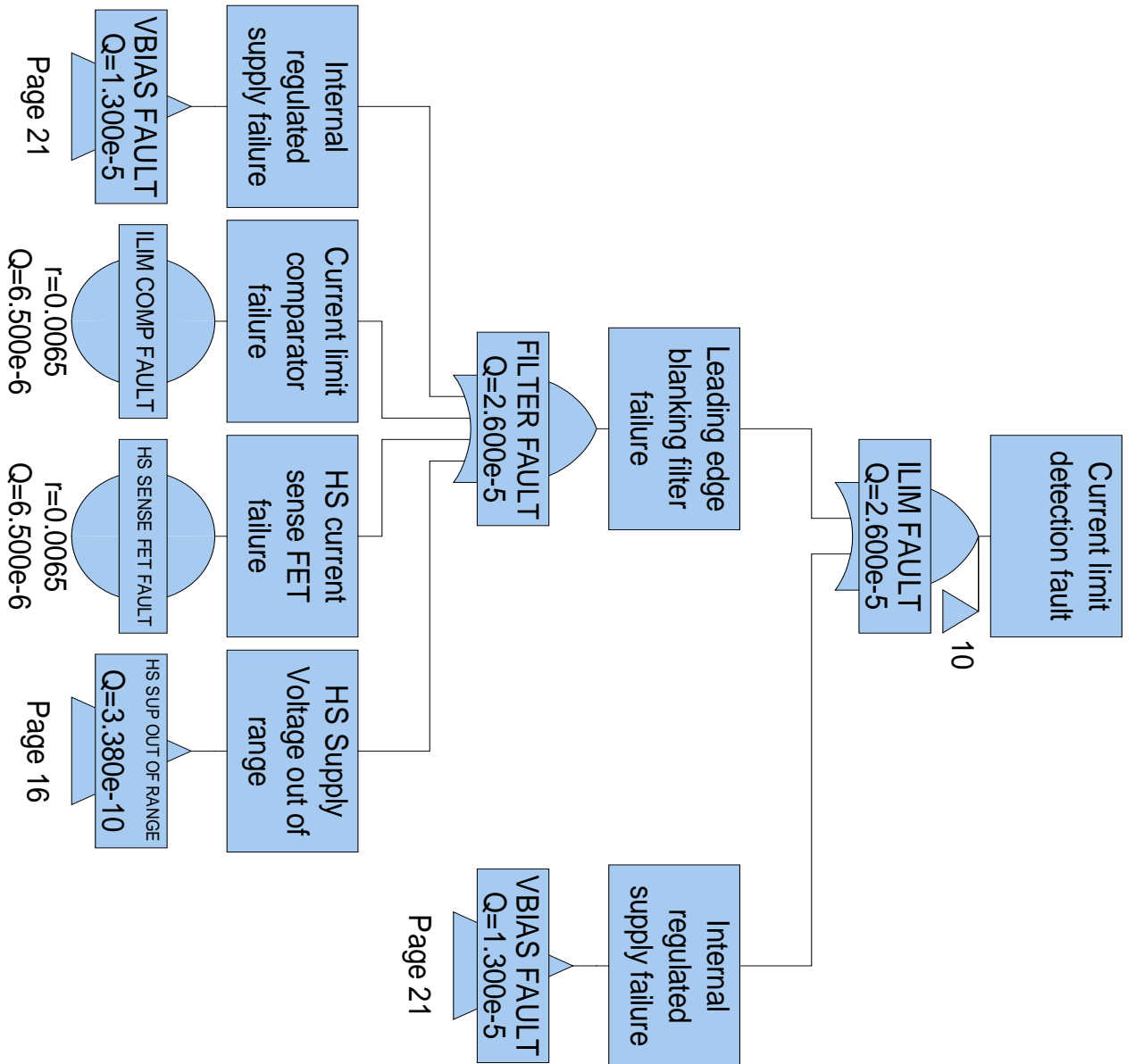


Figure 13. Current Limit Detection failure fault tree

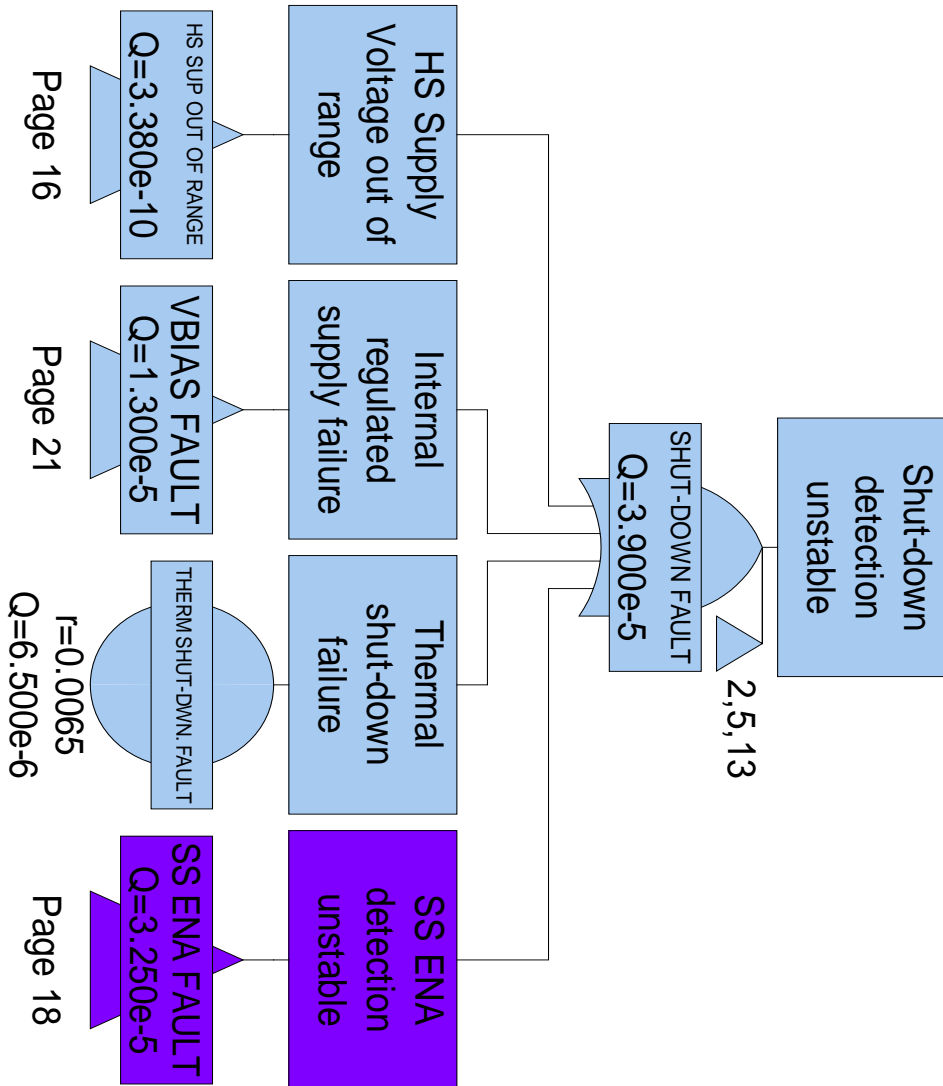


Figure 14. Shutdown Detection failure fault tree



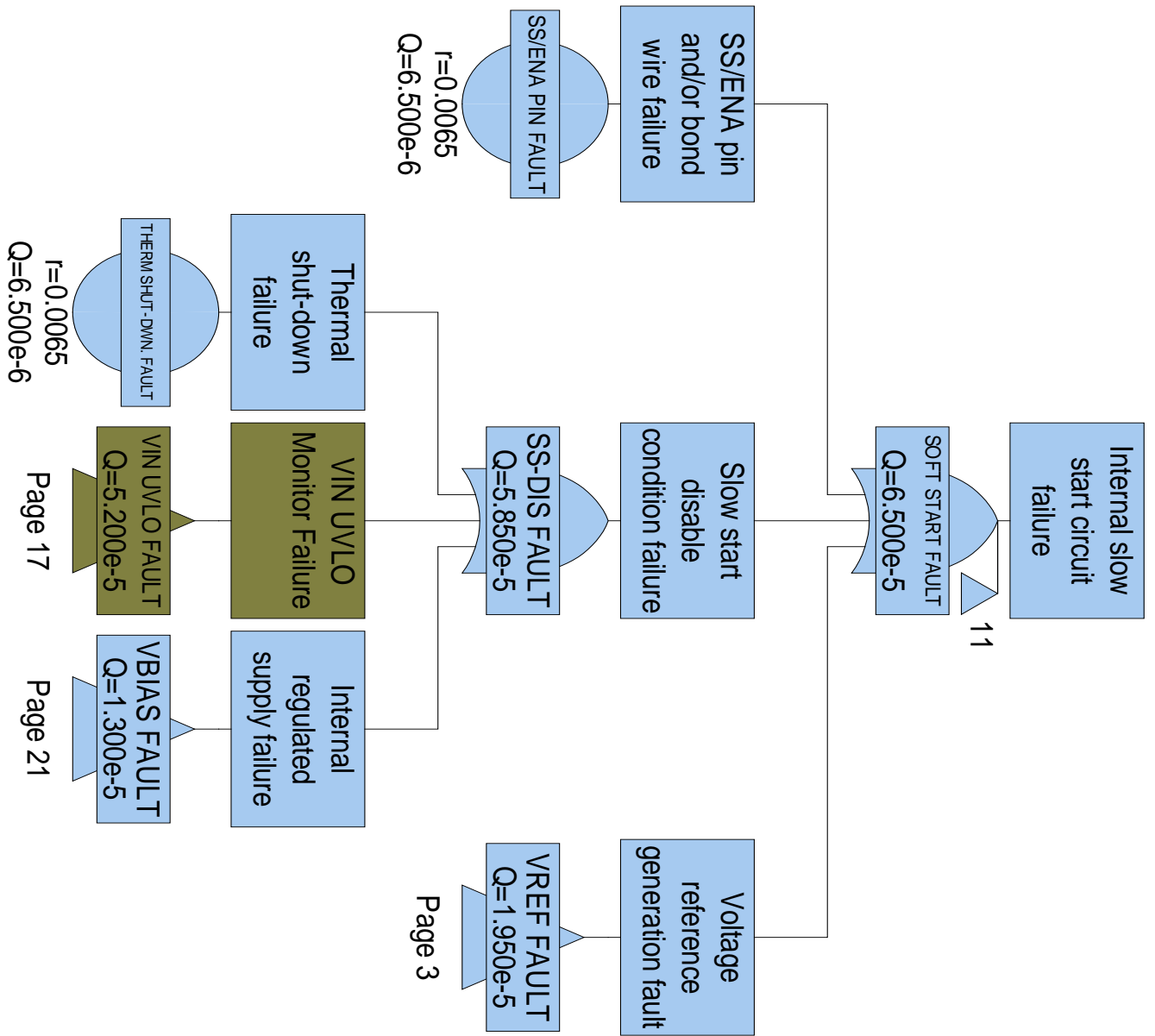


Figure 15. Slow Start failure fault tree

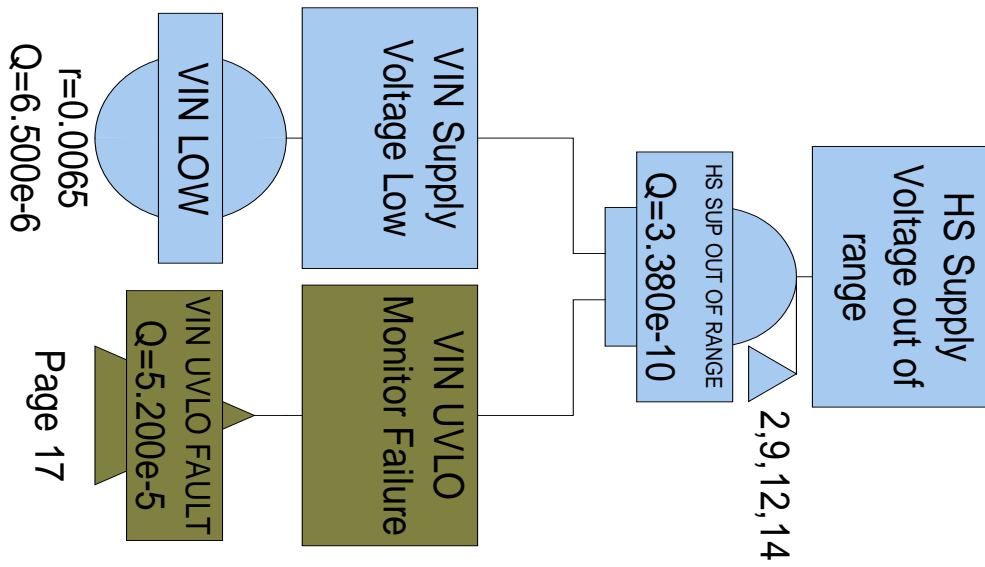
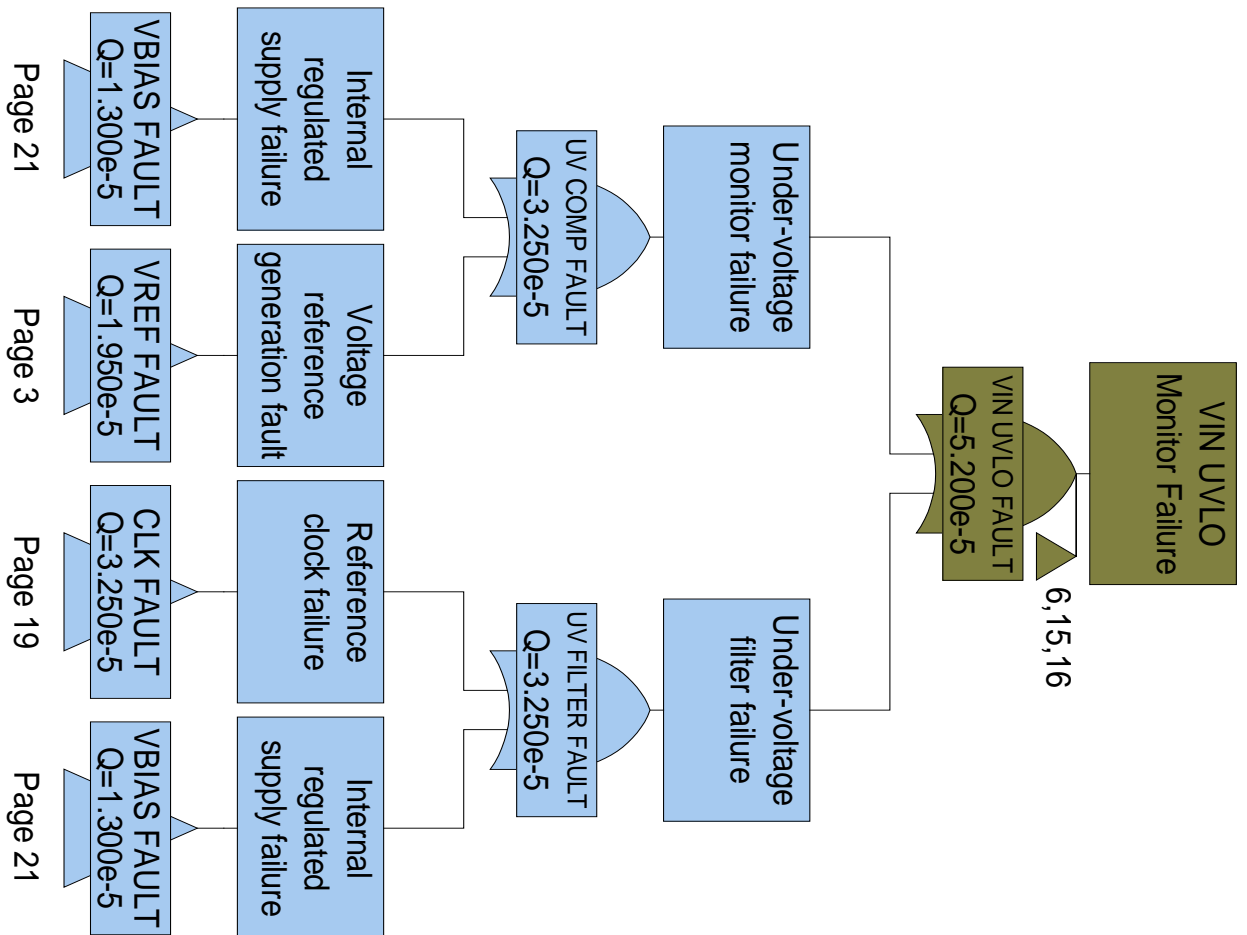


Figure 16. High Side Supply failure fault tree



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Figure 17. VIN Undervoltage Lockout failure fault tree

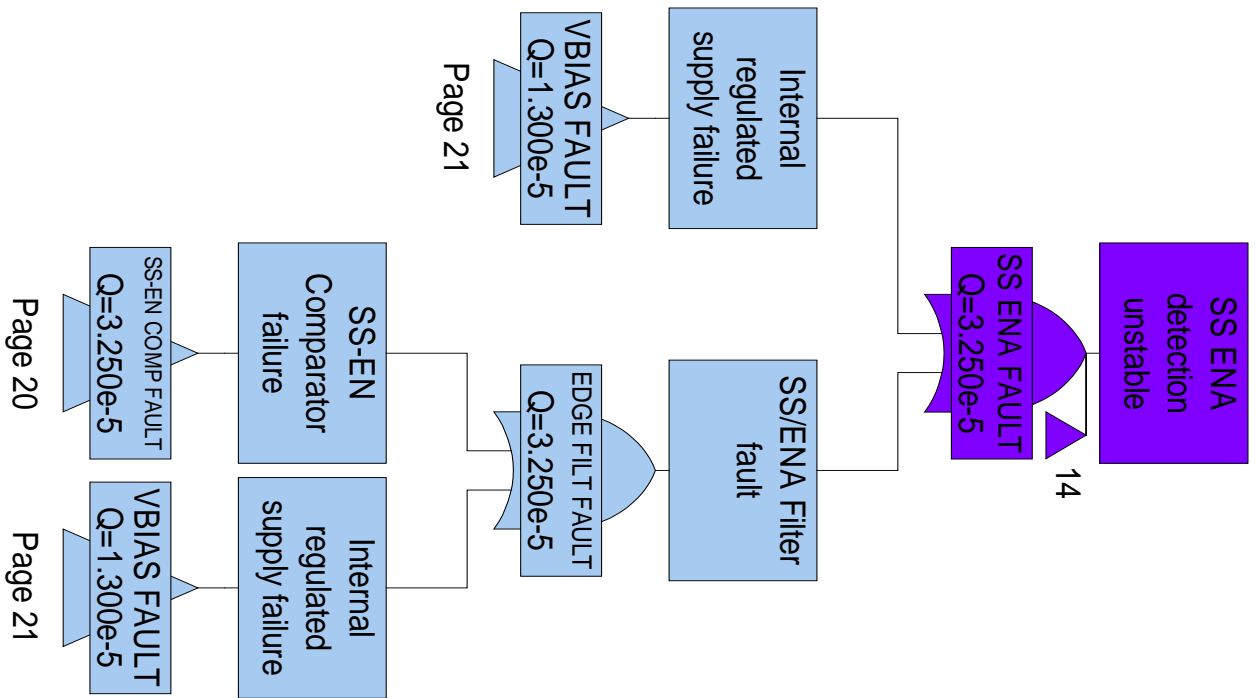


Figure 18. SS/ENA Detection failure fault tree

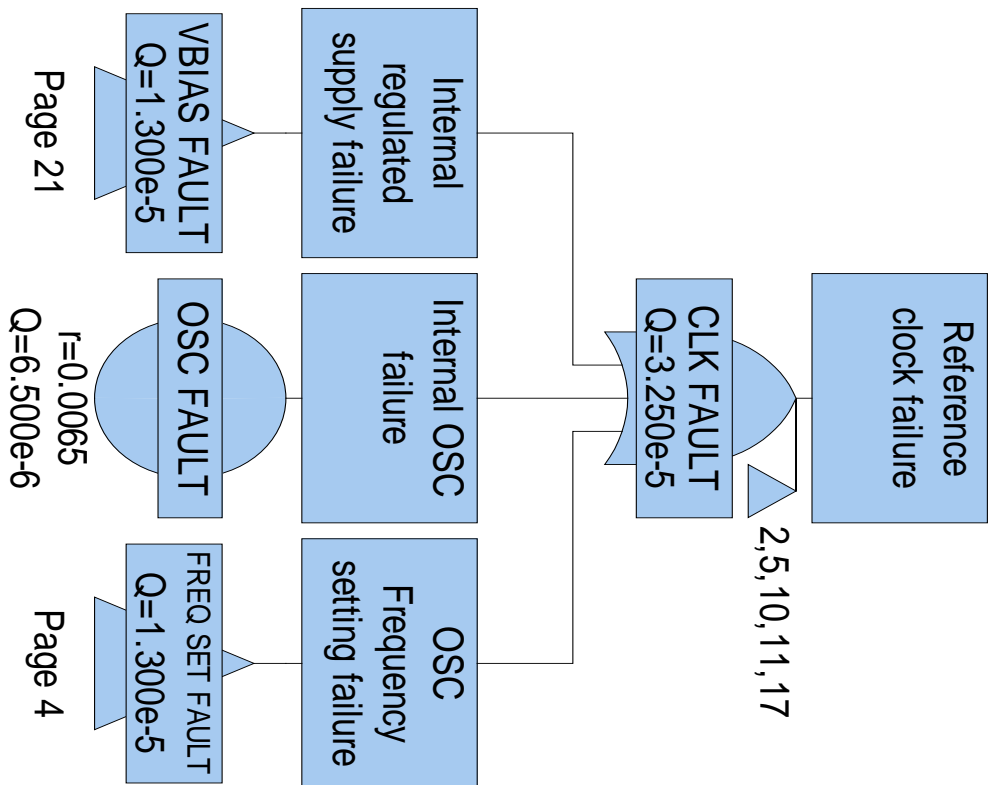
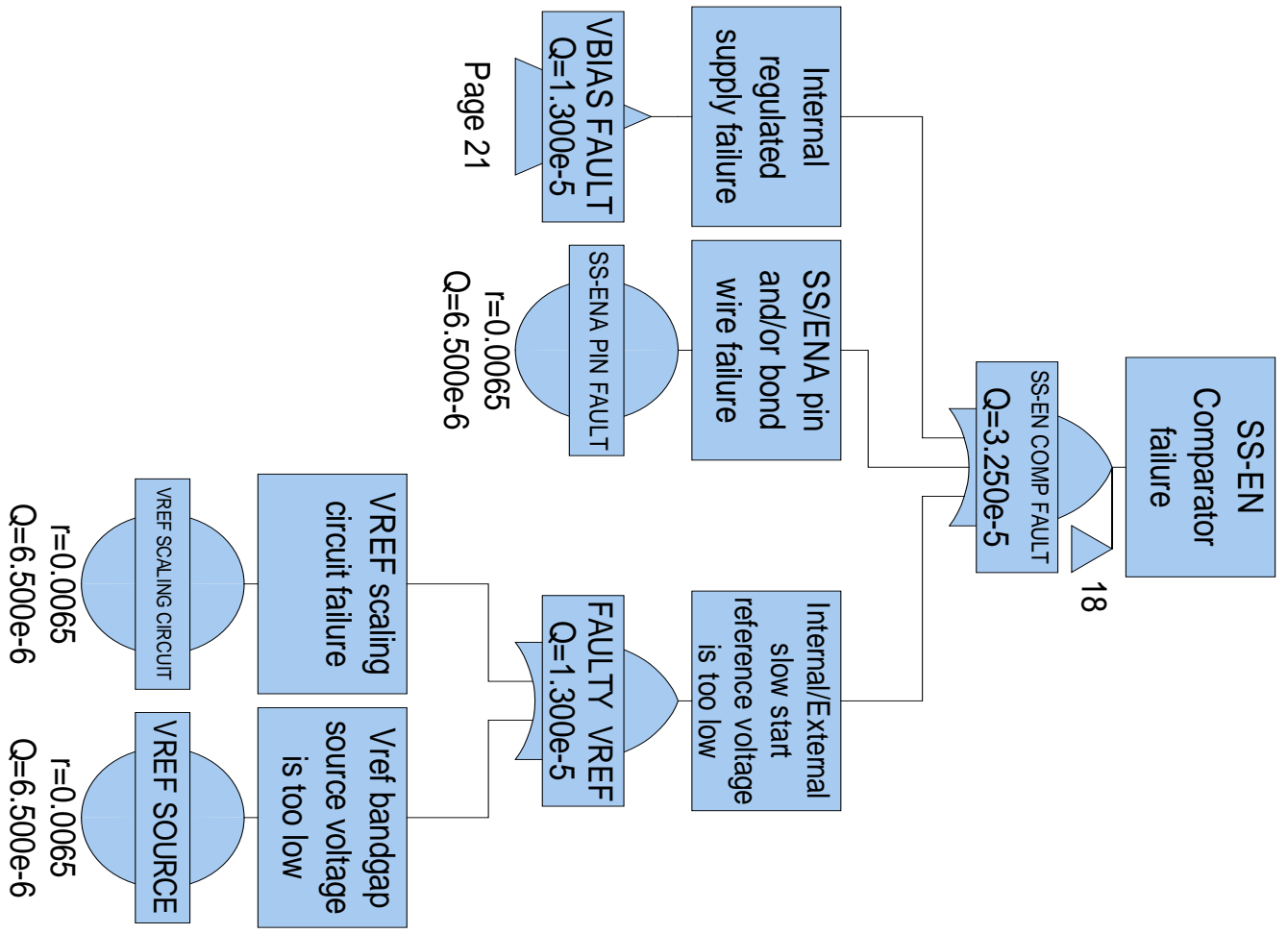


Figure 19. Reference clock failure



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Figure 20. SS/EN Comparator failure fault tree

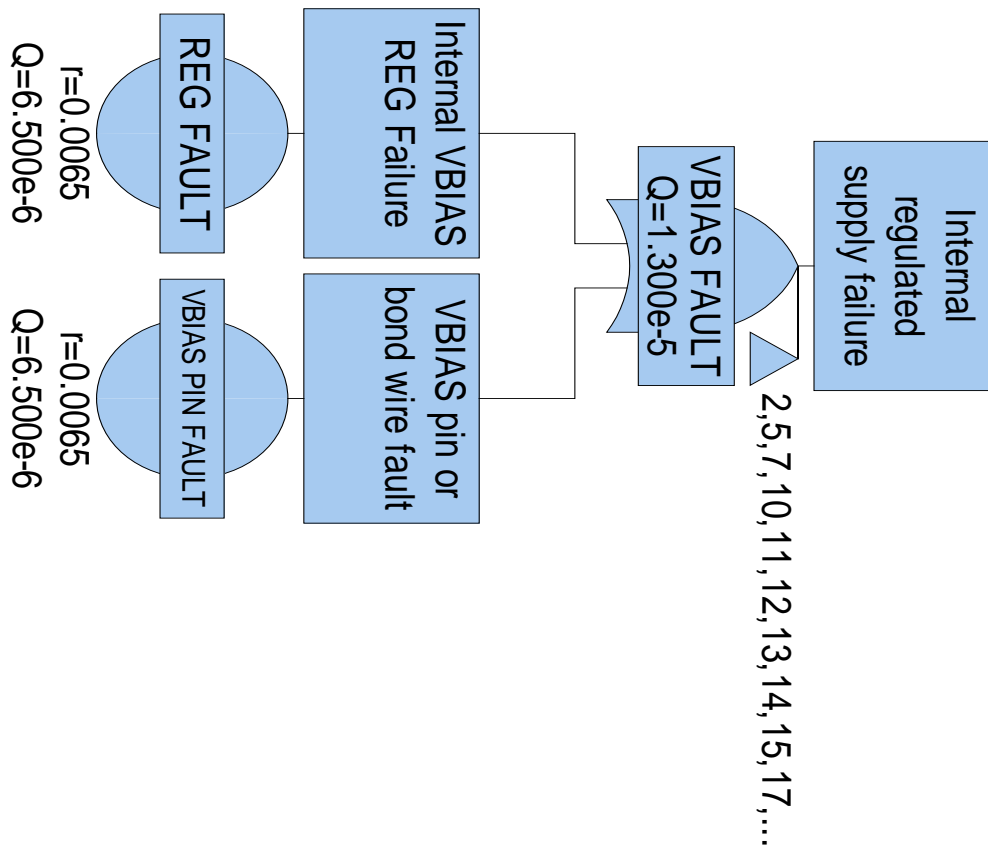


Figure 21. Internal Regulator failure fault tree

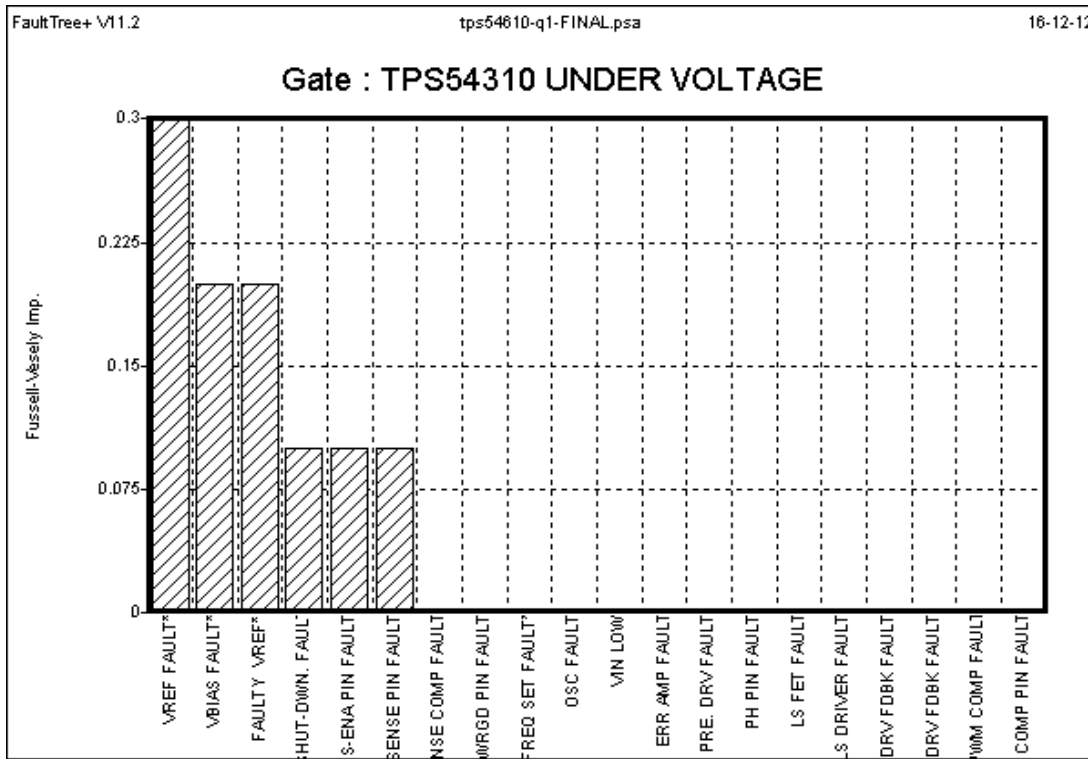


Figure 22. TPS54310 Undervoltage fault tree importance diagram

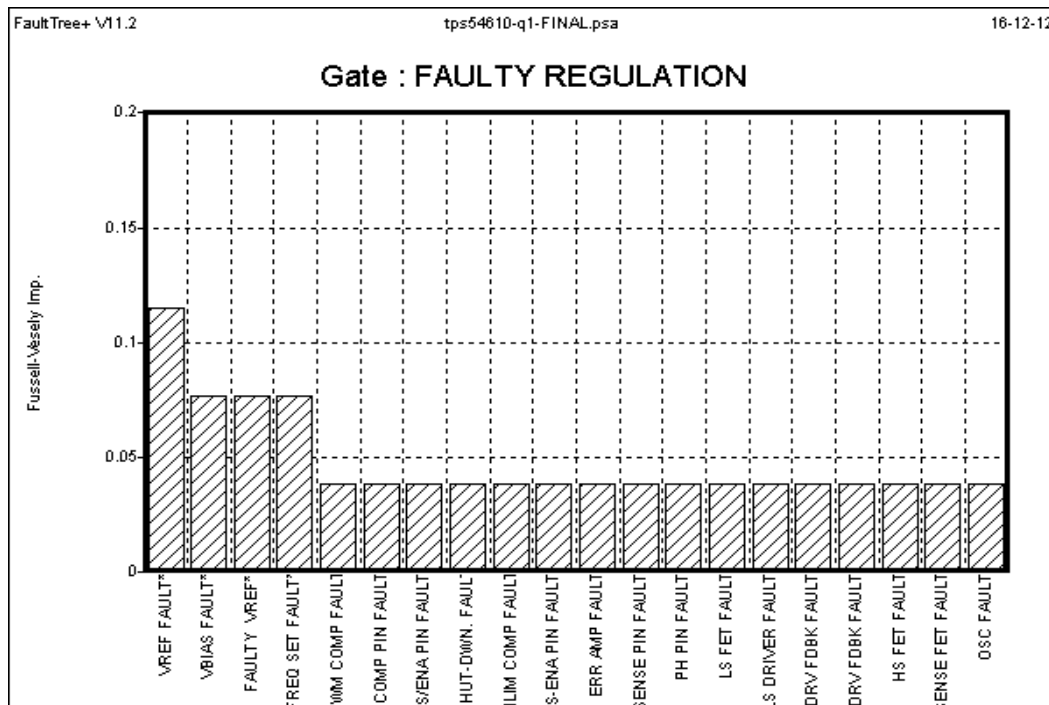


Figure 23. Faulty Regulation fault tree importance diagram



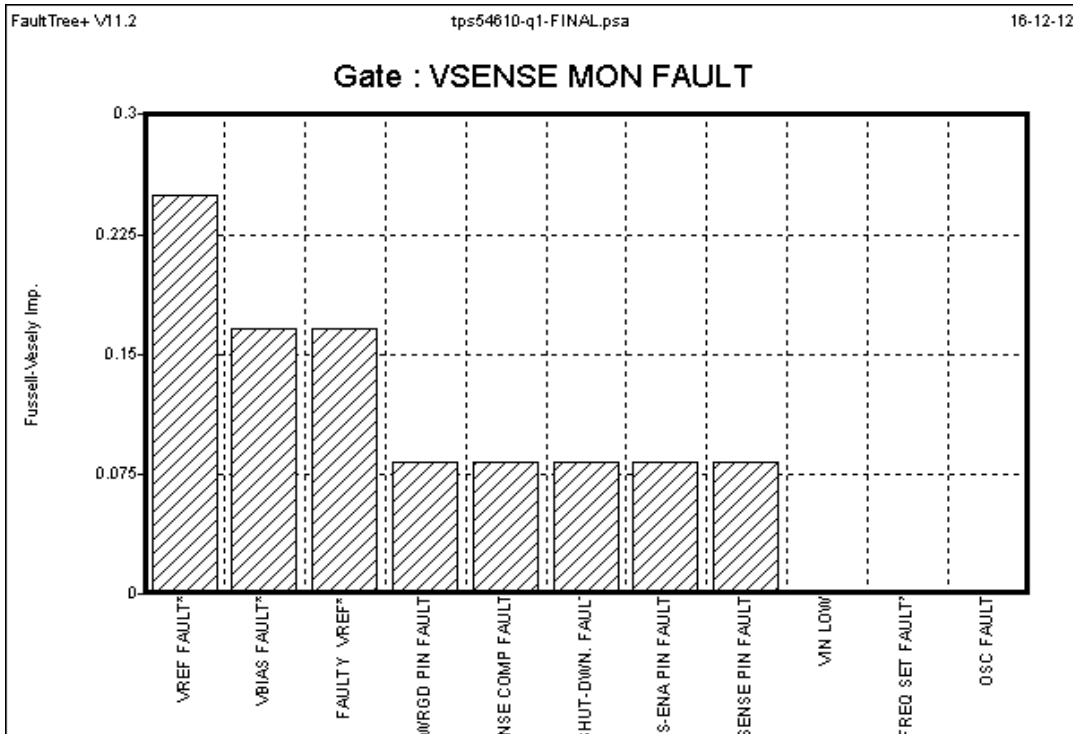


Figure 24. VSENSE Monitoring fault tree importance diagram

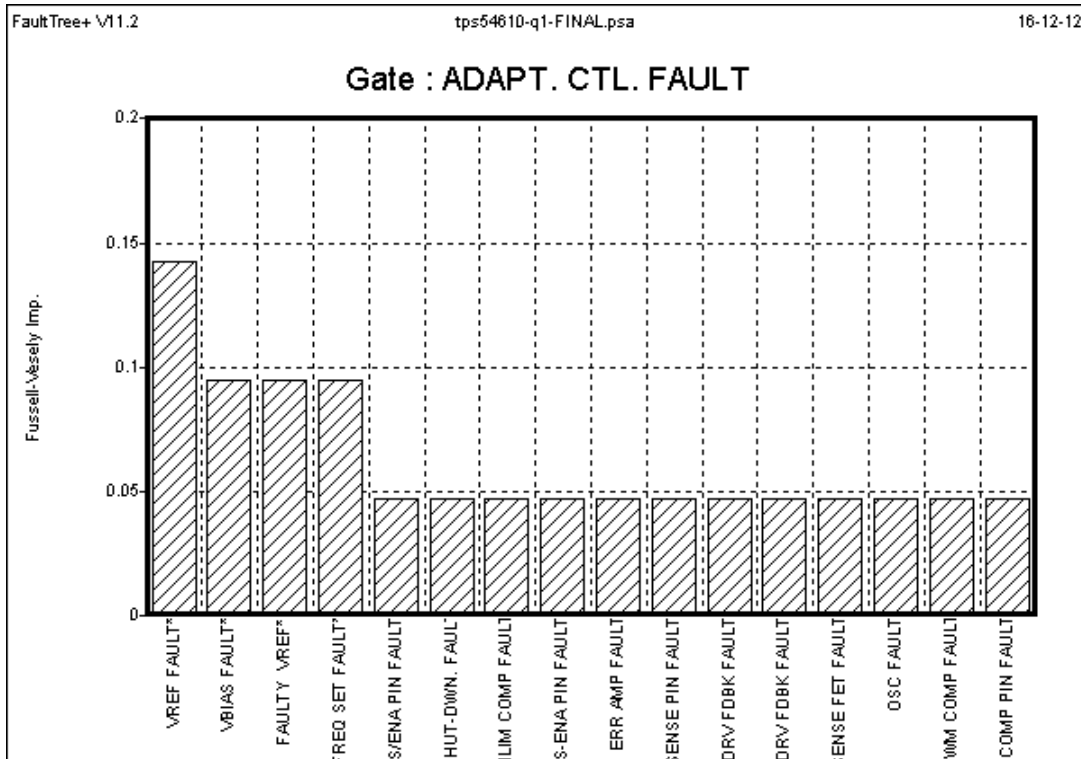


Figure 25. Adaptive PWM Control Circuit fault tree importance diagram

### 3 Hazards

- a. Faulty Switch Regulator leading to undervoltage condition

## 4 Analysis

### 4.1 Description

Cut Set: A group of events which will cause system failure when occurring together.

1<sup>st</sup> Order Cut Set: Single event failure causing hazard.

2<sup>nd</sup> Order Cut Set: Two failing events causing hazard.

3<sup>rd</sup> Order Cut Set: Three failing events causing hazard.

4<sup>th</sup> Order Cut Set: Four failing events causing hazard.

Base Event: Description of base events in associated fault tree diagram. Base events and their description referenced to TI's design database.

### 4.2 Faulty Switch Regulator Cut Sets

Hazard: Faulty Switch regulator leading to under voltage condition.

For this hazard a total 36 individual cut sets have been analyzed.

## 5 Conclusion

ASIC level hazard FTA completed. Switch regulator proactive system level monitoring and protection considerations were included.

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