Application Report

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TPS84A20 Parallel Operation

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ABSTRACT

The TPS84A20 is a 2.95-V to 17-V input, 10-A output, integrated power solution which integrates the PWM controller, power MOSFETs, inductor and passives in a low-profile, QFN package. For applications requiring greater than 10 A, it is possible to parallel up to six TPS84A20 devices by following the recommendations in this paper.

Current Sharing

The TPS84A20 is a peak current mode control device. In peak current mode control, the output voltage is scaled down through a resistor divider and fed into the error amplifier where it is compared to a fixed voltage reference. The output of the error amplifier is proportional to the device's output current. The output current information is available on the ISHARE pin (pin 25) of the TPS84A20. Connecting the ISHARE pins of multiple TPS84A20 devices together allows current sharing. Other connections must also be made between the devices.

Parallel Operation Connections

When paralleling TPS84A20 devices, several connections must be made between the devices. Figure 1 shows a typical schematic for paralleling two TPS84A20 devices.

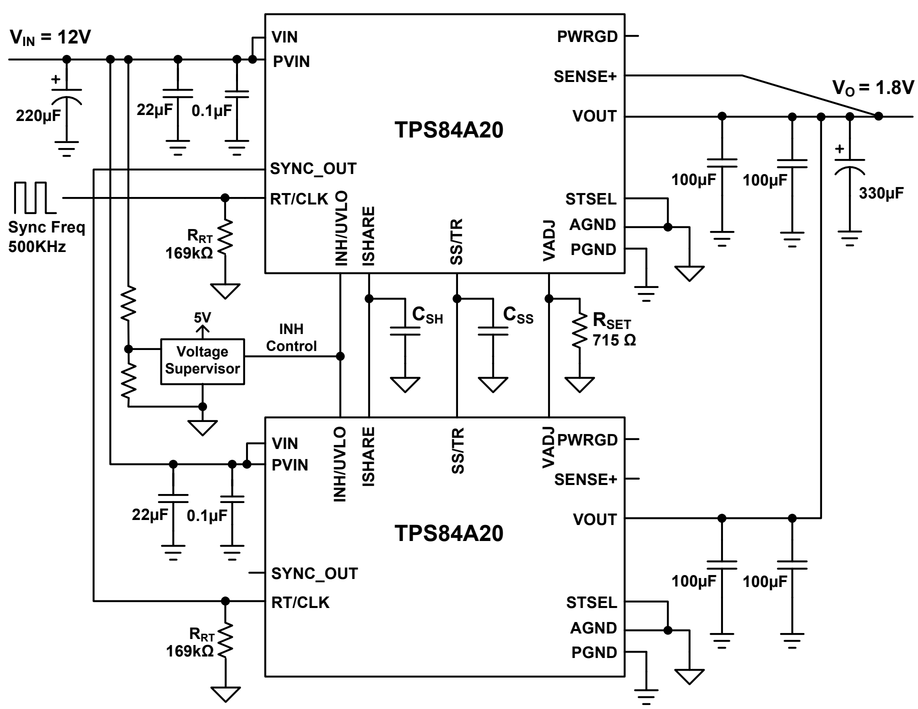

Figure 1. Typical TPS84A20 Parallel Schematic

Parallel Connections

- Connect the VOUT pins of all devices together to operate as a single output.
- The output voltage is monitored at the SENSE+ connection. The SENSE+ connection must only be made by one of the paralleled devices; the other device's SENSE+ pins must be left open.
- The VADJ pin of all devices must be connected together to ensure all devices see the same feedback voltage. The output voltage is set by connecting a single resistor (R_{SET}) between the VADJ connection and AGND. The R_{SET} resistor value can be selected from Table 2 in the TPS84A20 (SLVSBC6) datasheet.
- For proper current sharing, the ISHARE pin (pin 25) voltage of all devices must be equal. Connect the ISHARE pins together directly.
- Connecting the SS/TR pins together ensures that all devices start-up together by sharing the same slow start ramp voltage. The STSEL pins of all devices must be connected to AGND. To change the SS rise time, additional capacitance must be added to the SS/TR pin of each device according to Table 6 in the TPS84A20 (SLVSBC6) datasheet.
- The switching frequency of the devices must be the same to ensure proper current sharing and operation. It is required to drive the RT/CLK pin of all devices with an external clock to ensure they switch at the same frequency. The clock signal must be present before the devices are turned on. The TPS84A20 produces a SYNC_OUT signal which is a 180° out-of-phase clock that can be driven to another device's RT/CLK pin to synchronize 180° out of phase.
- The INH/UVLO pins of the devices must be tied together. To enable and disable the output voltage, the INH/UVLO pins must be controlled for all paralleled devices at the same time. It is recommended to monitor the input voltage using a supervisor and control the turn-on and turn-off of the output in order to ensure a clean and controlled power-up and power-down.

TPS84A20 Parallel Operating Conditions

When paralleling multiple TPS84A20 devices, the input voltage range and output voltage range is the same as for a single device, as specified in the datasheet. The amount of required output capacitance for a single device listed in Table 3 of the datasheet (SLVSBC6) must be multiplied by the number of devices being paralleled. The allowable synchronization frequencies are a function of Vin and Vout and can be found in Table 7 of the datasheet (SLVSBC6). However, the combined output current must be de-rated as described in Current Sharing Accuracy.

TPS84A20 Parallel Results

The results and waveforms presented in this report represent two devices in parallel, unless otherwise stated. The waveforms were taken at 12-V input, 1.8-V output, 25°C ambient temperature, and synchronized to a 500-kHz external clock. The 500-kHz clock was fed to the RT/CLK pin of one device, and the SYNC_OUT pin of that device was fed to the RT/CLK pin of the second device to easily achieve 180° out-of-phase operation. It is possible to parallel up to six devices with similar results, as is presented here. However, close attention must be paid to board layout when paralleling multiple devices to ensure clean inter-connecting signals.

ISHARE

For proper current sharing, the voltage on the ISHARE pin of all devices must be equal. Connect the ISHARE pins of all devices together. The ISHARE connection must be routed in a way to keep this signal as clean as possible. An optional capacitor (≤ 100 pF) can be added to the ISHARE pin of each device to help filter the signal.

Synchronizing to an External Clock

In order to operate the TPS84A20 devices in parallel, it is required to synchronize all devices to an external clock. The clock must be present before input power is applied, or before release of the INH control. All devices must be synchronized to the same frequency, however, the devices can be driven out of phase to reduce ripple voltage and improve transient response. The SYNC_OUT pin of one device can be fed to the RT/CLK pin of a second device to easily achieve 180° out-of-phase operation.

ON and OFF Control

It is recommended to turn-on and turn-off the paralleled devices by use of the Inhibit control, rather than by the internal UVLO of the TPS84A20. Using a voltage supervisor, such as the TPS3808, to monitor the input voltage and control the INH pins is recommended. The INH pins of the paralleled device should be connected to one another to ensure a controlled ramp up and ramp down of the output voltage. By doing this, it will avoid the slightly different UVLO turn-on and UVLO turn-off thresholds of the multiple devices. Figure 2 and Figure 3 show the turn-on and turn-off of the output voltage using the INH control.

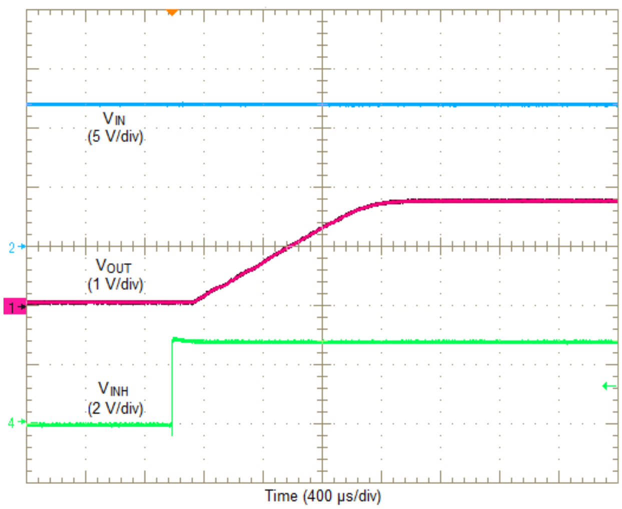

Figure 2. Start up Waveform (using INH)

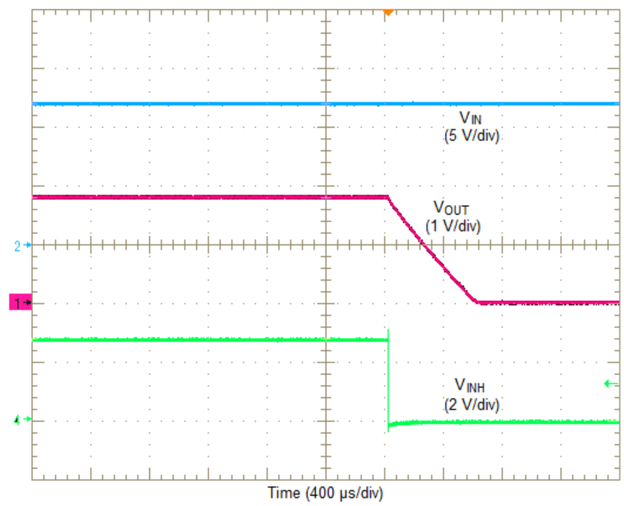

Figure 3. Shut Down Waveform (using INH)

Undervoltage Lock-Out (UVLO)

The TPS84A20 has a UVLO circuit internal to the device. When paralleling multiple TPS84A20 devices, the INH/UVLO pins of all modules must be connected together and the UVLO threshold must be set externally with a resistor divider from the input voltage. The values of the resistors in the divider can be selected from Table 8 of the TPS84A20 (SLVSBC6) datasheet; however, the resistor values shown in the table must be divided by the number of modules being paralleled. It is recommended to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

Current Sharing Accuracy

When paralleling multiple TPS84A20 devices, the maximum output current the solution can provide must be calculated using Equation 1. Due to internal variances between devices, the amount of output current must be de-rated to ensure none of the devices operate above the maximum output current of a single device (10 A). Figure 2 plots the typical output current per device of two paralleled devices. The X-axis is the total output current of both devices combined.

I_{OUTmax} = 0.9 × (n × 10) (A); where n is the number of TPS84A20 devices being paralleled. (1)

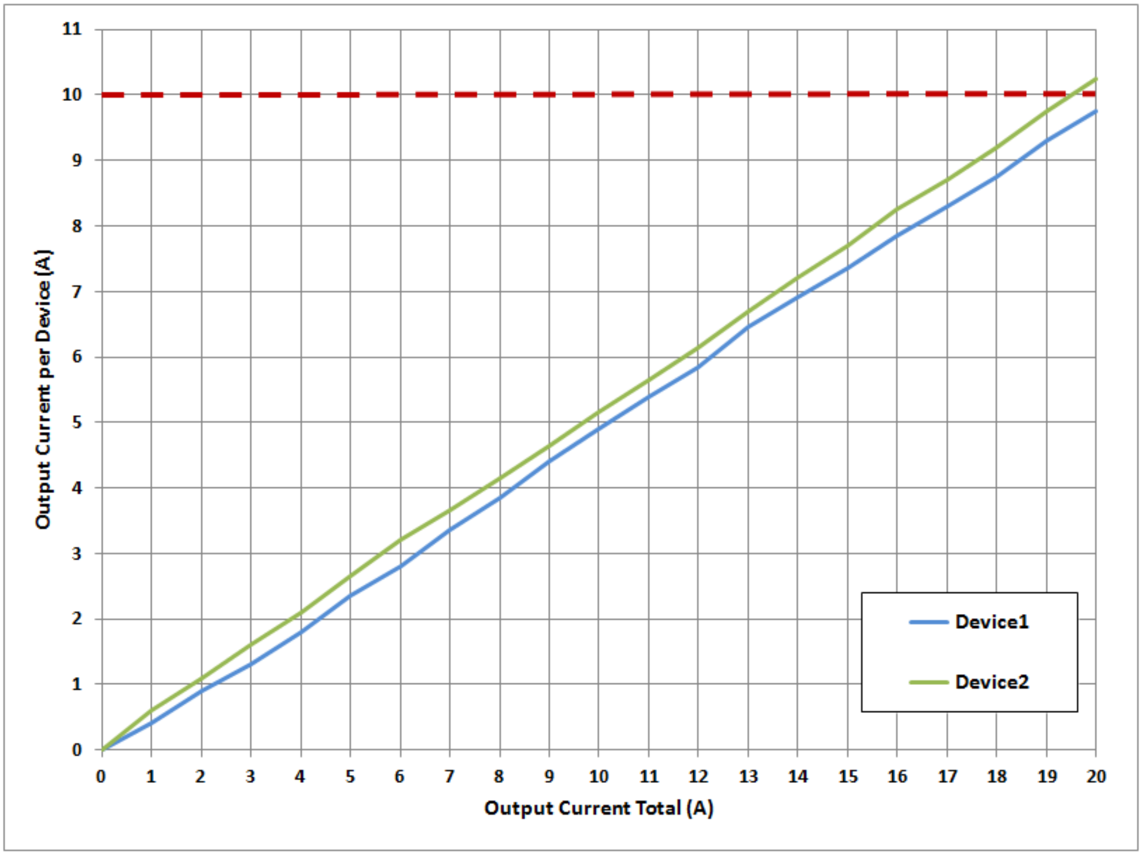

Figure 4. Typical Current Sharing Accuracy

Output Voltage Ripple

The output voltage ripple of two paralleled TPS84A20 modules is shown in Figure 5 and Figure 6. The operating conditions for this waveform are Vin = 12 V, Vout = 1.8 V, Iout = 18 A, fsw = 500 kHz, Cout = 8 × 47-µF ceramic + 2 × 470-µF polymer tantalum. Also included in the waveform are the Phase nodes of both devices. Figure 5 shows both devices switching in phase with one another. Figure 6 shows the devices switching 180° out-of-phase with one another. By operating out of phase the output voltage ripple is reduced.

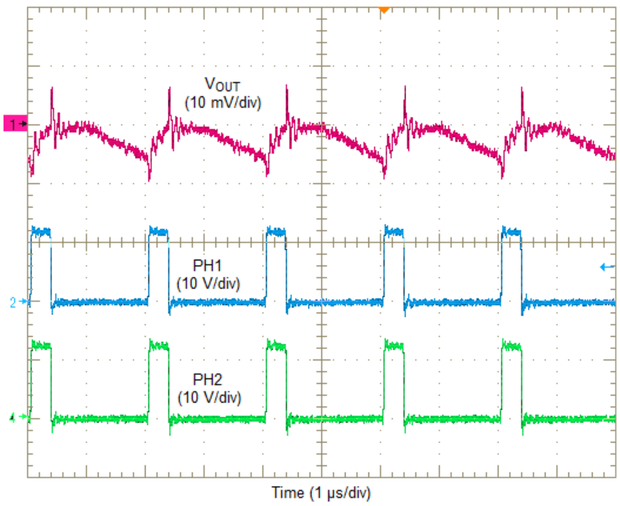

Figure 5. Output Voltage Ripple In-Phase

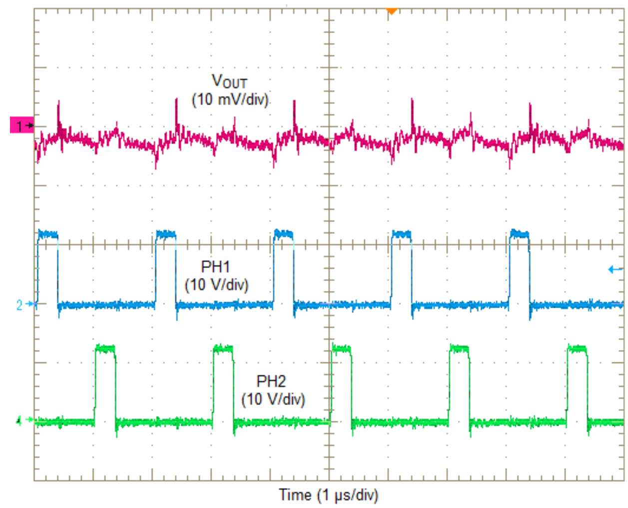

Figure 6. Output Voltage Ripple 180° Out-of-Phase

Input Voltage Ripple

The input voltage ripple of two paralleled TPS84A20 modules is shown in Figure 7 and Figure 8. The operating conditions for this waveform are Vin = 12 V, Vout = 1.8 V, Iout = 18 A, fsw = 500 kHz, Cin = 4 × 47-µF ceramic + 2 × 470-µF polymer tantalum. Also included in the waveform are the Phase nodes of both devices. Figure 7 shows both devices switching in phase with one another. Figure 8 shows the devices switching 180° out-of-phase with one another. By operating out of phase the input voltage ripple is reduced.

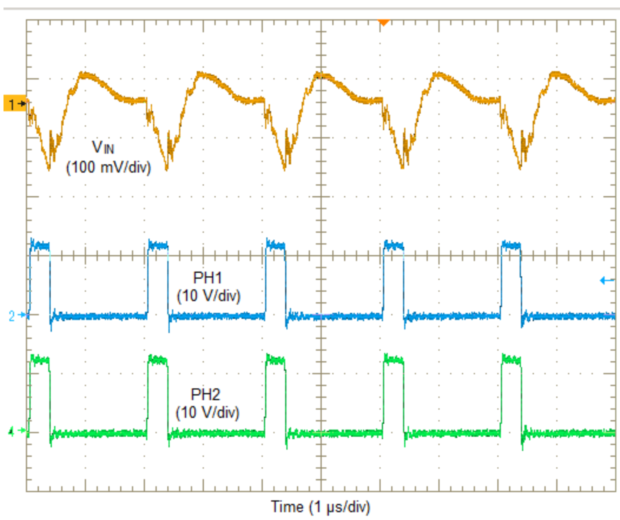

Figure 7. Input Voltage Ripple In-Phase

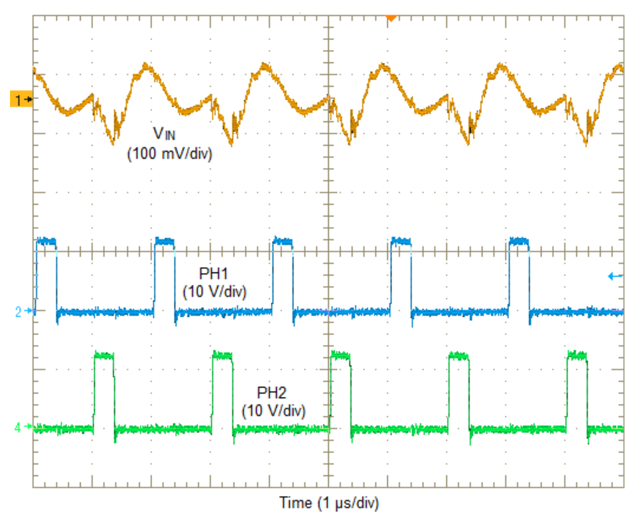

Figure 8. Input Voltage Ripple 180° Out-of-Phase

Transient Response

The waveform shown in Figure 9 shows the transient response of two TPS84A20 devices operating in parallel. The operating conditions for this waveform are Vin = 12 V, Vout = 1.2 V, fsw = 300 kHz; 180° out-of-phase, Iout load step = 8 A (2.5 A/µs), Cout = 8 × 47-µF ceramic + 2 × 1000-µF polymer tantalum.

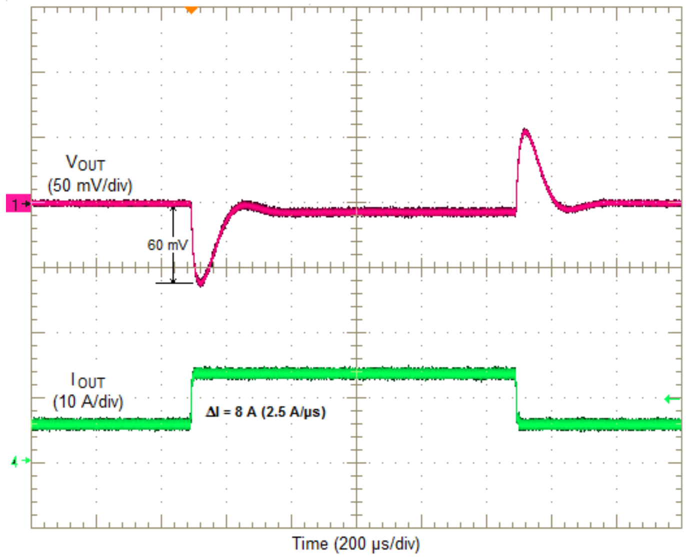

Figure 9. Transient Response (8-A Load Step)

Conclusion

By making the required connections between TPS84A20 devices and synchronizing the devices to the same switching frequency, paralleled devices will operate and behave as a single stand-alone device with increased output current capability. Controlling the turn-on and turn-off through the Inhibit function while a valid input voltage is present will ensure a proper ramp up and ramp down of the output voltage. By following the guidelines included in this paper and referencing the TPS84A20 datasheet (SLVSBC6), up to six TPS84A20 power modules can be paralleled for increased current applications.

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