Application Report
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# DRV10866 Lock Detection Functionality

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**ABSTRACT**

This document is provided as a supplement to the DRV10866 data sheet. It details how the DRV10866 can falsely detect a locked rotor and the recommended workaround procedures.

**Contents**

1 Introduction ..... 2
2 False Lock Detection ..... 2
2.1 Description of Circuit ..... 2
2.2 Target Motor Speed is Fixed Inside the False Detection Range of 101.6 Hz ±10% at $V_{CC}$ 5 V Room Temperature ..... 3
2.3 Target Motor Speed is Fixed Outside the False Detection Range of 101.6 Hz ±10% at $V_{CC}$ 5 V Room Temperature ..... 3
2.4 Target Motor Speed is Variable with FG Inside the False Detect Window ..... 3
3 Conclusion ..... 3

**List of Figures**

1 Timing of Internal Sampling Clock Versus FG Output ..... 2

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# 1 Introduction

The DRV10866 is an integrated device providing the benefits of low cost, low size, and ease of use. Under certain conditions, it has been determined that the lock detection mechanism can detect a locked rotor condition that is not real. If a locked rotor condition is incorrectly detected, the DRV10866 will stop driving the motor, wait for some time, and then re-start.

This false lock condition occurs when a number of conditions are met. The information in Section 2 describes the condition in which the lock is incorrectly detected and recommended workaround procedures.

# 2 False Lock Detection

## 2.1 Description of Circuit

The lock detection circuit inside the DRV10866 monitors the FG signal to determine if the signal is static. If the FG signal is sampled as a static value for approximately 305 clocks of an internal sampling clock, the internal logic signals that the rotor is locked. When this condition occurs, the DRV10866 is reset and after approximately 5 seconds is restarted.

The internal sampling clock reference is set to approximately 101.6 Hz, with a variance of 10% at $V_{CC}$ 5 V room temperature.

It has been observed that some devices falsely detect lock if the FG signal matches this internal sampling clock. An example is when the FG signal is within 0.16% of the sampling clock. When this condition occurs, the 305 samples will occur in either the high side or the low side of the FG signal.

Figure 1 shows the internal sampling clock sampling a logical high on the FG signal for 5 consecutive samples. If this is continued through 305 samples, the internal lock detection signals that the rotor is locked.

The relationship of the variation of FG and the internal sampling clock are inversely proportional.

FG Variation allowed = 0.16% / (FG/Internal Sampling Clock) (1)

As FG increases by a power of 2, the variation allowed decreases by the same power of 2. This means that it becomes less likely for a false lock to be detected as the motor speed increases.

As seen in Figure 1, the sampling of FG at multiples of the internal sampling clock can also result in false lock conditions. As the FG frequency increases by even multiples of the sample clock, the allowable variation of the FG signal decreases. For example, if FG is twice the internal sampling clock the allowed variation of the FG signal reduces to 0.08%.

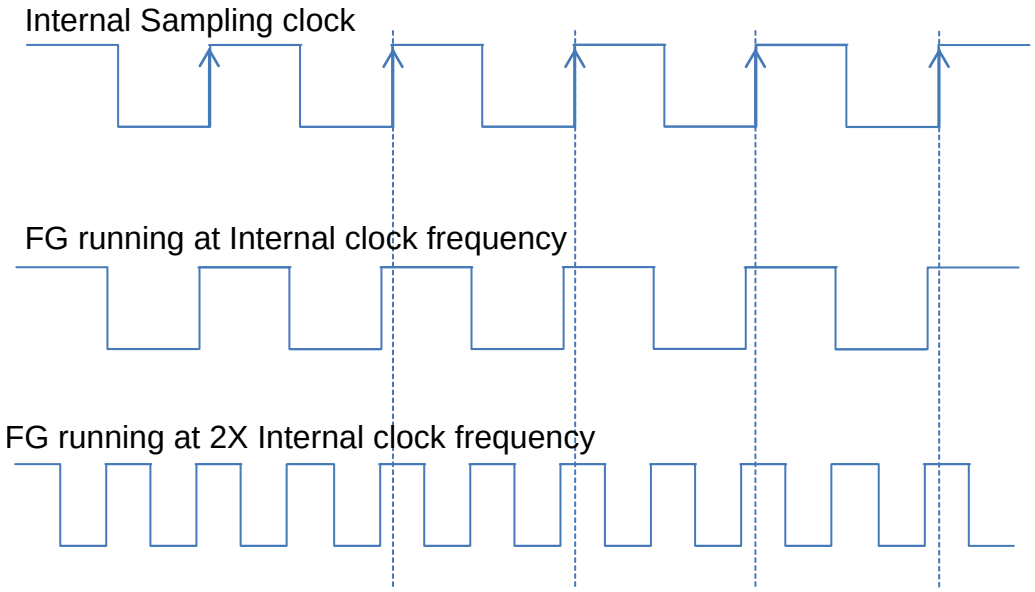


**Figure 1. Timing of Internal Sampling Clock Versus FG Output**



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The false lock condition depends on several conditions. The motor speed can vary as the temperature of the device varies. The voltage of the DRV10866 can vary from board to board or system to system. The internal sampling clock can vary due to process variations.

If the false lock is detected, the recommended workaround procedures are listed below. These workarounds depend on the application. In some applications, the target speed is fixed. In other applications, the target speed may vary from zero to the maximum motor speed.

### 2.2 Target Motor Speed is Fixed Inside the False Detection Range of 101.6 Hz ±10% at $V_{cc}$ 5 V Room Temperature

Use FGS input to change the FG frequency such that it will be outside of the window. The FG signal can either be increased or decreased by a multiple of 2 on power up by changing the FGS input.

### 2.3 Target Motor Speed is Fixed Outside the False Detection Range of 101.6 Hz ±10% at $V_{cc}$ 5 V Room Temperature

No action is required.

### 2.4 Target Motor Speed is Variable with FG Inside the False Detect Window

There are three possible actions if the lock detection occurs falsely. All actions change the speed of the motor:

- If using the PWM input to adjust the motor speed, raise or lower the PWM input duty cycle by 1%. This will move the FG signal away from the internal sampling clock frequency.
- If using $V_{CC}$ to adjust the motor speed, raise or lower $V_{CC}$ by 10 mV. This will move the FG signal away from the internal sampling clock frequency.
- Modulate the PWM input between 2 duty cycles 1% to 2% apart. Do this every 1 to 1.5 seconds to prevent the FG frequency matching the internal sampling frequency. The result is an average speed of the two PWM duty cycles.

## 3 Conclusion

The lock detect circuitry of the DRV10866 device can improperly report a rotor locked condition when several events align. The alignment of these events can be avoided by using the workarounds described above.


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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2013) to A Revision | Page |
|---|---|
| • Changed the second paragraph of Section 2.1 | 2 |
| • Changed From: 101.6Hz +/-30% To: 101.6 Hz ±10 at $V_{CC}$ 5 V Room Temperature in Section 2.2 and Section 2.3 | 3 |


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