Application Report
SLVA744–January 2016

Build a High-Density, High Refresh Rate, Multiplexing Panel With the TLC59581

Ge, Rosley

ABSTRACT

The application note describes the detailed steps to build a high-density, high refresh rate, multiplexing panel with the TLC59581. Detailed configurations and system structure guidelines are included in this report.

Contents

List of Figures

List of Tables

1 Introduction

The TLC59581 is a 48-channel, constant-current sink driver for multiplexing system with a 1-to-32 duty ratio. Each channel has an individually-adjustable, 65536-step, pulse width modulation (PWM) grayscale (GS). 48Kb display memory is implemented to increase the visual refresh rate and to decrease the GS data writing frequency.

The TLC59581 implements Low Grayscale Enhancement (LGSE) technology to improve the display quality at low grayscale conditions. This feature makes the TLC59581 more suitable for high-density multiplexing applications.

The output channels are categorized into three groups, each group has 16 channels. Each group has a 512-step color brightness control (CC) function. The maximum current value of all 48 channels can be set with an 8-step global brightness control (BC) function. CC and BC are used to adjust the brightness deviation between LED drivers. GS, CC, and BC data are accessible via a serial interface port.

The TLC59581 has one error flag: LED open detection (LOD), which can be read via a serial interface port. The TLC59581 also has a power-save mode that sets the total current consumption to 0.8 mA (typ) when all outputs are off. Each constant-current has a pre-charge field-effect transistor (FET), which can reduce ghosting and improve display performance on the multiplexing LED display. The TLC59581 also has an enhanced circuit that can cancel the caterpillar effect caused by a broken LED.

The TLC59581 has the following features:

- 48 channel constant current sink output
- Low Grayscale Enhancement (LGSE) technology
- Sink current capability with max BC/CC data:
  - 25 mA at 5 V V_{CC}
  - 20 mA at 3.3 V V_{CC}
- Global Brightness Control (BC) : 3 bit (8 Step)
- Color Brightness Control (CC) for each color group: 9 bit (512 Step), three groups
- Grayscale (GS) control with multiplexed enhanced spectrum (ES) PWM: 16 bit
- 48Kb Grayscale data memory support 32-multiplexing
- LED power-supply voltage up to 10 V
- V_{CC} = 3.0 V to 5.5 V
- Constant current accuracy
  - Channel to channel = ±1% (Typ), ±3% (Max)
  - Device to device = ±1% (Typ), ±2% (Max)
- Data transfer rate: 25 MHz
- Grayscale clock: 33 MHz
- LED open detection (LOD)
- Thermal shut down (TSD)
- I_{REF} resistor short protection (ISP)
- Power-save mode (PSM) with high-speed recovery
- Delay switching to prevent inrush current
- Pre-charge FET to avoid ghosting phenomenon
- Operating temperature : –40°C to 85°C

The TLC59581 is mainly targeted for the following applications:

- LED video displays with a multiplexing system
- LED signboards with a multiplexing system
- High refresh rate and high-density LED panels

Figure 1 represents a typical application circuit of TLC59581.

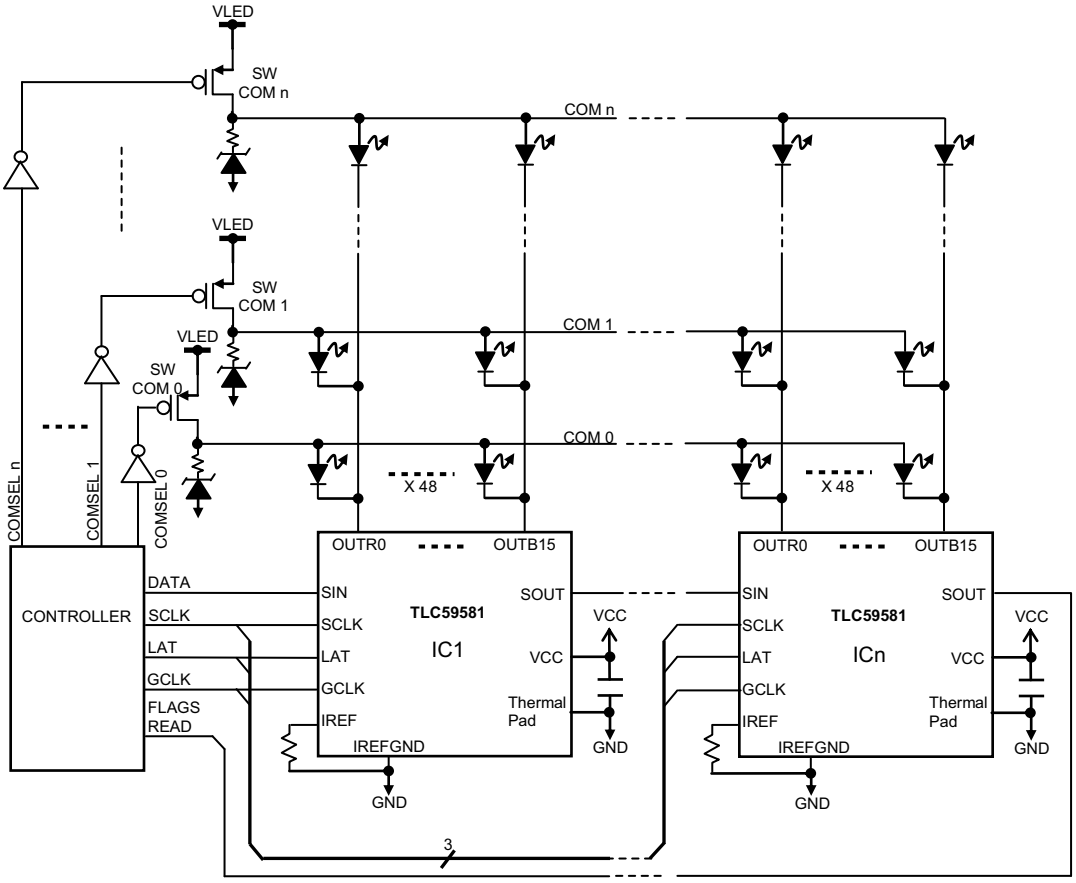


Figure 1. Typical Application Circuit (Multiple Daisy Chained TLC59581s)

2 Device Specification

2.1 Basic Information

Basic information, such as electrical characteristics, thermal, package information, and recommended operation conditions, are found in TLC59581 datasheet (SLVSCZ9). The TLC59581 function block diagram, pin-out information, and pin descriptions are also found in datasheet.

2.2 Switching Characteristics

The following table contains the TLC59581 switching characteristics.

At V_{CC} = 3.0–5.5 V, T_A = –40 to 85°C, C_L = 15 pF, R_L = 4 kΩ, target at 1 mA I_{OLC}, V_{LED} = 5.0 V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted).

Parameter		Test Conditions		MIN	TYP	MAX	Unit
t_{r0} (1)	Rise time	SOUT			2	5	ns
t_{r1}		OUTx0-15, x = R/G/B, BC = 0h, CCR/G/B = 1FFh, R_{IREF} = 976 Ω (25-mA target), T_a = 25°C, R_L = 160 Ω			35		
t_{f0} (1)	Fall time	SOUT			2	5	
t_{f1}		OUTx0-15, x = R/G/B, BC = 0h, CCR/G/B = 1FFh, R_{IREF} = 2.46 kΩ (10-mA target), T_a = 25°C, R_L = 400 Ω			15		
t_{d0} (1)	Propagation delay time	SCLK ↑ to SOUT, SEL_TD0 = 00b		8	15	27	
		SCLK ↑ to SOUT, SEL_TD0 = 01b		13	25	45	
		SCLK ↑ to SOUT, SEL_TD0 = 10b		19	35	60	
		SCLK ↓ to SOUT, SEL_TD0 = 11b		6	10	22	
t_{d1} (1)		LAT ↓ to SOUT, ReadFC1/2, ReadSID			26	50	
t_{d2}		GCLK↓ to OUTR0/7/8/15 turn on or turn off	R_{IREF} = 976 Ω (25-mA target), BC = 0h, CCR/G/B = 1FFh, T_a = 25°C, SEL_GDLY = 1		15		
t_{d3}		Propagation delay time between group and next group			5		
t_{d4}		Propagation delay time between color and next color in same group			1.67		

(1) Ensure by design.

2.3 Parameter Measurement Information

Figure 2, Figure 3, and Figure 4 illustrate the parameter measurement information.

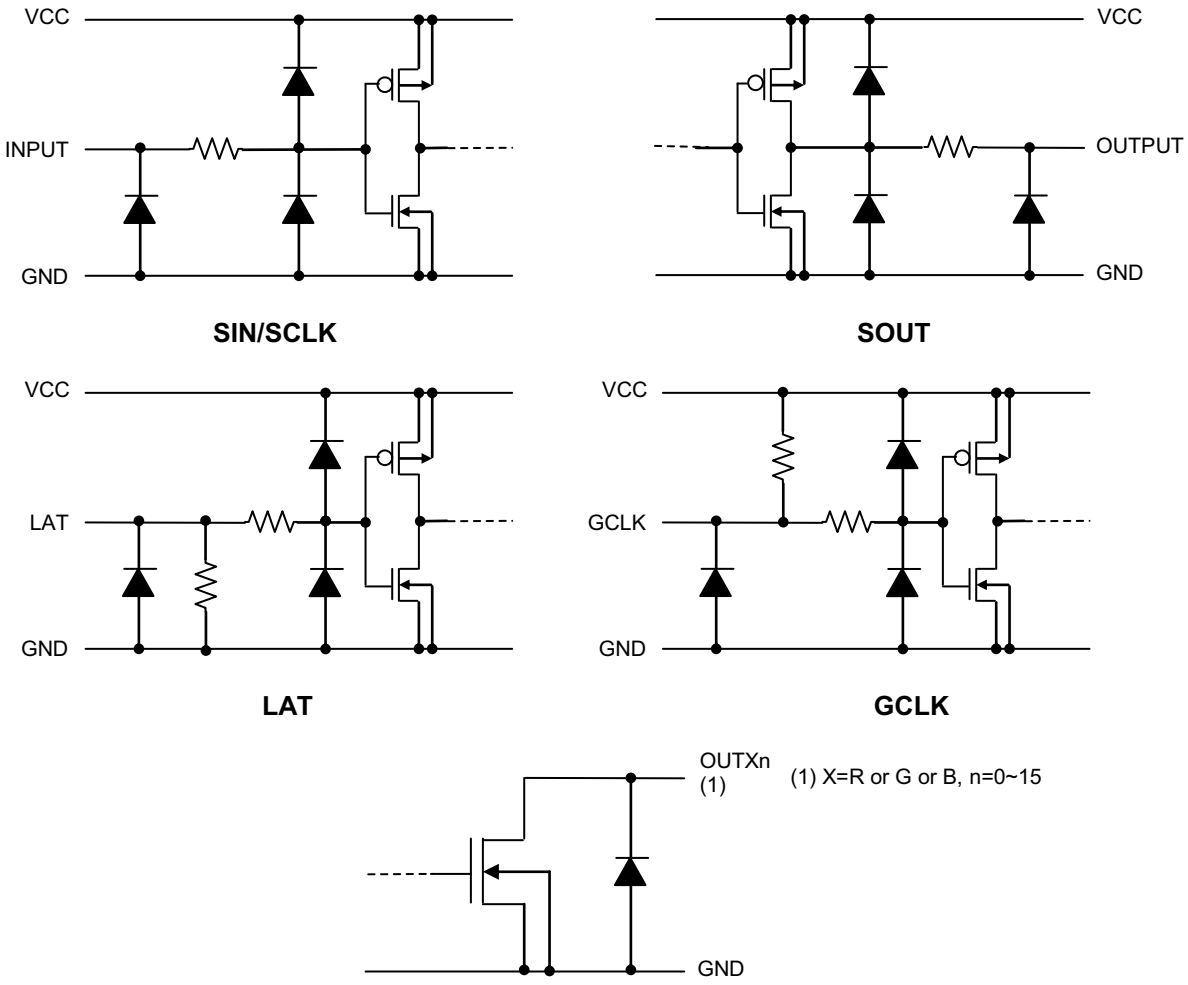
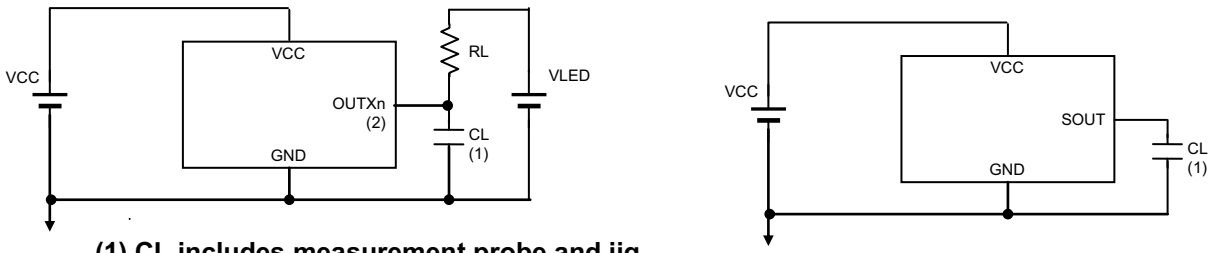


Figure 2. Pin Schematic Diagrams



(1) CL includes measurement probe and jig capacitance.

(1) CL includes measurement probe and jig capacitance.

Figure 3. Rise Time and Fall Time Test Circuit

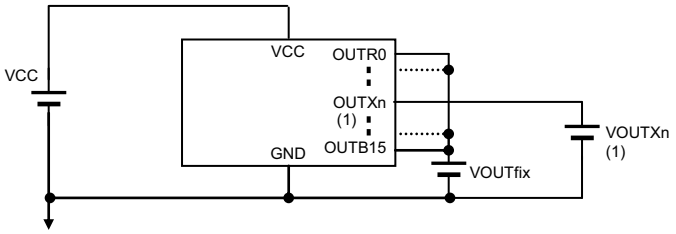
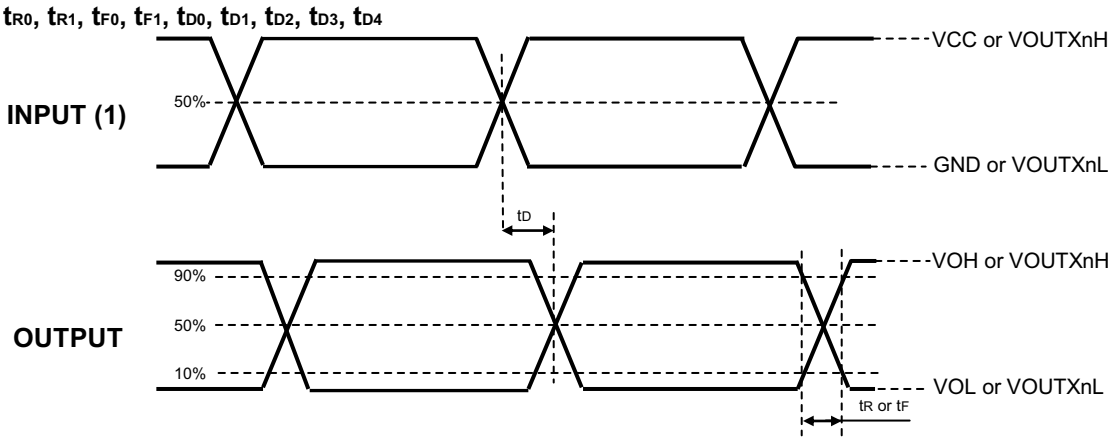


Figure 4. Constant Current Test Circuit for OUTXn

2.4 Timing Diagrams



(1) Input pulse rise and fall time is 1~3nS.
(2) X=R or G or B, n=0~15

Figure 5. Output Timing

3 Detailed Description

3.1 How to use the TLC59581

After power on, all OUTXn of TLC59581 are turned off. All the internal counters and function control registers (FC1/FC2) are initialized. A brief summary of the sequence to operate the TLC59581 follows, providing a general idea how this part works. After that, the function block related to each step is detailed in the following sections.

1. According to required LED current, choose BC and CC code, select the current programming resistor R_{IREF}.
2. Send the WRTFC command to set FC1/2 register value if the default value needs changing.
3. Write GS data of all lines (max 32 lines) into one of the two memory BANKs.
4. Send Vsync command, the BANK with the GS data just written is displayed.
5. Input GCLK continuously, 257 GCLK (or 129 GCLK) as a segment. Between the interval of two segments, switch supply voltage from one line to the next line accordingly.
6. During the same period of step 5, write GS data for the next frame into another BANK.
7. When the time of one frame ends, input the Vsync command to swap the purpose of the two BANKs.

Repeat steps 5–7…

3.2 Step 1 — Choose BC and CC, Select R_{IREF}

3.2.1 What is the BC function?

The TLC59581 is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 3-bit word, thus all output currents can be adjusted in 8 steps from 12.9% to 100% (see Table 1) for a given current programming resistor (R_{IREF}).

BC data are set via the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control (FC) register FC1 is set to 4h as the initial value.

3.2.2 What is the CC Function?

The TLC59581 is able to adjust the output current of each of the three color groups OUTR0-OUTR15, OUTG0-OUTG15, and OUTB0-OUTB15 separately. This function is called *color brightness control* (CC). For each color, there is 9-bit data latch CCR, CCG, or CCB in FC1 register (see Table 3 for FC1 register bit assignment). Thus, all color group output currents can be adjusted in 512 steps from 0% to 100% of the maximum output current, I_{OLCMax}. See Section 3.2.3 for more detail about I_{OLCMax}. The CC data are entered via the serial interface. When the CC data changes, the output current also changes immediately. When the IC is powered on, the CC data are set to '100h'. Equation 1 calculates the actual output current.

$$I_{OUT}\ (mA) = I_{OLCMax}\ (mA) \times (CCR/511d \text{ or } CCG/511d \text{ or } CCB/511d) \quad (1)$$

where

- I_{OLCMax} = the maximum channel current for each channel determined by BC data and R_{IREF} (see Equation 2)
- CCR/G/B = the color brightness control value for each color group in the FC1 register (000h to 1FFh)

Table 1 shows the CC data versus the constant-current against I_{OLCMax}.

Table 1. CC Data vs Current Ratio and Set Current Value

CC Data (CCR, CCG, or CCB)			Ratio of Output Current to I_{OLCMax} (%, typical)	Output Current (mA, R_{IREF} = 7.41 kΩ)	
Binary	Decimal	Hex		BC = 7h (I_{OLCMax} = 25 mA)	BC = 0h (I_{OLCMax} = 3.2 mA)
0 0000 0000	0	00	0	0	0
0 0000 0001	1	01	0.2	0.05	0.006
0 0000 0010	2	02	0.4	0.10	0.013
…	…	…	…	…	…
1 0000 0000 (Default)	256 (Default)	100 (Default)	50.1	12.52	1.621
…	…	…	…	…	…
1 1111 1101	509	1FD	99.6	24.90	3.222
1 1111 1110	510	1FE	99.8	24.95	3.229
1 1111 1111	511	1FF	100.0	25	3.235

3.2.3 How to Select R_{IREF} for a Given BC

The maximum output current per channel, I_{OLCMax}, is decided by a resistor, R_{IREF}, which is placed between the IREF and IREFGND pins, and the BC code in FC1 register (see Table 4 for FC1 register bit assignment). The voltage on IREF is typically 1.209 V. Calculate R_{IREF} with Equation 2.

$$R_{IREF}\ (k\Omega) = V_{IREF}\ (V) / I_{OLCMax}\ (mA) \times Gain \quad (2)$$

Table 2. Current Gain Versus BC Code

BC Data		Gain	Ratio of Gain/Gain_max (at max BC)
Binary	Hex		
000 (recommend)	0 (recommend)	20.4	12.9%
001	1	40.3	25.6%
010	2	59.7	37.9%
011	3	82.4	52.4%
100 (default)	4 (default)	101.8	64.7%
101	5	115.4	73.3%
110	6	144.3	91.7%
111	7	157.4	100%

3.2.4 How to Choose BC/CC for Different Applications

BC is mainly used for global brightness adjustment between day and night. Suggested BC is 4h, which is in the middle of the range, thus, one can change brightness up and down flexibly.

CC can be used to fine tune the brightness in 512 steps, this is suitable for white balance adjustment between RGB color groups. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 3:6:1. Depending on LED's characteristics (Electro-Optical conversion efficiency), the current ratio of R, G, B LED is much different from this ratio. Usually, the Red LED requires the largest current. Choose 511d (the max value) CC code for the color group which needs the largest current at first, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used.

Example 1: Red LED current is 2 0 mA, Green LED requires 12 mA, Blue LED requires 8 mA.

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 × 12 mA / 20 mA = 306.6, thus choose 307d for CCG. With the same method, choose 204d for CCB.
3. According to the required Red LED current, choose 7h for BC.
4. According to Equation 2, R_{IREF} = 1.209 V / 20 mA × 157.4 = 9.5 kΩ

In this example, we choose 7h for BC, instead of using the default 4h. This is because the Red LED current is 20 mA, which is approaching the upper limit of current range. To prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidently, we choose the max BC code here.

Example 2: Red LED current is 5 mA, Green LED requires 2 mA, Blue LED requires 1 mA.

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 × 2 mA / 5 mA = 204.4, thus choose 204d for CCG. With the same method, choose 102d for CCB.
3. According to the required Blue LED current, choose 0h for BC.
4. According to Equation 2, R_{IREF} = 1.209 V / 5 mA × 20.4 = 4.93 kΩ

In this example, we choose 0h for BC, instead of using the default 4h. This is because that the Blue LED current is 1 mA, which is approaching the lower limit of current range. To prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidently, we choose the min BC code here.

In general, if LED current is in the middle of range (that is, 10 mA), one can just use the default 4h as BC code.

3.3 Step 2 — Write Function Control Register FC1 and FC2

3.3.1 Input Data for FC1/2 Through Common Shift Register

The common shift register is 48 bits long and is used to shift data from the SIN pin into the TLC59581. The data shifted into the register can be latched into GS memory unit, or latched into function control (FC) registers FC1/2 depending on which command received.

Figure 6 shows the configuration of the common shift register and the data latches.

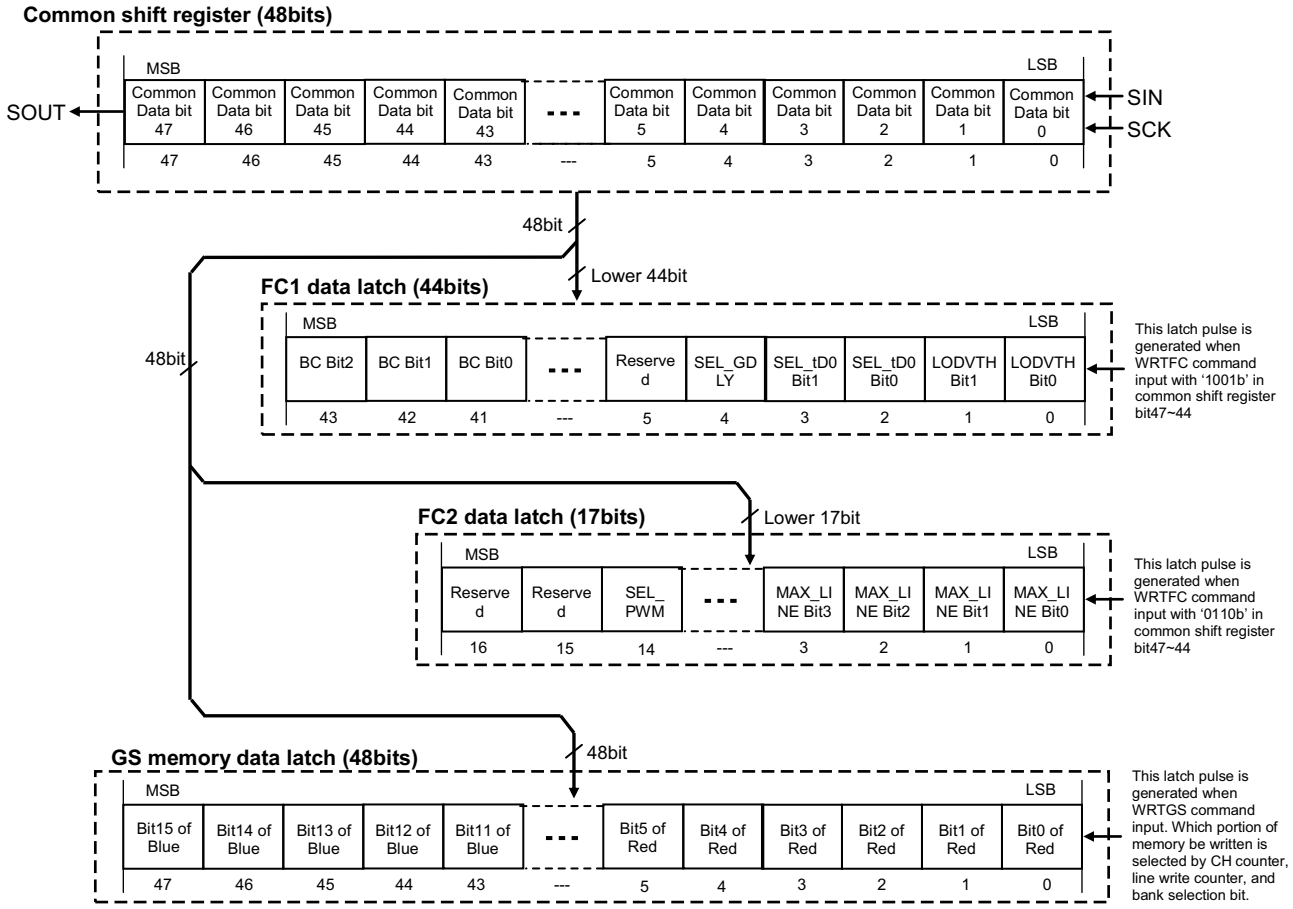


Figure 6. Common Shift Register and Data Latch Configuration

3.3.2 How to Write to the Function Control Register

The TLC59581 uses the FCWRTEN and WRTFC commands to latch the data of the common shift register into FC1/FC2. These commands are distinguished by the number of SCLK rising edges included in the LAT pulse. Table 3 describes more about these two commands.

Table 3. WRTFC/FCWRTEN Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
WRTFC (FC data write)	5	The lower 44-bit data or the lower 17-bit data in the common shift register are copied to the FC1 or FC2 register. Bit 47–44 of the common shift register is used to choose which FC register is written to. If '1001b' is received for bit 47–44 of the common shift register, then the lower 44 bits in the common shift register are copied to the FC1 register. If '0110b' is received for bit 47–44 of the common shift register, then the lower 17 bits in the common shift register are copied to the FC2 register. Refer to Figure 7 for a timing diagram of this command operation.
FCWRTEN (FC write enable)	15	FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

Note that FCWRTEN command must be input first, before the WRTFC command, otherwise this WRTFC command is neglected.

When inputting the WRTFC command, bit 47–bit 44 of the common shift register is used to choose which FC register be written to. See Table 3 for more detail.

Refer to Figure 7 for a detailed command input timing diagram.

3.3.3 Function Control (FC) Register FC1

FC1 is used to select BC/CC code, precharge enable, LOD caterpillar removal enable and LED open detection (LOD) voltage.

Table 4 shows the FC1 register bit assignment.

Table 4. FC1 Register Bit Assignment

Bit Number	Bit Name	Default Value (Binary)	Description
1 - 0	LODVTH	01b	LOD detection threshold voltage. These two bits select the detection threshold voltage for the LED open detection (LOD). Table 5 shows the detect voltage truth table.
3 - 2	SEL_TD0	01b	TD0 select. SOUT hold time is decided by TD0 definition and selection. Table 6 shows the detail.
4	LOD_Removal_EN	1b	LOD caterpillar Removal function enable. When this bit is ‘0’, the LOD caterpillar removal function is disabled. When this bit is ‘1’, the LOD caterpillar removal function is enabled.
7 - 5	RSV	000b	Reserved data. Input ‘0’ in this bit. Don’t care.
8	PREC_EN	0b	Pre-charge function enable. 0b — Pre-charge function enable (default) 1b — Pre-charge function disable
9	PREC_MODE3	0b	This bit is used to control a new pre-charge mode when SEL_PREC (bit 7 in FC2) = 1. 0b — Pre-charge MODE3 disable (default) 1b — Pre-charge MODE3 enable
12 - 10	RSV	000b	Reserved data. Input ‘0’ in these bits. Do not change.
13	Center Uniformity Enhancement	0b	Center Uniformity Enhancement 0b — Center Uniformity Enhancement enable 1b — Center Uniformity Enhancement disable
22 - 14	CCB	1 0000 0000b	Color brightness control data for BLUE color group (Data = 000h-1FFh. See Table 1.)
31 - 23	CCG	1 0000 0000b	Color brightness control data for GREEN color group (Data = 000h – 1FFh. See Table 1.)
40 - 32	CCR	1 0000 0000b	Color brightness control data for RED color group (Data = 000h-1FFh. See Table 1.)
43 - 41	BC	100b	Global brightness control data for all output (Data = 0h- 7h. See Table 2.)

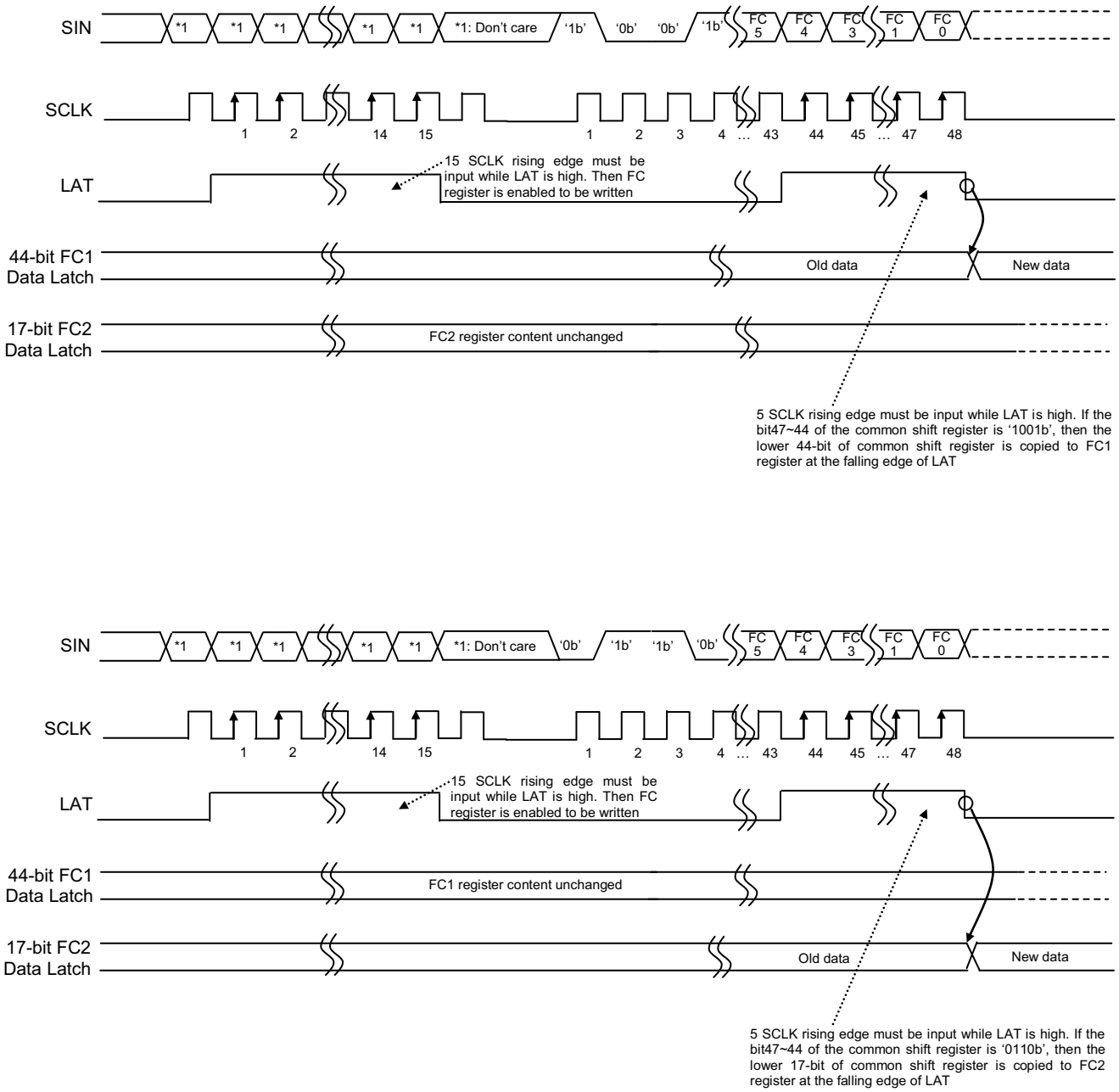


Figure 7. FC Write Enable (FCWRTEN) and FC Data Write (WRTFC) Command

Table 5. LOD Threshold Voltage Truth Table

LODVTH		LED Open Detection (LOD) Threshold Voltage
Bit 1	Bit 0	
0	0	VLOD0 (0.2-V typ)
0	1	VLOD1 (0.4-V typ, default value)
1	0	VLOD2 (0.6-V typ)
1	1	VLOD3 (0.8-V typ)

Table 6. TD0 Definition and Selection

SEL_TD0		TD0 Definition and Selection
Bit 3	Bit 2	
0	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 15 ns. Once SCLK↑ is received, after a 15 ns delay, SOUT begins change.
0	1	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 25 ns (default value when powered up). Once SCLK↑ is received, after a 25 ns delay, SOUT begins change.
1	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value 35 ns. Once SCLK↑ is received, after a 35 ns delay, SOUT begins change.
1	1	TD0 is the time from SCLK↓ to SOUT↑↓, typical value 10 ns. Once SCLK↓ is received, after a 10 ns delay, SOUT begins change. The hold time is adjustable from SCLK↑ to SOUT↑↓ by changing the duty of SCLK.

3.3.4 Function Control (FC) Register FC2

FC2 is used to select ES-PWM mode, pre-charge function, power save mode, Low-grayscale Enhancement and the multiplexing ratio.

Table 7 shows the FC2 register bit assignment.

Table 7. FC2 Register Bit Assignment

Bit Number	Bit Name	Default Value (Binary)	Description
4 - 0	MAX_LINE	0 0000b	Multiplexing ratio select. Based on the multiplexing ratio in a real application, select the correct scan line number here. Table 8 shows the scan line number vs MAX_LINE setting.
5	PSAVE_ENA	0b	Power save mode select. When this bit is '0', the power save function is disabled. This is the default value when the power is on. When this bit is '1', power save function is enabled. The TLC59581 will enter power save mode if all '0' GS data is input. If a non '0' GS data input is detected, normal mode is resumed. Refer to Figure 26 for the timing diagram of enter/exit power save mode.
6	SEL_GCLK_EDGE	0b	GCLK edge select. When this bit is '0', OUTn only turns on/off at the rising edge of GCLK, this is the default setting; When this bit is '1', OUTn turns on/off at both edges (rising and falling) of GCLK. At this condition, the maximum input GCLK is 16.5 MHz.
7	SEL_PCHG	0b	Pre-charge working mode select. Pre-charge starting point and time depend on this bit and PREC_MODE3 in FC1 register. See Figure 27 for more details.
10 - 8	RSV	000b	Reserved data. Input '0' in this bit. Do not change.
11	EMI_REDUCE_B	0b	EMI reduce select for blue channels. When this bit is '0', EMI noise contributed by blue channels is reduced. When this bit is '1', EMI noise contributed by blue channels is at default value. However, low grayscale visual effect will be better.
12	EMI_REDUCE_G	0b	EMI reduce select for green channels. When this bit is '0', EMI noise contributed by green channels is reduced. When this bit is '1', EMI noise contributed by green channels is at the default value. However, low grayscale visual effect will be better.
13	EMI_REDUCE_R	0b	EMI reduce select for red channels. When this bit is '0', EMI noise contributed by red channels is reduced. When this bit is '1', EMI noise contributed by red channels is at default value. However, low grayscale visual effect is better.
14	SEL_PWM	0b	ES-PWM mode select. When this bit is '0', 8MSB + 8LSB mode is chosen. The whole 65536 GCLK display period is divided into 256 segments. Each segment includes 257 GCLK. LED turn on time is scattered in these 256 segments. When this bit is '1', 7MSB + 9LSB mode is chosen. The whole 65536 GCLK display period is divided into 512 segments. Each segment includes 129 GCLK. LED turn on time is scattered in these 512 segments. See Section 3.6.2, Multiplexed Enhanced Spectrum (ES) PWM Control for more details.
16 - 15	1st-Line Enhancement	01b	These two bits improve the first line issue at low grayscale condition. 00b — no improvement 01b — Typical value 10b — medium improvement 11b — strong improvement
18 - 17	RSV	00b	Reserved data. Input '0' in this bit. Do not change.
19	RSV_HIGH	1b	Reserved data. Input '1' in this bit. Do not change.
23 - 20	LGSE1-B	0000b	These four bits improve blue low-grayscale uniformity. Total of 16 steps. The compensation level increases with the value of LGSE1-B. For example, '0000b' means no compensation. '1111b' means highest compensation.
27 - 24	LGSE1-G	0000b	These four bits improve green low-grayscale uniformity. Total of 16 steps. The compensation level increases with the value of LGSE1-G. For example, '0000b' means no compensation. '1111b' means highest compensation.

Table 7. FC2 Register Bit Assignment (continued)

Bit Number	Bit Name	Default Value (Binary)	Description
31 - 28	LGSE1-R	0000b	These four bits improve red low-grayscale uniformity. Total of 16 steps. The compensation level increases with the value of LGSE1-R. For example, '0000b' means no compensation. '1111b' means highest compensation.
33 - 32	Interference_B	00b	These two bits improve the interference issue between high GS data and low GS data in blue color. 00b — low improvement 01b — typical value 10b — medium improvement 11b — strong improvement
35 - 34	Reverse_V_B	00b	These two bits control reverse voltage in blue color. 00b — High 01b — Medium High 10b — Medium 11b — Low
37 - 36	Interference_G	00b	These two bits improve the cross interference issue between high GS data and low GS data in green color. 00b — low improvement 01b — typical value 10b — medium improvement 11b — strong improvement
39 - 38	Reverse_V _G	00b	These two bits control reverse voltage in green color. 00b — High 01b — Medium High 10b — Medium 11b — Low
41 - 40	Interference_R	00b	These two bits improve the interference issue between high GS data and low GS data in red color. 00b — low improvement 01b — typical value 10b — medium improvement 11b — strong improvement
43 - 42	Reverse_V_R	00b	These two bits control reverse voltage in red color. 00b — High 01b — Medium High 10b — Medium 11b — Low

Table 8. Scan Line Number VS MAX_LINE Setting

MAX_LINE (Bit 4–bit 0)	Scan Line Number
0 0000b	1
0 0001b	2
0 0010b	3
…	…
0 1111b	16
…	…
1 1101b	30
1 1110b	31
1 1111b	32

3.4 Step 3 — Write GS Data Into One Memory BANK

3.4.1 Overview of the Memory Structure

The bottleneck for a traditional PWM LED driver to realize a high visual refresh rate is the GS data transmission limitation. To remove this limitation, the TLC59581 has 48Kb display memory implemented. With this memory size, a multiplexing LED display system with from 1 up to 32 duty ratio (that is, 32 multiplexing) is supported.

The memory is divided into two BANKs: BANK A and BANK B. One is read for the current display image, the other one is written with GS data of the next display image. This BANK selection is decided by the BANK_SEL bit which is an internal flag bit. At power on, BANK_SEL = 0, thus BANK A is selected to be written with GS data for next frame, while the GS data in BANK B is read out for current frame display. When the time of one frame has elapsed, input the Vsync command (see Section 3.4.2 for details) and the usage of these two BANKs is exchanged.

With this method, TLC59581 can display the image of current frame at a very high refresh rate, without the limitation of GS data transmission. See Figure 8 for this BANK select mode change.

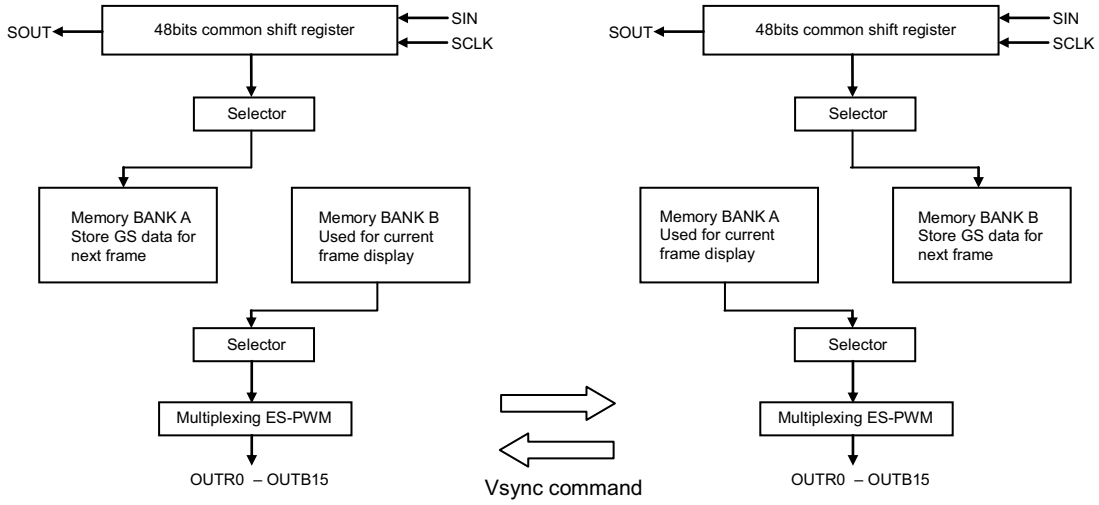


Figure 8. BANK Select Mode Change

3.4.2 What is the Vsync Command?

Vsync is the vertical frame synchronization command. When the period of one frame ends, input this command to exchange the usage of the two memory BANKs, then the new image in the other BANK is displayed in the coming frame period.

If 3 SCLK rising edges are detected during LAT high period, then the TLC59581 considers this as a Vsync command.

Table 9. Vsync Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
Vsync (Vertical Synchronization)	3	Vertical synchronization signal. When this command is received, BANK_SEL bit is toggled, and all counters are reset to 0. A new frame image is displayed in the coming frame period. Refer to Figure 9 for a timing diagram of this command operation.

All the internal counters are initiated once the Vsync command is received. Figure 9 shows the timing of the Vsync command.

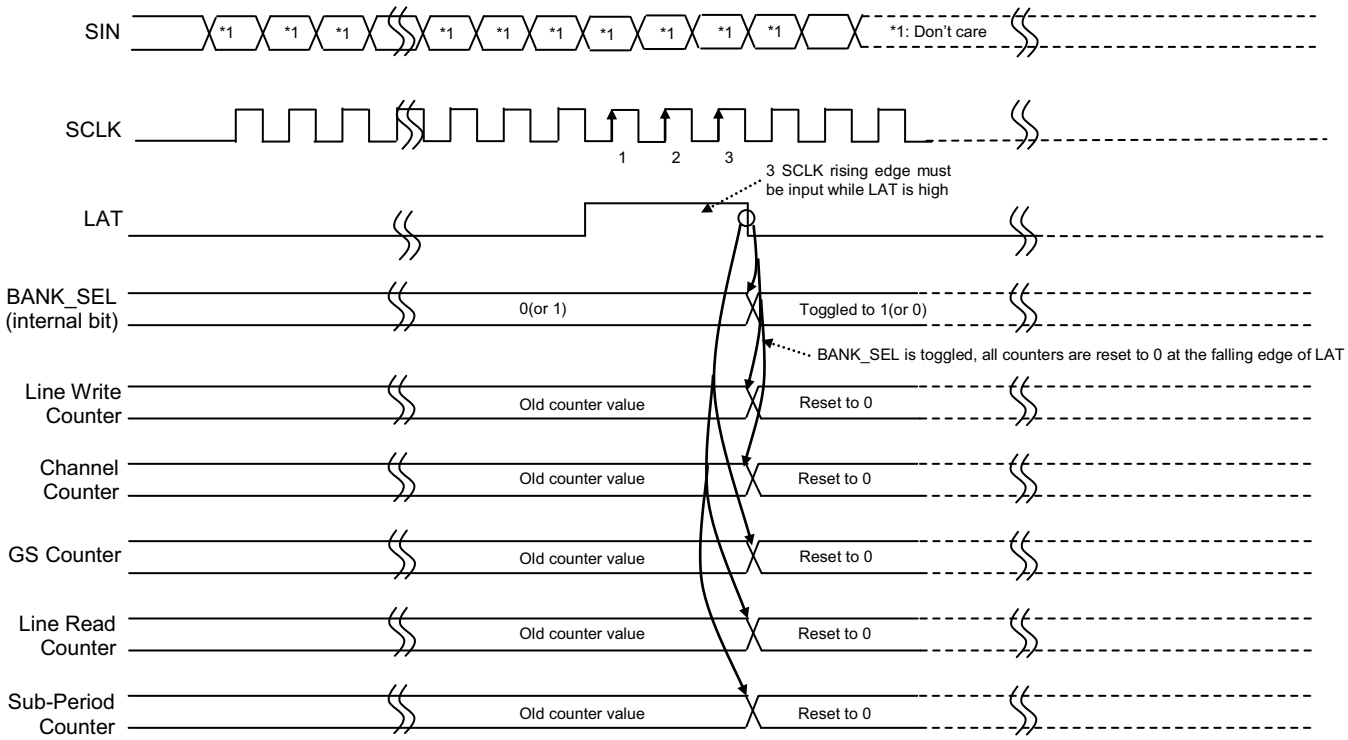


Figure 9. Vertical Synchronization (Vsync) Command

3.4.3 Detail of the Memory BANK

Each BANK contains all the GS data of 32 scan lines. Each line is comprised of sixteen 48-bits-width memory units. Each unit contains the R/G/B grayscale (GS) data of one channel. For example, the memory unit for channel 0 contains 16-bit GS data for OUTR0, 16-bit GS data for OUTG0, and 16-bit GS data for OUTB0. Figure 10 shows the bit arrangement of this memory unit. In this example, bit 32–47 contain the 16-bit GS data for OUTB0 (pin 10 of the IC) for line x.

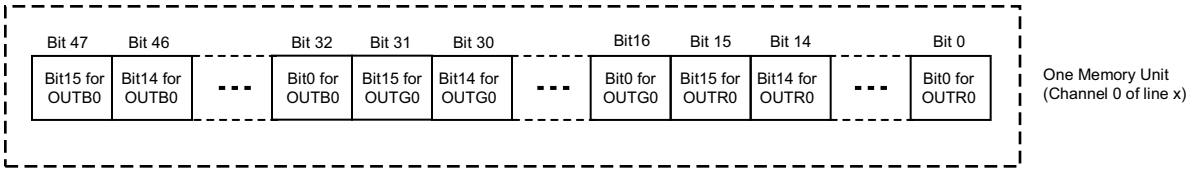


Figure 10. Bit Arrangement of One Memory Unit

Depending on the scan line number selected in the FC2 register (bit 4–0), the total memory units that must be written in one BANK is: 16 × scan_line_number. For example, if choosing 32 multiplexing, then write 512 (32 × 16 = 512) memory units during one frame period. Figure 12 shows the detailed memory structure.

3.4.4 Write GS Data to One Memory Unit (48-bit Width) With the WRTGS Command

If TLC59581 detected one SCLK rising edge during the LAT high period, it considers this as a WRTGS command, and will latch the data of the common shift register into one memory unit (48-bit width) at the falling edge of LAT.

The data of the common shift register is latched into the memory unit according to the following bit sequence. When shifting GS data into the common shift register, input bit 15 of OUTBn (Blue color) first.

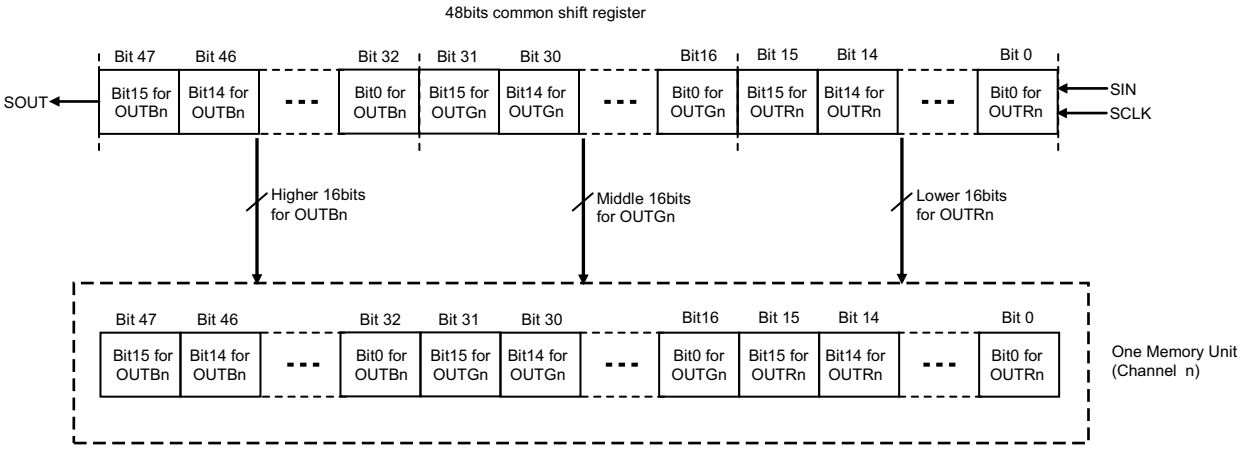


Figure 11. Latch Common Shift Register Data Into One Memory Unit

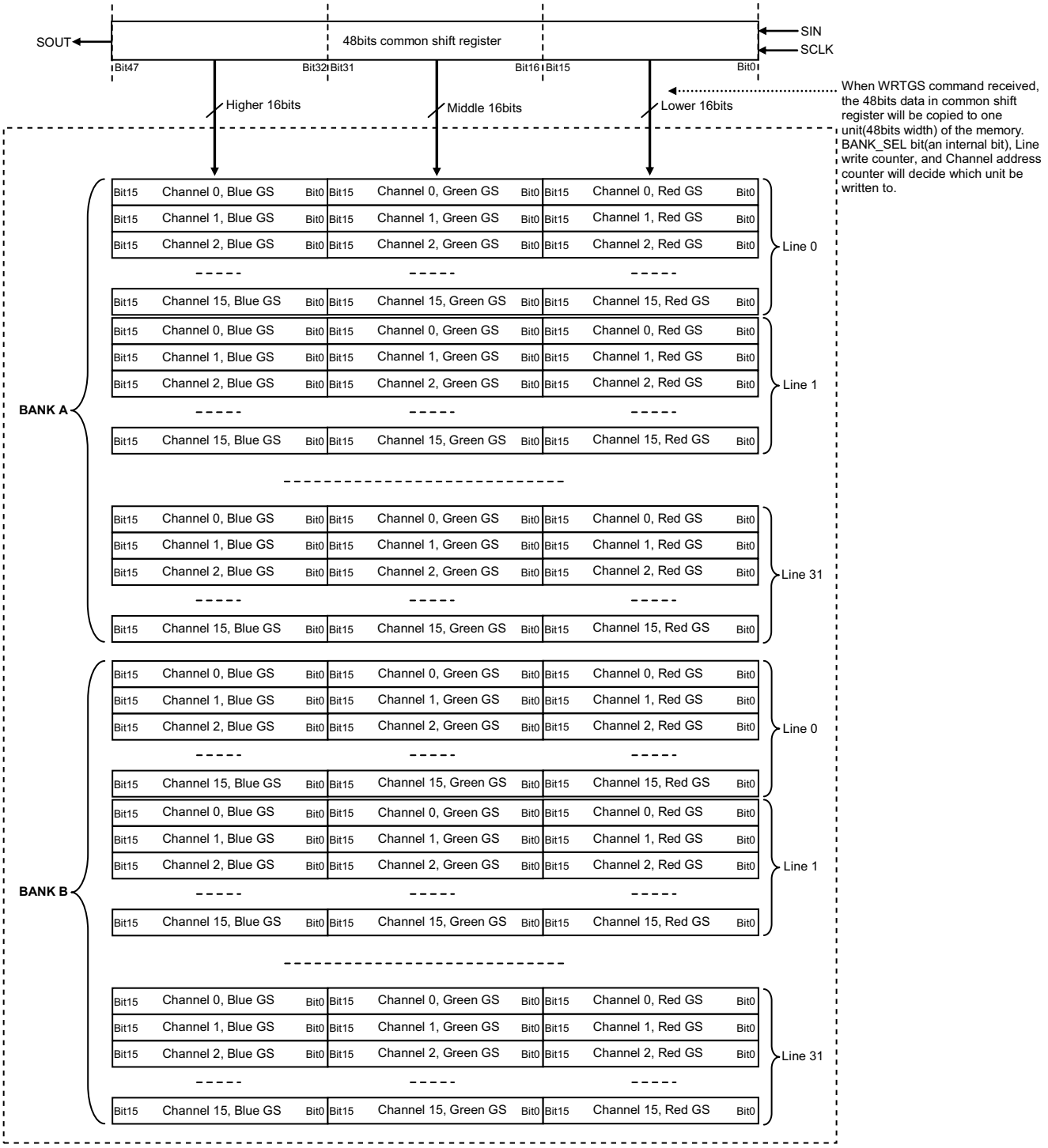


Figure 12. Memory Structure

BANK_SEL bit (an internal bit), line write address counter, and channel address counter decide which unit is written.

Figure 13 shows the timing of this command.

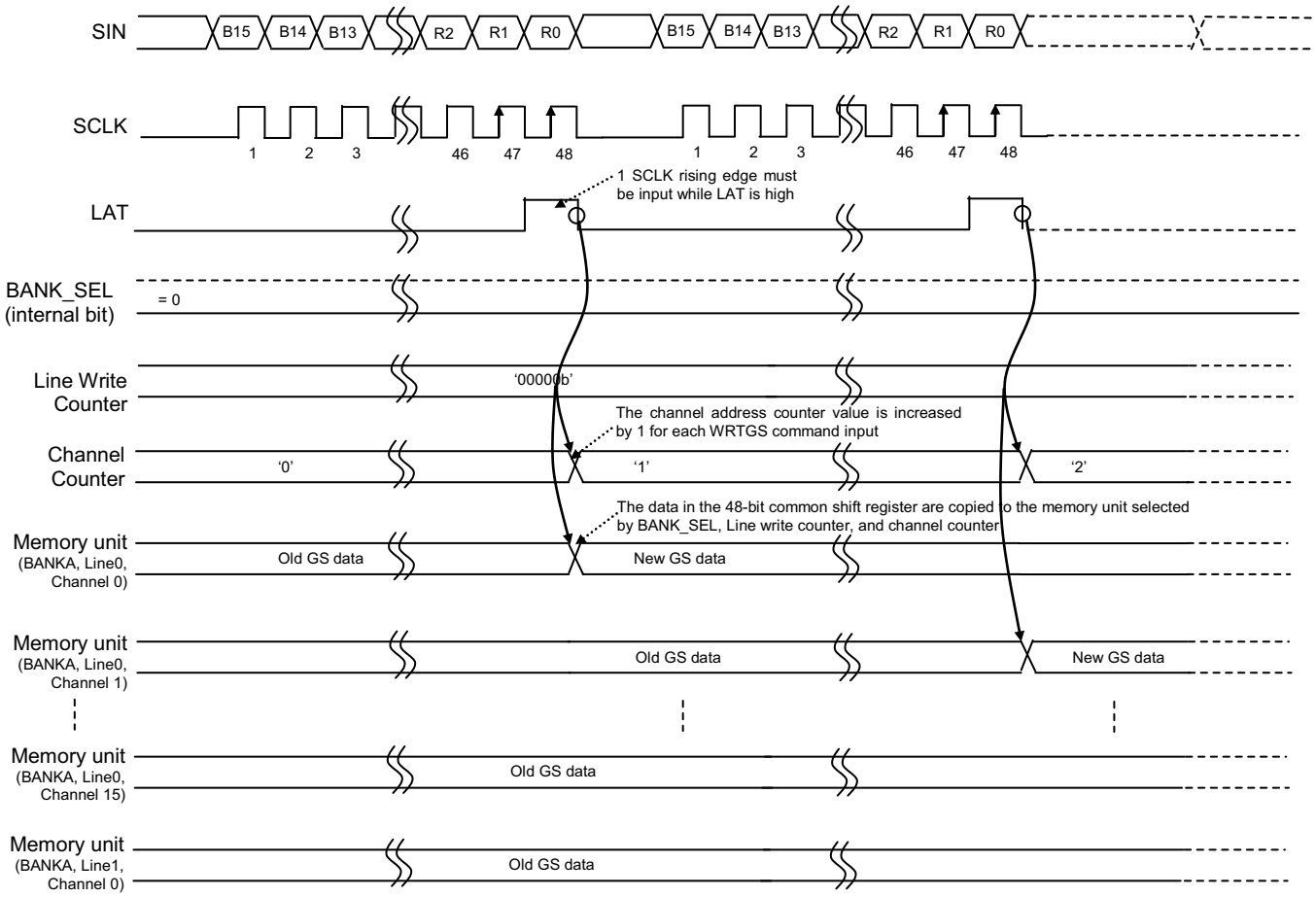


Figure 13. 48-bit GS Data Write (WRTGS) Command

3.4.5 Write GS Data to One Memory BANK

One BANK contains maximum memory units (48-bits-width) number is: 32 lines × 16 channels = 512.

Depending on the multiplexing ratio selected in the FC2 register (bit 4–0), the total memory units must be written in one BANK is: 16 × scan_line_number. Users should write to these memory units one by one, sequentially. A detailed description follows.

After power on, the BANK_SEL bit, line write counter, and channel counter are reset to 0. Thus, the memory unit of BANK A, line 0, channel 0 is selected to be written with the 48-bit GS data in the common shift register when the WRTGS command is received.

After that, the channel counter increments 1, then the memory unit of BANK A, line 0, and channel 1 are copied with the 48-bit data in the common shift register with the next WRTGS command input.

In this sequence, when all sixteen channels of the memory unit of line 0 have been written, the channel counter is higher than 15. At this moment, the channel counter is reset to 0, and the line counter increments 1.

Next, the sixteen-channel memory unit of line 1 is written one by one in same method. When line1 is finished, line counter increments 1, and the sixteen channels of line 2 are written.

In this manner, when the line counter goes higher than MAX_LINE (see Table 8), all scan lines have been updated with new GS data, then the line counter is reset to 0. See Figure 14 for this timing diagram.

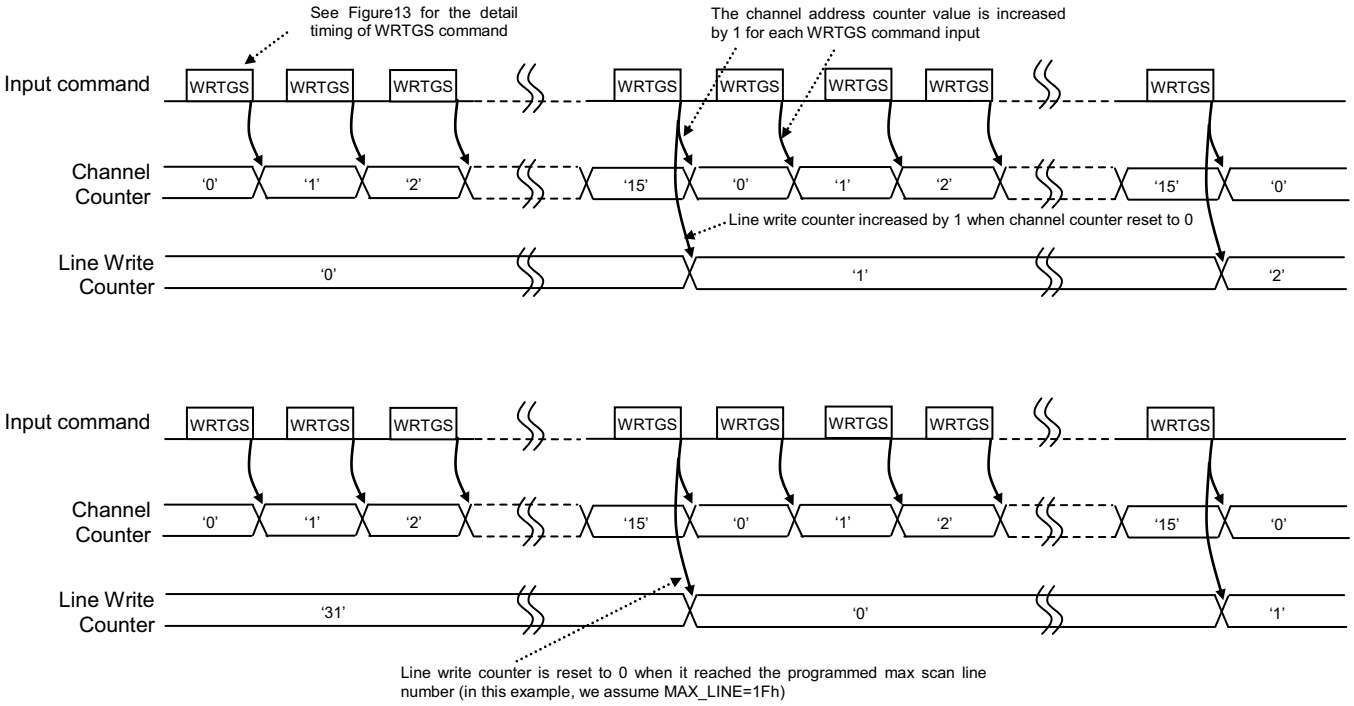


Figure 14. Memory Write Sequence

3.5 Step 4 — Send Vsync Command to Switch the BANK Purpose

Send Vsync command, then the BANK to which the GS data had been written in the previous step is displayed in the coming frame period. See Figure 9 to learn how to send the Vsync command.

3.6 Step 5 — Input GCLK to Begin Displaying the Image of One New Frame

Input GCLK continuously, 257 GCLK (or 513 GCLK) as a segment. Between the interval of two segments, switch LED supply voltage from one line to next line accordingly.

Since the TLC59581 needs time to prepare GS data for the 1st line of a new frame, after sending the Vsync command (falling edge of LAT pulse), some wait time (2.5 µs) is needed before sending the first GCLK.

3.6.1 Basic Knowledge: What is PWM Control?

PWM control means pulse width modulation (PWM) control scheme, which controls the OUTx pin turn on ratio during one display period proportional to the grayscale (GS) data of this channel. The use of 16-bits GS data per channel results in 65536 brightness steps, from 0% up to 100% brightness.

For example:

- If GS = 0, then OUTx will not turn on during one display period (65536 GCLK period totally), the brightness is 0%
- If GS = 500, then during one display period, OUTx turns on 500 GCLK period, then the brightness ratio is 500/65535 = 0.763% (Assume 100% brightness if 65535 GCLK period is turn on during one display period)
- If GS = 65534, then during one display period, OUTx turns on 65534 GCLK period, then the brightness ratio is 65534/65535 = 99.9985%

3.6.2 Multiplexed Enhanced Spectrum (ES) PWM Control

The TLC59581 is designed mainly for multiplexed display systems, using an innovative multiplexed ES PWM method to improve the visual refresh rate while maintaining the best grayscale performance.

Two PWM modes can be selected: 8-bit MSB + 8-bit LSB (8+8) mode, and 9-bit MSB + 7-bit LSB (9+7) mode. This is decided with the SEL_PWM (bit 14 of FC2 register).

3.6.2.1 8+8 Mode ES PWM Control

When SEL_PWM (bit 14 of FC2 register) = 0, ES-PWM is in 8MSB + 8LSB mode.

In the conventional 8MSB + 8LSB ES-PWM control, one total display period (include 65536 GCLK period) is divided to 256 display segments. Each segment has 256 GCLK periods. The OUTx total on-time during one display period is distributed evenly in these 256 segments. By this means, the visual refresh rate is increased by 256 times.

This is a good method for a static display system, but not good for a multiplexed (dynamic) display system. If one finished all 256 segments of one scan line, then changes to display another scan line, the refresh rate is very low.

In the TLC59581's multiplexed ES PWM control, one display period is divided into 256 sub-periods, which corresponds to the 256 segments of the conventional ES-PWM. During one sub-period, all scan lines display their corresponding segment sequentially. When all scan lines finish their segment, this sub-period ends, and next sub-period starts. Because each scan line has a chance to display in one sub-period, the visual refresh rate is 256 times higher than that of the conventional ES-PWM control.

The time of one sub-period determines the visual refresh rate, as Equation 3 shows:

$$f_{Refresh} = 1/t_{Sub\text{-}period} \quad (3)$$

where

- $f_{Refresh}$ is the visual refresh rate
- $t_{Sub\text{-}period}$ is the time of one sub-period needed

Figure 15 shows the timing of multiplexed ES PWM operation in 8+8 mode.

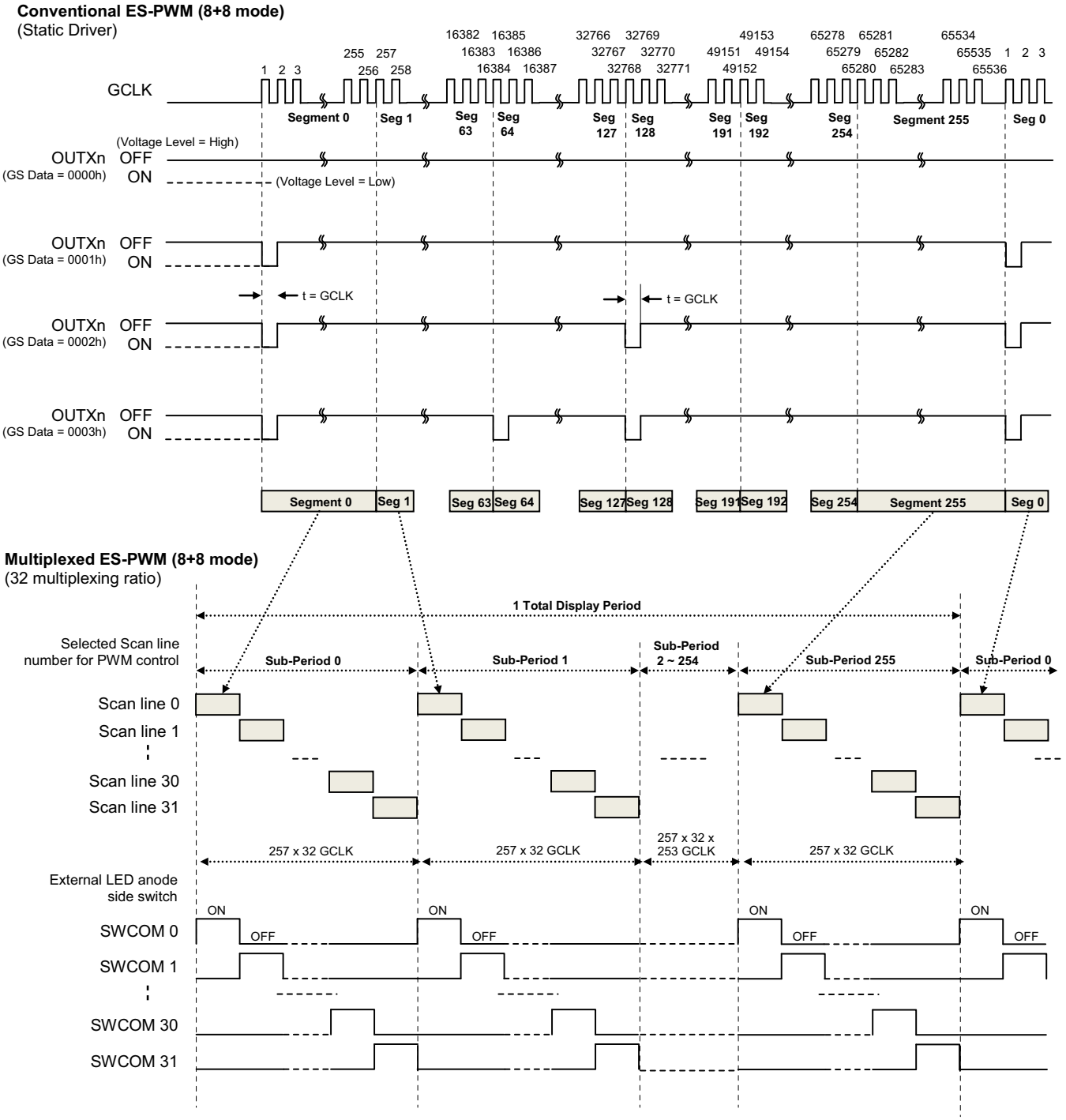


Figure 15. Multiplexed ES-PWM Operation (8+8 Mode)

3.6.2.2 7+9 Mode ES PWM Control

When SEL_PWM (bit 14 of FC2 register) = 1, ES-PWM is in 7MSB + 9LSB mode.

In the conventional 7MSB +9LSB ES-PWM control, one total display period (include 65536 GCLK period) is divided to 512 display segments. Each segment has 129 GCLK periods. The OUTx total on-time during one display period is distributed evenly in these 512 segments. By this means, the visual refresh rate is increased by 128 times.

This is a good method for a static display system, but not good for a multiplexed (dynamic) display system. If one finished all 512 segments of one scan line, then changes to display another scan line, the refresh rate is very low.

In the TLC59581's multiplexed ES PWM control, one display period is divided into 512 sub-periods, which correspond to 512 segments of the conventional ES-PWM. During one sub-period, all scan lines display their corresponding segment sequentially. When all scan lines finish their segment, this sub-period ends, and next sub-period starts. Because each scan line has a chance to display in one sub-period, thus the visual refresh rate is 512 times higher than that of the conventional ES-PWM control.

Figure 17 shows the timing of multiplexed ES PWM operation in 7+9 mode.

3.6.3 How to Input GCLK and Address of Lines for Multiplexing

Example: 8+8 Mode, Multiplexing Ratio 1/32

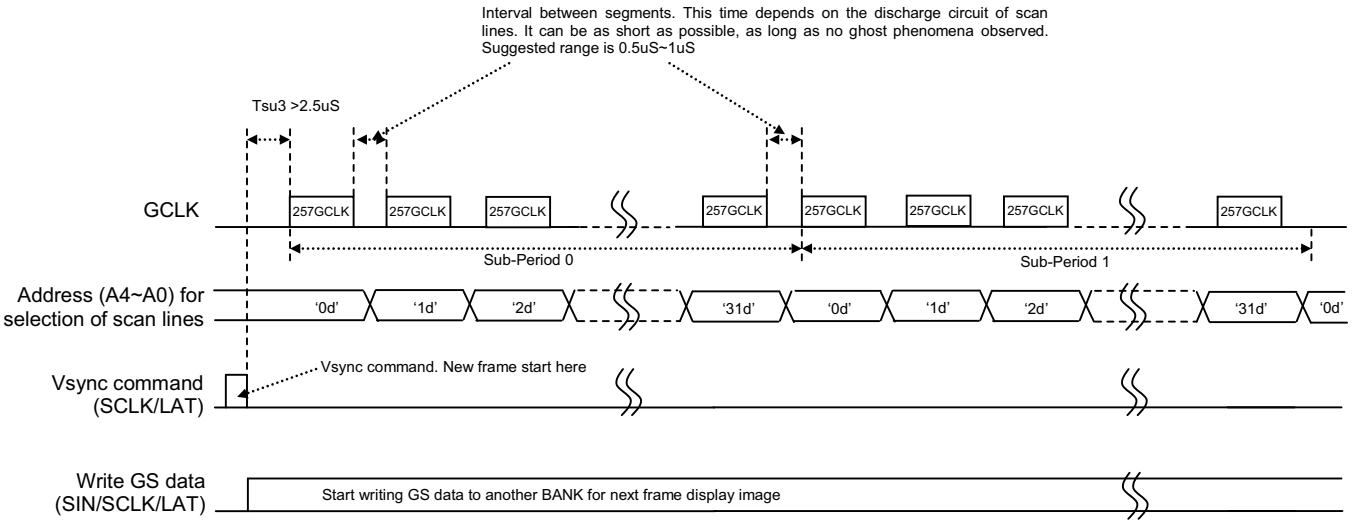


Figure 16. Controller Timing Sequence, 8+8 Mode, 32 Multiplexing

Example: 7+9 Mode, Multiplexing Ratio 1/32

Same timing sequence as 8+8 mode, except 129 GCLK per segment instead of 257 GCLK per segment.

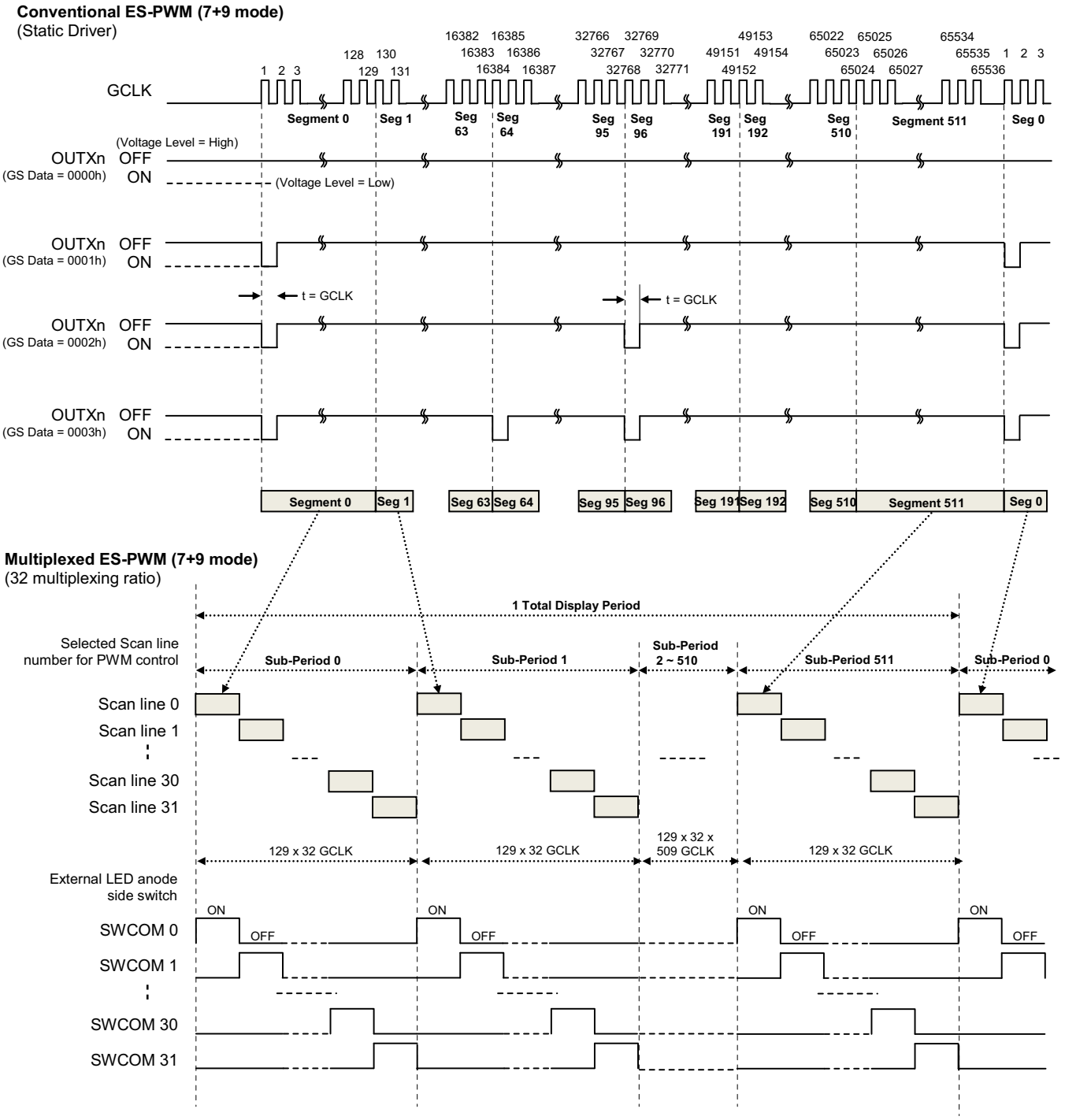


Figure 17. Multiplexed ES-PWM Operation (7+9 Mode)

3.7 Step 6 — During the Same Period of Step 5, Write GS Data for Next Frame Into Another BANK

See Figure 16 for details.

3.8 Step 7 — When the Time of One Frame Ends, Input the Vsync Command to Swap the Purpose of the Two BANKs

Example: A big picture of the timing sequence, 7+9 mode

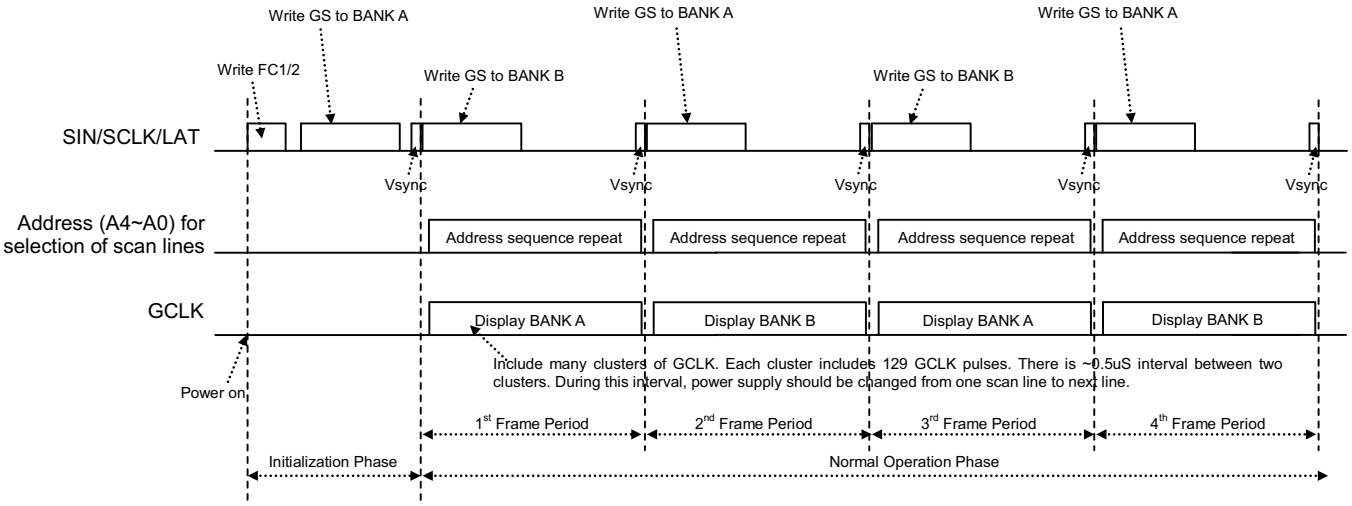


Figure 18. Timing Sequence, 7+9 Mode

3.9 LED Open Detection (LOD)

3.9.1 How Does LOD Operate?

LOD function detects a fault caused by an open circuit in any LED string or a short from OUTXn to ground with low impedance, by comparing the OUTXn voltage to the LOD detection threshold voltage level set by LODVLT in the FC1 register (see Table 5). If the OUTXn voltage is lower than the programmed voltage, the corresponding output LOD bit is set to '1' to indicate an open LED. Otherwise, the output of that LOD bit is '0' (see Figure 19). LOD data output by detect circuit are valid only during the 'on' period of that OUTXn output channel. LOD data are always '0' for outputs that are turned off.

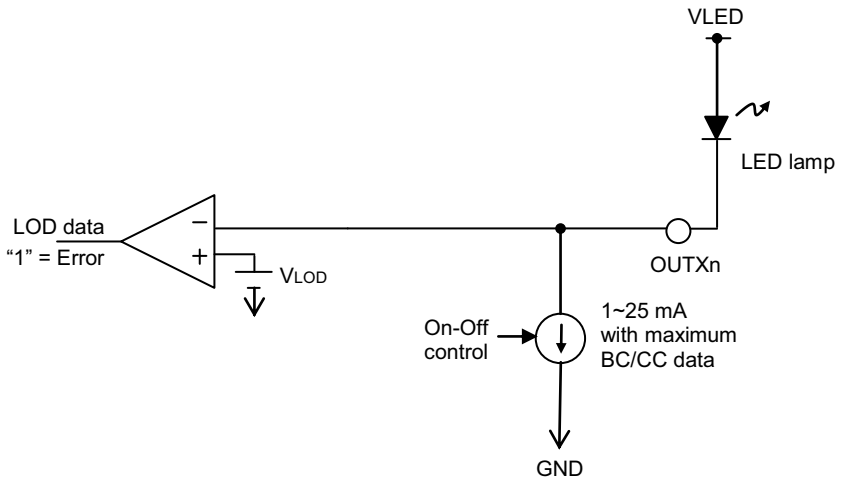


Figure 19. LOD Detect Circuit Of One Channel

The output of the LOD detect circuit is loaded into the 48-bit register called SID holder (Figure 20 shows the bit arrangement of this SID holder) at the rising edge of the 33th GCLK in each segment. To get a correct detecting result, it is necessary to make sure OUTXn is kept 'on' in the 33th GCLK period in one segment. See Figure 21 for the timing diagram.

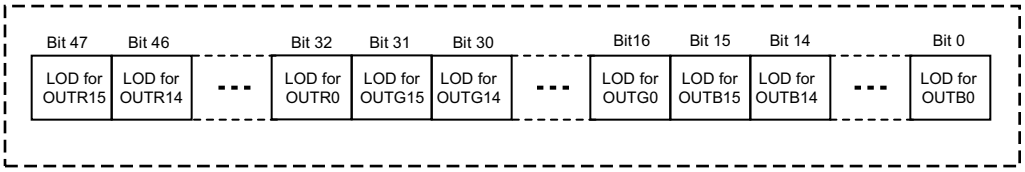
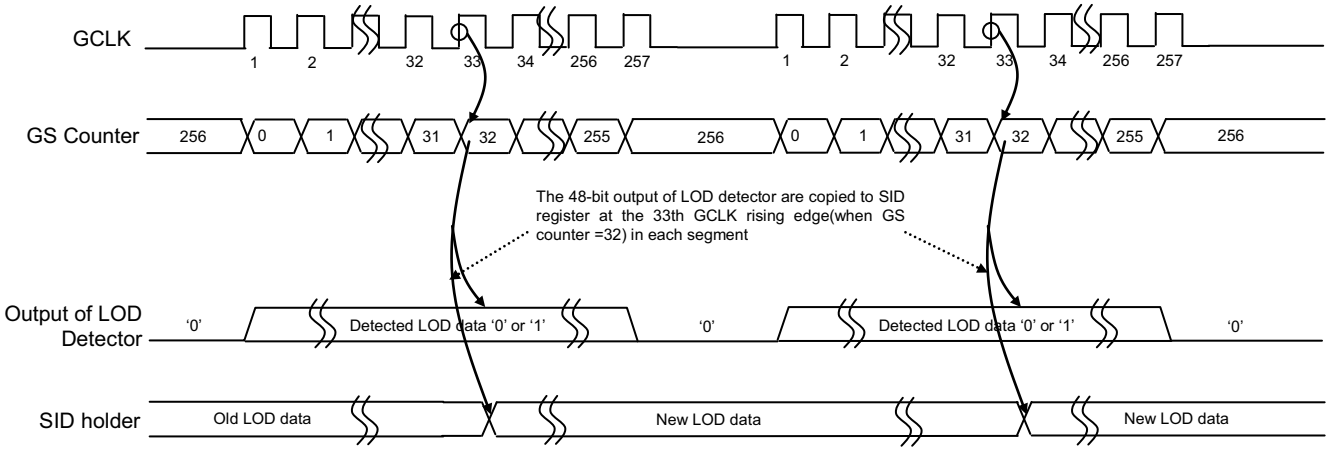


Figure 20. Bit Arrangement of the SID Holder

8+8 mode (SEL_PWM=0):



7+9 mode (SEL_PWM=1):

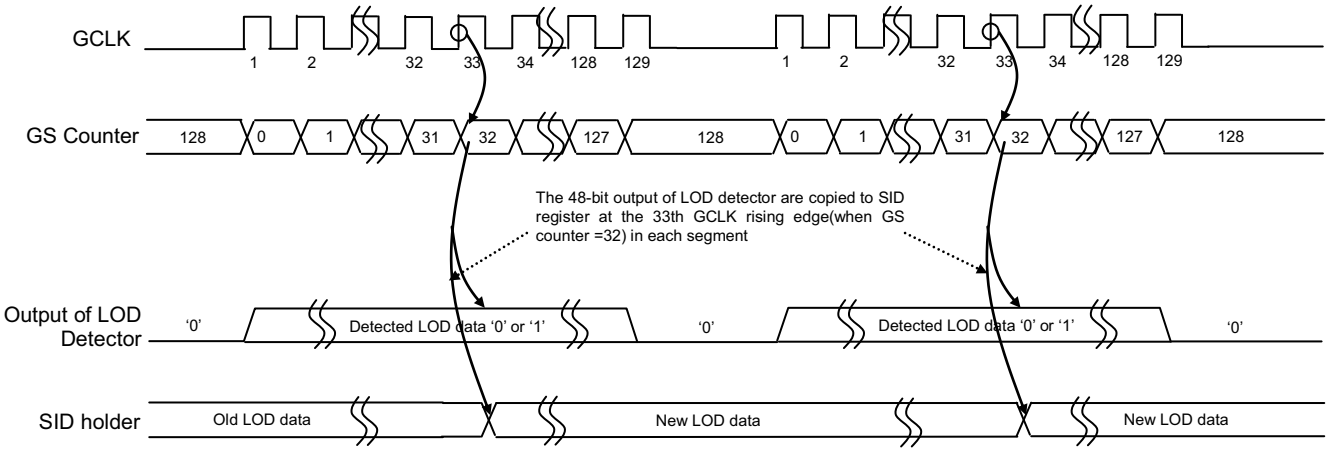


Figure 21. LOD Information Latch Into SID Holder

3.9.2 Read LOD Information With the READSID Command

Once the TLC59581 detected 7 rising edges of SCLK during LAT high period, it considers this as a READSID command. The 48-bit data in SID holder is latched into common shift register at the falling edge of LAT signal. After that, input 48 SCLK pulse to shift out the LOD data at the SOUT pin. Figure 22 shows this timing diagram.

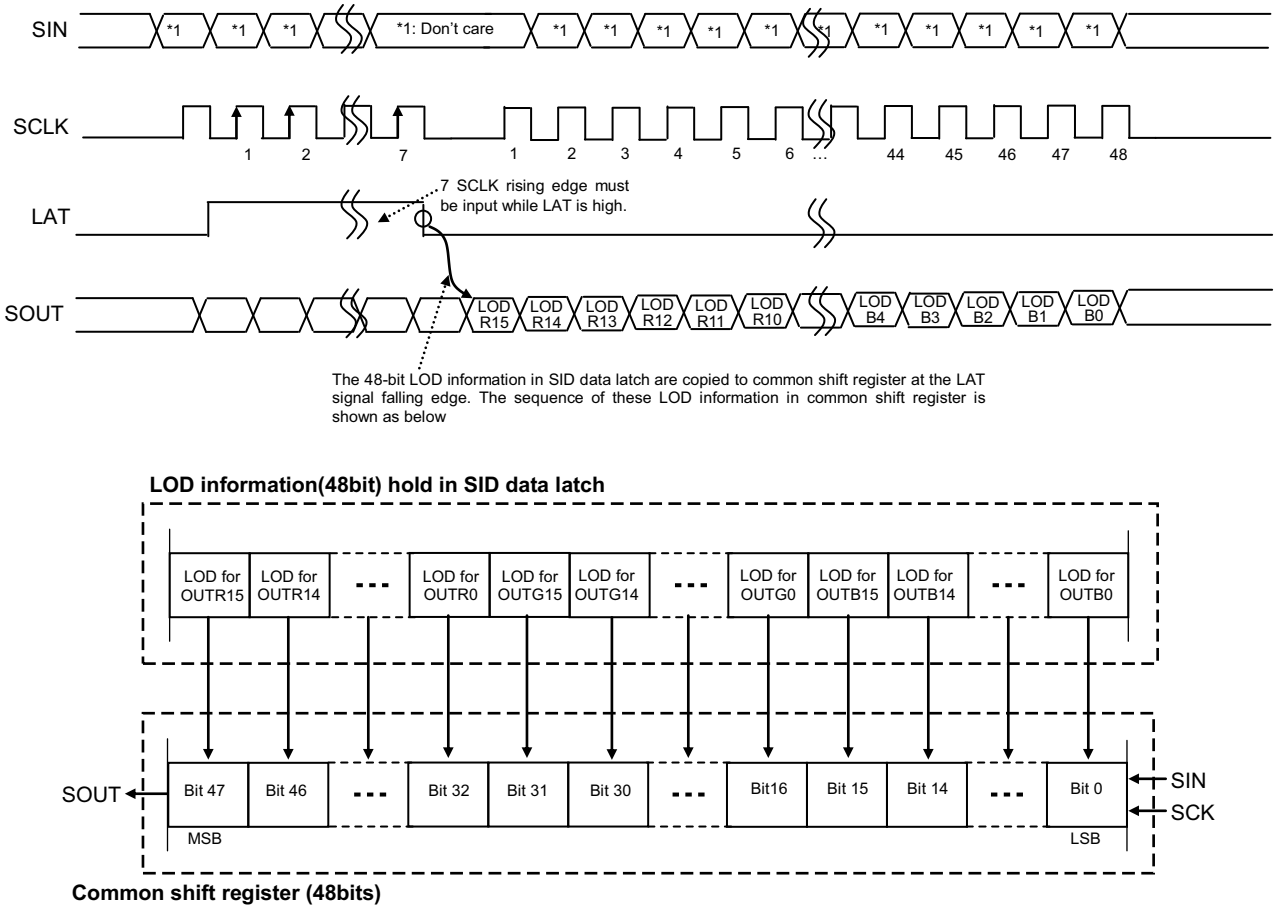


Figure 22. LOD Information Read (READSID) Timing

3.9.3 Suggested LED Open Detection Process

Figure 23 shows the flow of the LOD detection process.

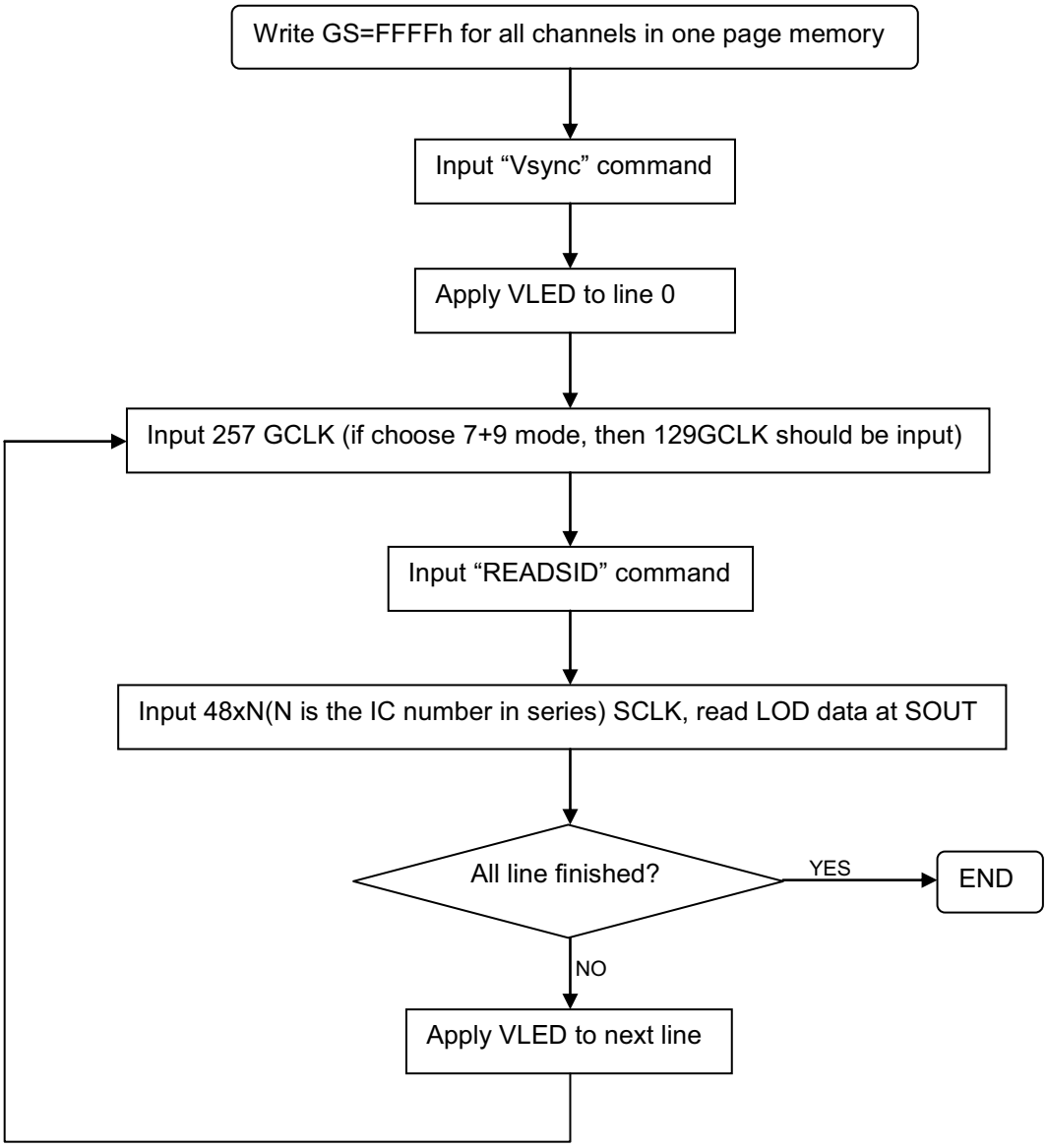


Figure 23. Example of LOD Detection Process (8+8 Mode)

3.10 How to Read the Function Control Register

Once TLC59581 detected 10 rising edges of SCLK during the LAT high period, it considers this as a READFC1 command. The 44-bit data in the FC1 register is latched into the lower 44 bits of the common shift register at the falling edge of the LAT signal. Other bits in the common shift register are reset to 0.

Once the TLC59581 detected 11 rising edges of SCLK during the LAT high period, it considers this as a READFC2 command. The 17-bit data in the FC2 register is latched into the lower 17 bits of the common shift register at the falling edge of the LAT signal. Other bits in the common shift register are reset to 0.

Next, the loaded data can be read out from SOUT synchronized with the SCLK rising edge.

Refer to Figure 24 and Figure 25 for the timing diagram of these two commands.

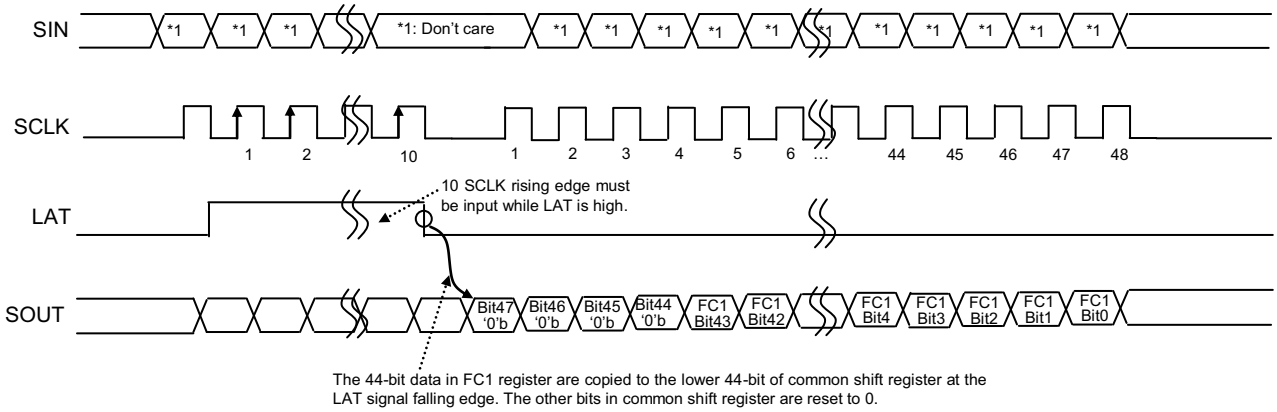


Figure 24. FC1 Data Read (READFC1) Command

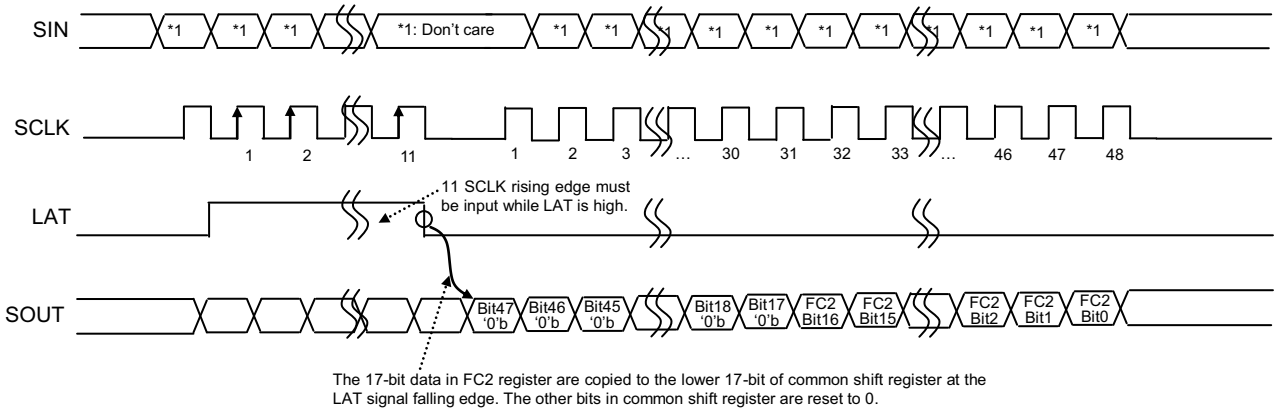


Figure 25. FC2 Data Read (READFC2) Command

3.11 Function Commands Summary

Table 10 lists a summary of all the seven commands that can be input with SCLK and LAT signals: WRTGS, VSYNC, WRTFC, READSID, READFC1, READFC2, and FCWRTEN.

Table 10. Function Commands Summary

Command Name	SCLK Rising Edges While LAT is High	Description
WRTGS (48-bit GS data write)	1	The 48-bit data in the common shift register are copied to the memory unit selected by channel address counter, line write counter, and BANK_SEL bit. Refer to Figure 13 for a timing diagram of this command operation.
Vsync (Vertical Synchronization)	3	Vertical synchronization signal. When this command is received, the BANK_SEL bit is toggled, and all counters are reset to 0. New frame images are displayed in the coming frame period. Refer to Figure 9 for a timing diagram of this command operation.
WRTFC (FC data write)	5	The lower 44-bit data or the lower 17-bit data in the common shift register are copied to the FC1 or FC2 register. Bit 47–44 of the common shift register are used to choose which FC register is written to. If '1001b' is received for bit 47–44 of the common shift register, then the lower 44-bits in the common shift register are copied to the FC1 register. If '0110b' is received for bit 47–44 of the common shift register, then the lower 17 bits in the common shift register are copied to the FC2 register. Refer to Figure 7 for a timing diagram of this command operation.
READSID (SID data read)	7	The 48-bit LOD data in the SID data latch are copied to the 48-bit shift register. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 21 for a timing diagram of this command operation.
READFC1 (FC1 data read)	10	The 44-bit data in the FC1 register are copied to the lower 44 bits of the shift register. Other bits in the shift register are reset to 0. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 24 for a timing diagram of this command operation.
READFC2 (FC2 data read)	11	The 17-bit data in the FC2 register are copied to the lower 17 bits of the shift register. Other bits in the shift register are reset to 0. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 25 for a timing diagram of this command operation.
FCWRTEN (FC write enable)	15	FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

3.12 Power-Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSAVE_ENA (bit5 of FC2 register) to '1'. When the power is on, this bit default is '0'.

When this function is enabled, if all the GS data received for next frame are '0', IC enters power-save mode at the moment the Vsync command is input.

In power-save mode, the IC detects if non-zero GS data is input for next frame. Among all the GS data for next frame, if anyone is non-zero, it starts to resume normal mode once finishing the whole GS input for next frame. See Figure 26 for the timing diagram.

In power-save mode, if all analog circuits like constant current output, LOD circuit, and so forth, do not work, the device total current consumption I_{CC} is below 1 mA.

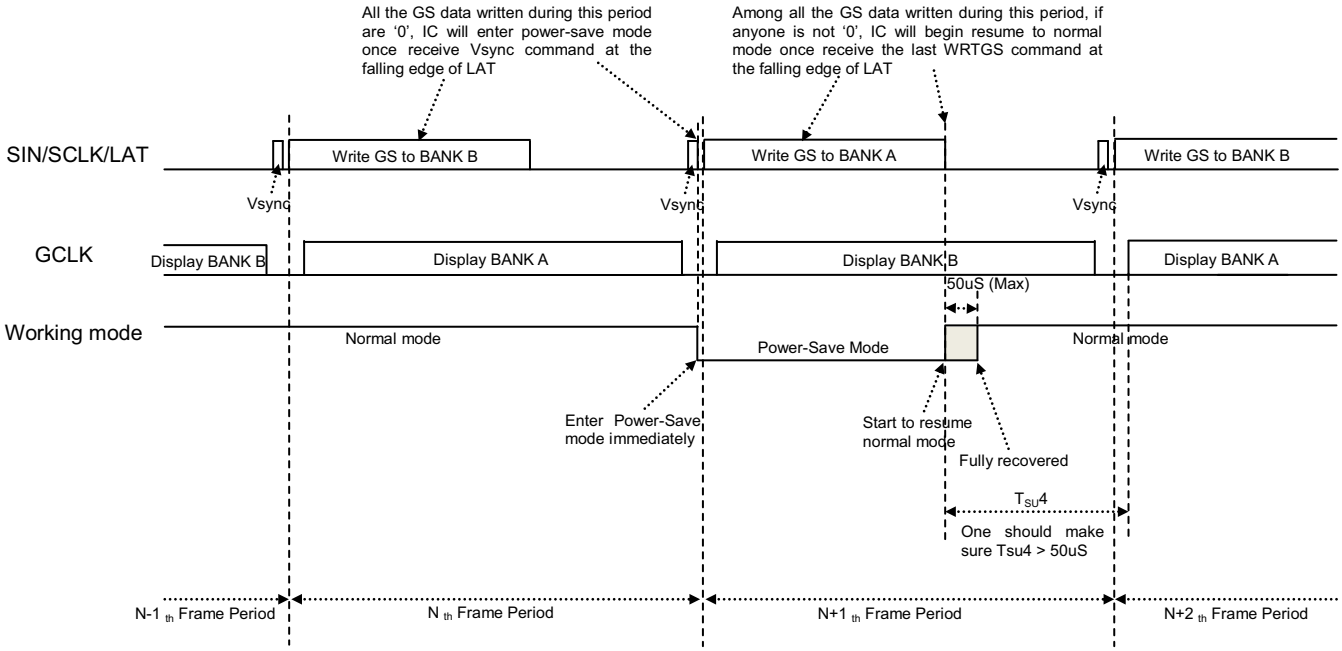


Figure 26. Enter/Exit Power-Save Mode

3.13 Pre-Charge Function

The internal pre-charge FET is implemented to remove ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current for parasitic capacitance of OUTXn through the LED when the supply voltage switches from one common line to next common line.

To prevent this unwanted charging current, the TLC59581 uses an internal FET to pull OUTXn during the common line switching period. Thus, no charging current flows through the LED and the ghosting is eliminated.

Three pre-charge working modes can be selected by SEL_PCHG, bit 7 of FC2 and PREC_MODE3, bit 9 of FC1. Table 11 shows the pre-charge function truth table.

Table 11. Pre-Charge Function Mode

EL_PCHG Bit 7 of FC2	PREC_MODE3 Bit 9 of FC1	Pre-Charge Function Mode
0	--	Mode 1
1	0	Mode 2
1	1	Mode 3

Take the 8+8 mode as the example. Pre-charge mode1, the pre-charge FET only remains off during the period in which the channel is on.

Pre-charge mode2, the pre-charge FET remains off during the whole segment period (257 GCLK period), and only remains on during the dead-time (the time between two adjacent segments).

Pre-charge mode3, the pre-charge FET remains off during the first half segment period (1 to 128 GCLK of the 257 GCLK period), and only keep on during the last half segment period (129 to 257 GCLK of the 257GCLK period) and the dead-time (the time between two adjacent segments).

Figure 27 shows these differences (take 8+8 mode as example).

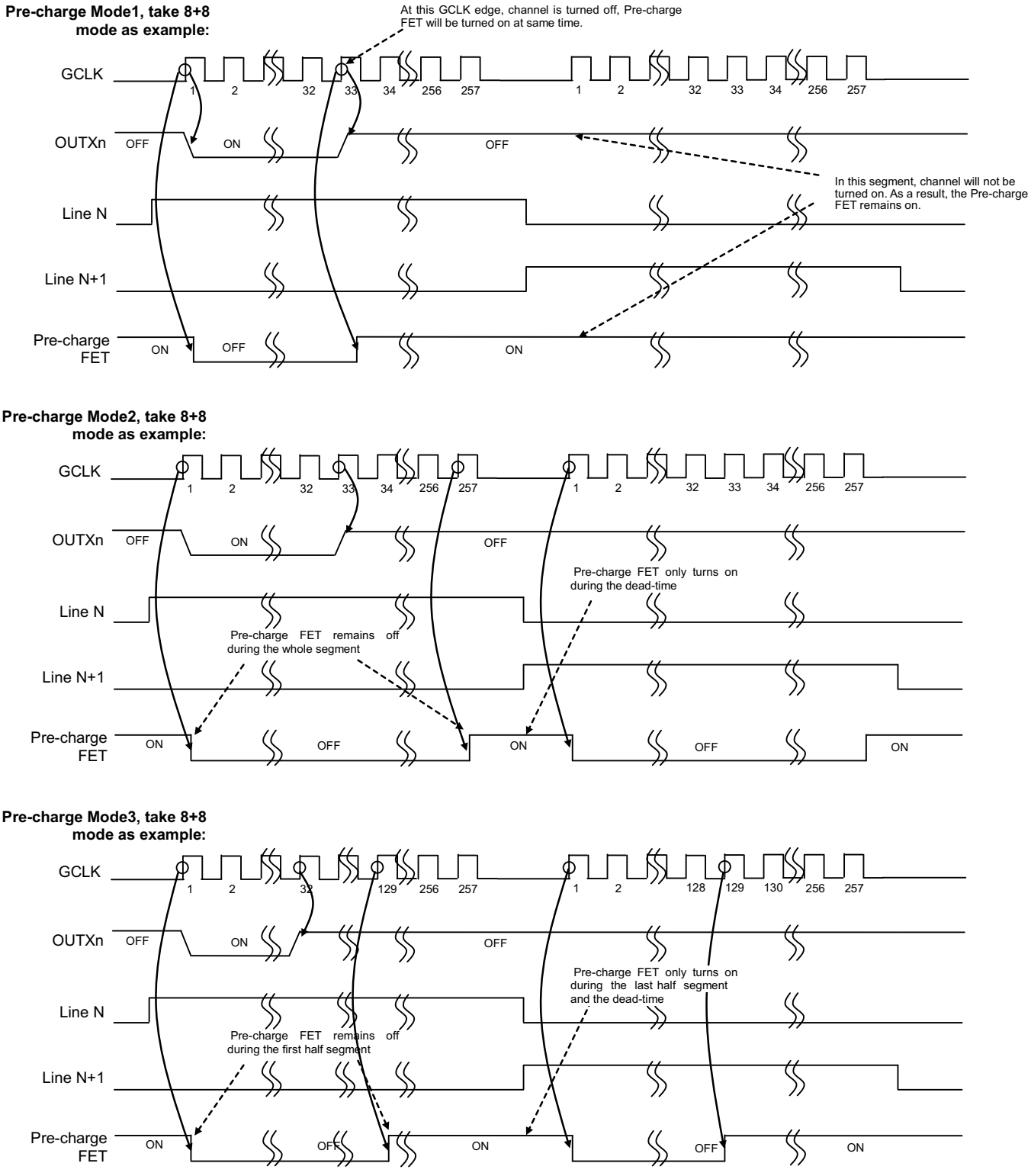


Figure 27. Pre-Charge FET Working Mode

3.14 1st-Line Enhancement

The 1st-line issue is a common phenomenon in multiplexing applications, especially in high density, high refresh rate panels. This issue can be solved with a specific circuit in the TLC59581. We can choose a different setting in the FC2 register according to hardware structure. A typical value is '01'.

Table 12. 1st-Line Enhancement Summary

1st-Line (FC2)		1st-Line Enhancement Effect
Bit 16	Bit 15	
0	0	No
0	1	Weak (Typ)
1	0	Medium
1	1	Strong

3.15 HG-LG Interference Enhancement

When high grayscale and low grayscale patterns are displayed at the same time, the low grayscale part is affected by the high grayscale part. HG-LG interference is solved by choosing different settings of Interference-R, Interference-G, and Interference-B in the FC2 register of TLC59581.

Table 13. Interference Compensation Summary

Interference-R (FC2)		Interference Compensation Effect
Bit 41	Bit 40	
0	0	Normal
0	1	Weak (Typ)
1	0	Medium
1	1	Strong
Interference-G (FC2)		**Interference Compensation Effect**
Bit 37	**Bit 36**	
0	0	Normal
0	1	Weak (Typ)
1	0	Medium
1	1	Strong
Interference-B (FC2)		**Interference Compensation Effect**
Bit 33	**Bit 32**	
0	0	Normal
0	1	Weak (Typ)
1	0	Medium
1	1	Strong

3.16 Low Gray-Scale Enhancement

Low grayscale uniformity is a common issue in multiplexing applications, especially under low current conditions. This issue is solved by choosing different setting of LGSE1-R, LGSE1-G, LGSE1-B in the FC2 register. Adjusting these control bits also helps improve the white balance at low grayscale condition.

Table 14. Low Grayscale Enhancement Setting

LGSE1-R (Bit 31–28)	LGSE1-G (Bit 27–24)	LGSE1-B (Bit 23–20)	Compensation Effect
0000b			0
0001b			1
0010b			2
…			…
1011b			11
1100b			12
1101b			13
1110b			14
1111b			15

Different multiplexing ratios require a different setting. The guidelines follow:

1. The higher the multiplexing ratio is, the higher enhancement is needed.
2. The enhancement of G/B should be higher than that of Red.

For example, one suggested setting for a 1/32 multiplexing panel is: LGSE1-R = 2d, LGSE1-G = LGSE1-B = 9d

3.17 LOD Caterpillar Cancelling

The caterpillar effect is a phenomenon caused by broken LEDs. The TLC59581 has an internal circuit to remove the caterpillar issue in multiplexed LED modules. One cause of this phenomenon is the electric charge on the parasitic capacitor of line goes through the LED when the OUT is pulled down to GND due to the LED open of another line. This makes all the LED multiplexing with the open LED turn on during the special time.

To prevent the caterpillar issue, the TLC59581 has integrated internal circuits for LED open detection. When LED open is detected, the output channel is turned off for this specific line and then the caterpillar effect is eliminated. The LOD caterpillar cancelling function is enabled by choosing different settings of bit 4 in the FC1 register of the TLC59581. Figure 28 illustrate is a detailed explanation of the caterpillar effect.

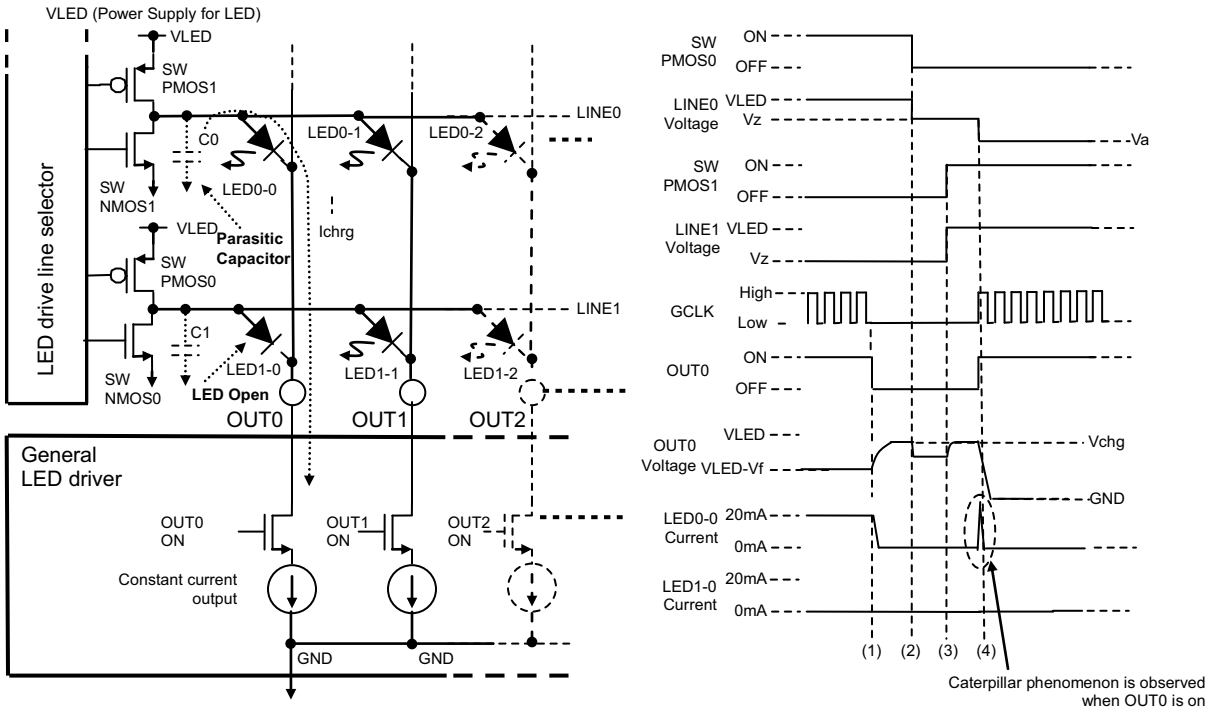


Figure 28. LED Caterpillar Phenomenon Mechanism

3.18 Protection

3.18.1 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs of the IC when the junction temperature (T_J) exceeds 170°C (typ). The TSD function resumes normal work once Tj is lower than 160°C (typ).

3.18.2 IREF Resistor Short Protection (ISP)

The Iref resistor short protection (ISP) function prevents unwanted large current from flowing though the constant-current output when the Iref resistor is shorted accidently. TLC59581 turns off all output channels when the Iref pin voltage goes lower than 0.125 V (typ). When the Iref pin voltage goes higher than 0.35 V (typ), the TLC59581 resumes normal work again.

3.19 System Structure Guidelines

Follow these system structure guidelines:

1. Use less than 60 tri-color LED lamps in one MOSFET line.
2. If not all 48 output channels are used, the separate distribution of empty channels is suggested. For example, if 6 of 48 channels in one IC are empty, empty channel RGB 0 and RGB 15. If 12 of 48 channels in one IC are empty, empty channel RGB 0, 1, 14 and 15.
3. If the empty channels are more than 6 channels, do not place all empty channels in one IC. Distribute the empty channels into different ICs.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265