Picking ESD Diodes for Ultra High-Speed Data Lines

Will Zhou, Jeff Skarzynski

ABSTRACT

This application report addresses three key criteria for selecting an ESD device for protecting high-speed signals. As the industry continues to trend towards smaller chipset features sizes to address higher speed data rates, tolerance of transient voltages has continued to shrink as well. Picking the right ESD device the first time is critical to preventing costly board re-spins during EMC testing. By using the three techniques discussed in this paper, device selection can be greatly simplified and streamlined.

Contents

List of Figures

1 Introduction

When designing a system to support high speed interfaces such as USB 3.1 Gen 2, HDMI 2.0, DisplayPort 1.3, or Thunderbolt, a designer must take into account the entire system in order to meet all end customer requirements. When selecting a TVS diode device, two important criteria come into account: does this device's added capacitance still allow my signals to pass cleanly, and does this device provide the necessary protection from transient events such as ESD? This paper discusses three techniques that can be applied to satisfy the two main TVS diode requirements. Those techniques are:

- TLP analysis – to understand the system breaking point, and the right device to protect it
- Eye diagram analysis – to show what effect a TVS diode has on the system eye diagram
- Layout considerations – best practices that can improve ESD performance and signal integrity

2 TLP Analysis

The TLP (Transmission Line Pulse) test is an efficient way to characterize a protection structure's performance during ESD events. Since TLP has a similar transient duration as IEC 61000-4-2 ESD events and regular waveform shapes, it is common to use this test for assessing how well an ESD device clamps during the IEC strikes. The lower voltage a TLP curve shows for a certain current level, the better it clamps for ESD, which provides more protection for the sensitive ICs behind it.

The TLP technique is realized by charging a long, floating cable and discharging it into the DUT (Device Under Test) at successively increasing levels. The discharging pulses occur within a short duration of 100 ns. Gradually increasing currents and the according voltages are averaged over a time range during the pulse (usually 70%-90% of the pulse duration) and each pulse get recorded. Each current and voltage pair then defines a point on the TLP I-V curve as shown in Figure 1.

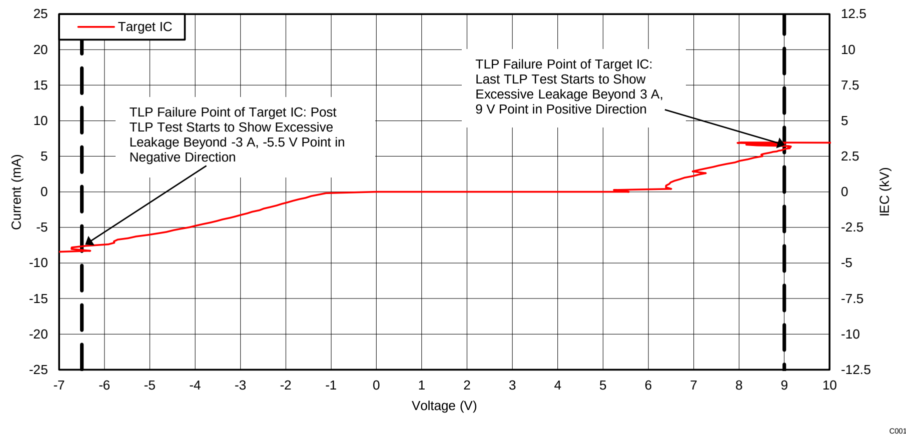

Figure 1. TLP Measurement Example

The TLP curve resembles the DC I-V curve but it characterizes the DUT's transient clamping behavior. Since the test is only carried out over a very short period, the current can run at much higher levels than a DC sweep. Important information like snapback behavior and dynamic resistance can be extracted from the TLP curve.

TLP can be destructive at high levels. There is usually an apparent shift on the TLP curve when the DUT fails. A more reliable criterion to identify failure is a DC I-V sweep after each TLP pulse. The failure level is defined at the point where it starts to show excessive leakage after the pulse. The failure point from TLP is indicative of that from an ESD event.

A general guideline for correlating TLP current with IEC voltage level is as follows:

- IEC 1-kV level = 2 A, 100 ns TLP pulse
- IEC 2-kV level = 4 A, 100 ns TLP pulse
- IEC 4-kV level = 8 A, 100 ns TLP pulse
- Etc...

TLP is an effective tool for evaluating the transient robustness of a system that includes both protection devices and the protected ICs. By using the TLP test, one can determine the protection device performance needed for the protected IC. Figure 2 shows the TLP curve of an IC that needs to be protected. Without any protection, it fails at ±3 A, which translates to only 1.5-kV IEC 61000-4-2 ESD.

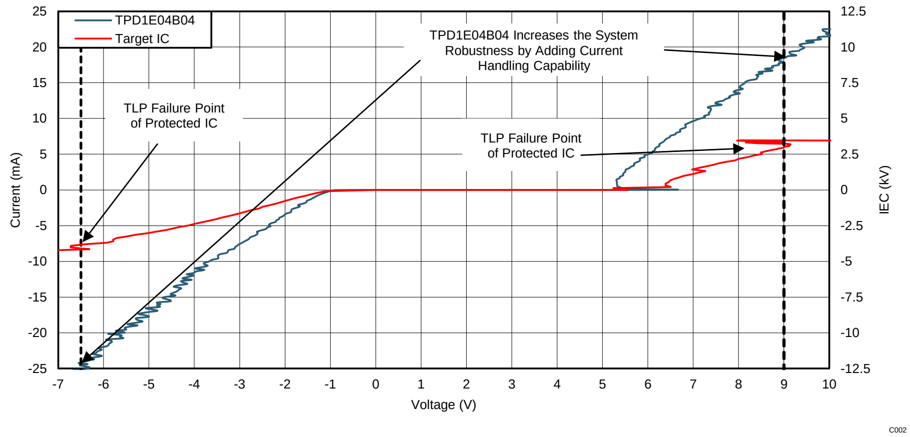

Figure 2. Example IC TLP Results

If the goal is to pass +8-kV IEC 61000-4-2 contact discharge, the protection device and the TVS should withstand at least 16 A of current and keep the clamping voltage below the failure point of the protected IC.

TI's TPD1E04U04 is a superior ESD protection device with low capacitance and dynamic resistance which enables the part to operate at a high-speed data rate and protects downstream ICs with an extremely low clamping voltage. In this example, at 9 V and –5.5 V, TPD1E04U04 adds ±18 A current handling capability during TLP tests, which are equivalent to ESD. This adds ±9-kV IEC 61000-4-2 capability, making the whole system IEC 61000-4-2 ESD compliant up to ±10.5 kV. Figure 3 shows the example IC TLP curve with TPD1E04U04's TLP results overlaid on top. The corresponding IEC 61000-4-2 passing level is shown on the right axis.

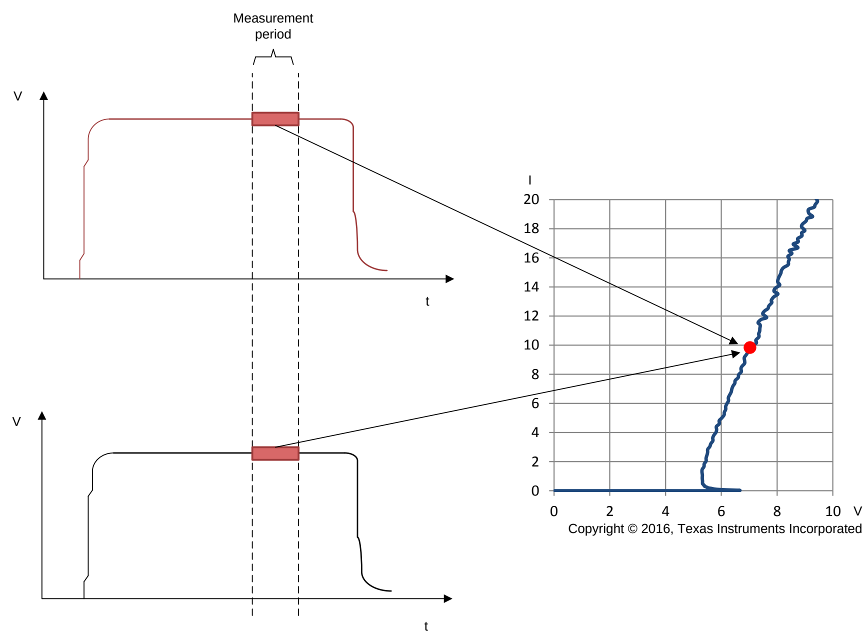

Figure 3. Example IC TLP Results with TPD1E04U04 Superimposed

3 Eye Diagram Analysis

For most high speed differential signals the eye diagram test is the final authority on signal integrity. By testing the eye diagram, many different measurements can be captured which allows for quick understanding of the problem in a system. A TVS diode generally affects eye diagrams by slowing the rise and fall times due to the inherent capacitive loading of the TVS. However, choosing the correct TVS diode for the application should only degrade the eye diagram minimally. The examples in Figure 4 and Figure 5 show USB 3.1 Gen 2 (10-Gbps) eye diagram with and without our TPD1E01B04.

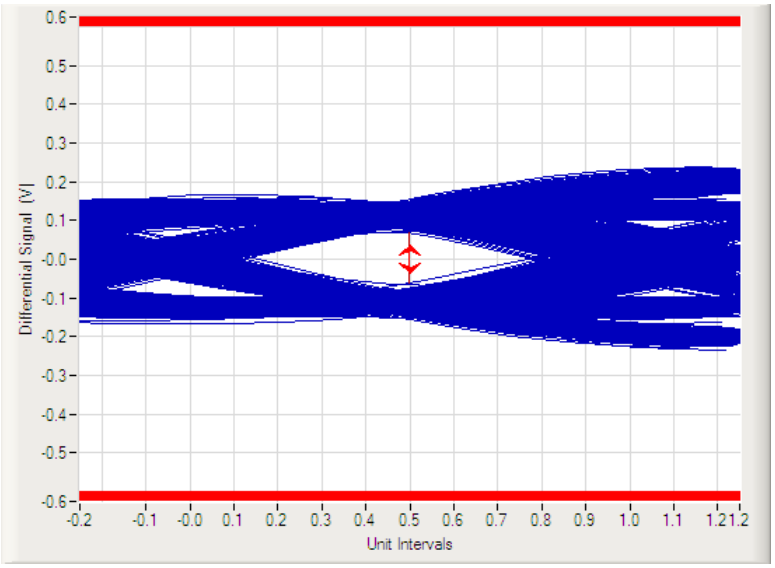

Figure 4. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

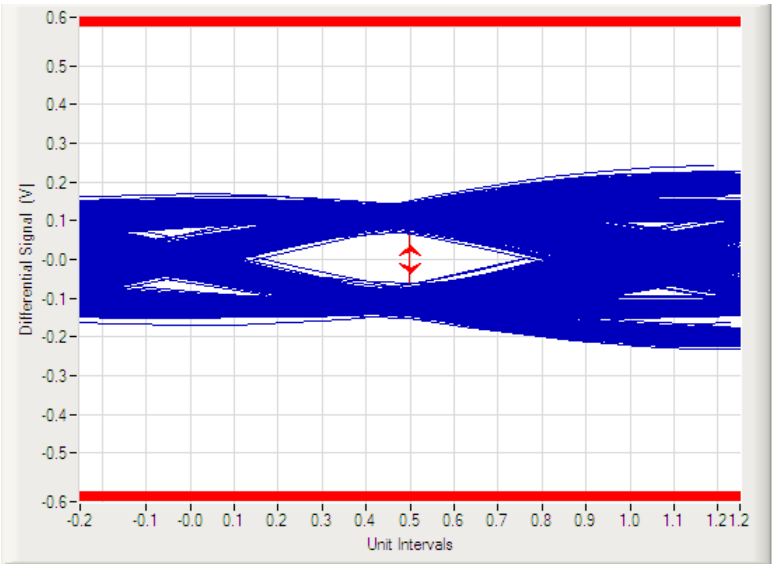

Figure 5. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04)

As it is seen in the USB 3.1 Gen 2 10 Gbps Compliance Test, the above tests show almost no difference in eye diagram performance. This is due to the extremely low capacitive loading (0.2-pF maximum). For more details on eye diagram performance and the impact of TVS diodes on signal integrity, see the application report *Capacitance Requirements for High Speed Signals*, SLVA793.

4 Layout Considerations

Board layout is an important factor to get the best system performance in protection and other aspects like signal integrity. By following these ESD layout guidelines it can be ensured that the protection device gets optimum performance in the system.

- General ESD layout best practices:
  - In order to discharge the ESD before it couples onto anything close to it, place the protection devices as near to the connector as design rules allow
  - Place the Protected IC much further from the protection device than the protection device is to the connector
  - Do not use stubs between the ESD source and protection device, route directly from the ESD source to protection
  - In order to conduct most current into the ESD device and keep the clamping voltage low, minimize any inductance between the ESD Source and the path to ground through the TVS
- Use a grounding scheme that has very low impedance:
  - Connect the protection device Ground Pin directly to a same layer ground plane that has nearby VIAs stitching to an adjacent internal ground plane
  - Use multiple ground planes when possible
  - Use VIAs of large diameter with a large drill, which lowers impedance
- Limit the effects of EMI on unprotected circuits:
  - Do not route unprotected circuits in the area between the ESD Source and the TVS to minimize EMI coupling onto unprotected traces
  - Route with straight traces between the ESD Source and the protection device if possible
  - Avoid using sharp corners in routing since electric fields tend to build up on corners, increasing EMI coupling

Also, the number of VIAs should be kept to minimum for high speed data lines. Take USB Type-C data lines as an example (Figure 6), there are four SuperSpeed TX-RX data lines on each end of the connector. This is split into four on each side of a two-layer board. A four-channel ESD device is a popular choice for many applications, but for Type-C connectors that have 20-Gbps differential pairs it may not be the best option since VIAs are needed to route all four data lines to the same layer. This issue can be mitigated by using single or dual channel ESD devices.

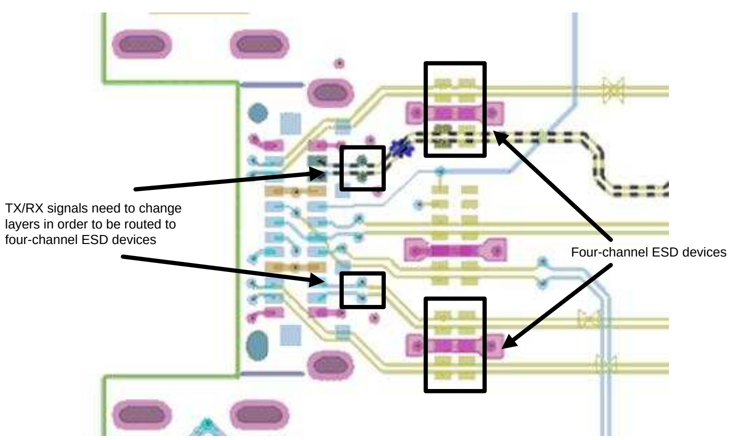

Figure 6. Example Layout with 4-Channel Routing Inefficiencies

5 Conclusion

Today's high-speed signals can be challenging to design. This application note provides three helpful techniques to simplify EMC design and aid in success. TI's TVS diode portfolio provides a large variety of choices for high-speed data line protection to meet customer requirements.

6 References

- TI's ESD portfolio (ti.com/esd)
- Reading and Understanding an ESD Protection Datasheet (SLLA305)
- ESD Protection Layout Guide (SLVA680)
- Capacitance Requirements for High Speed Signals (SLVA793)
- TPD1E04U04
- TPD1E01B04

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265