Application Report
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Power and Dimming LED With TPS54200 and TPS54201

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ABSTRACT

The TPS54200 and TPS54201 (TPS5420X) devices are 28-V wide input range, 1.5-A maximum output current, synchronous buck LED drivers supporting deep dimming ratio with high dimming accuracy. The TPS5420X supports both analog and PWM dimming mode. Especially, in analog dimming mode, a 1% dimming ratio is easily attained by inputting a PWM signal with 1% duty cycle. This is a welcomed feature in surveillance applications. In some other applications where LED color shift is not allowed, PWM dimming mode may be used. To use this part flexibly, the dimming mechanism implemented inside the TPS5420X is explained in detail, and various dimming methods in applications are discussed as well in this report.

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Trademarks

1 Typical Application

The TPS5420X family is a 4.5- to 28-V input voltage, 1.5-A output current, synchronous buck LED driver. With SOT23-6 small package, the device offers a compact, efficient, and cost-effective solution in many kinds of LED lighting markets, such as video surveillance cameras, industrial and commercial illumination, architecture lighting, and so forth.

The TPS5420X supports both PWM dimming mode and analog dimming mode. Especially, in analog dimming mode, the TPS5420X can achieve extreme wide dimming range from 100% to 0.1%, provide a super-smooth transition from LED on to LED off status. Since the LED current amplitude is directly controlled by PWM duty, the device achieves a very accurate LED current control even under low dimming ratio. This is welcomed in surveillance camera applications.

Complete protection features in the TPS5420X guarantee a safe operation of the LED circuit. Besides the cycle-by-cycle current limit implemented for the built-in high-side and low-side power FET, LED open and short, sense resistor open and short protection are also implemented. To maximize the system flexibility, TPS54200 and TPS54201 adopts different protection modes. The TPS54200 uses shutdown-and-latch protection mode, while the TPS54201 adopts hiccup mode protection.

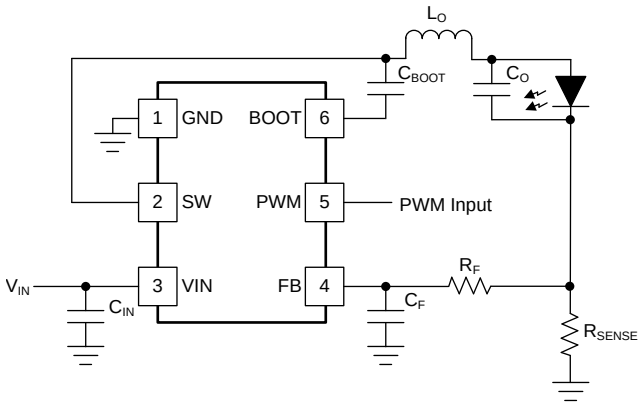

Figure 1. Typical LED Driver Circuit With TPS5420X

External component selection includes the determination of L_O, C_O, C_{IN}, R_{SENSE}, R_F and C_F.

The allowed voltage ripple at the input rail will determine the input capacitance needed. The output capacitance C_O will affect the ripple current through the LED string. The selection of output inductance, L_O, is a tradeoff between LED ripple current, efficiency, cost, and solution size. Current sense resistor R_{SENSE} is sized for a target LED current. The RC filter at the FB pin, R_F and C_F, generates a pole to cancel the internal zero for loop stability consideration. Detail design procedures for these components is found in the TPS5420X data sheet (SLUSCO8).

2 TPS5420X Dimming Mechanism

The TPS5420X has two dimming modes, its behavior is different in these two dimming modes. The magnitude of the PWM signal is used to determine which dimming mode the device will enter at power on. Once the dimming mode is detected and locked, it will not change unless V_{IN} or PWM is recycled.

2.1 Dimming Mode Detection

2.1.1 Normal Mode Detection Process

The internal dimming mode detection circuit is shown in Figure 2.

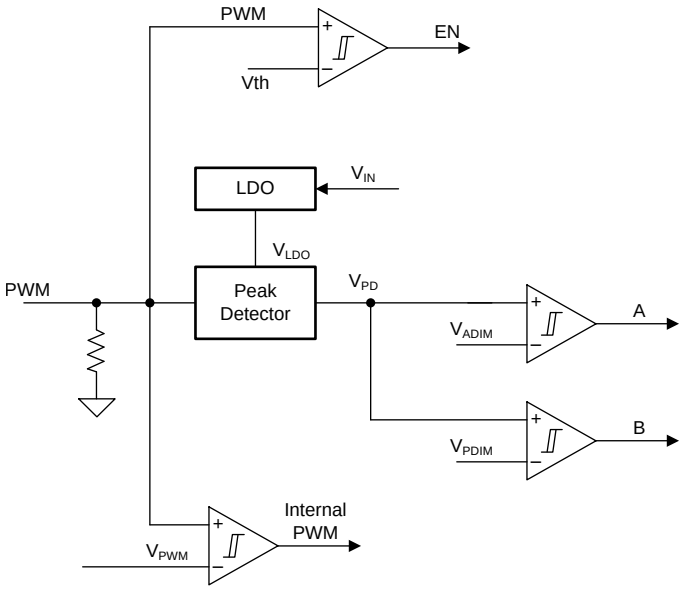

Figure 2. Dimming Mode Detection Circuit

The output of the peak detector at the PWM pin, V_{PD}, will hold the magnitude of the PWM signal as long as it is less than the upper limit of peak detector output voltage which is around V_{LDO} – 1 V (worst case); otherwise, V_{PD} will be clamped at V_{LDO} – 1 V, see Figure 7 for the relationship between V_{IN} and V_{LDO}. V_{LDO} is the power supply of the peak detector, it limits the maximum output voltage of the peak detector at V_{LDO} – 1 V. Here, 1 V is the minimum voltage drop between V_{LDO} and V_{PD}. See Figure 3 for the block diagram of the peak detector.

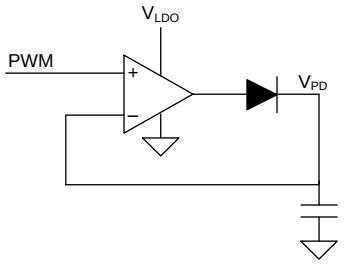

Figure 3. Peak Detector Block Diagram

Once the device is enabled, and after a 300-µs delay, the output of the peak detector will be compared with two voltage thresholds V_{ADIM} and V_{PDIM}, which is typically 1 V and 2.07 V, respectively. See the TPS5420X data sheet (SLUSCO8) for the variation of these two parameters. If the output of the peak detector is higher than 2.07 V, analog dimming mode will be chosen and locked. If it is between 1 V and 2.07 V, PWM dimming mode will be chosen and locked. If it is less than 1 V, the device will wait another 300-µs and compare again, and this process will repeat until at least one mode is chosen and locked. Refer to Table 1 for the dimming mode detection condition summary.

Table 1. Mode Detection Condition

A	B	Mode
H	H	Enter Analog dimming mode
L	H	Enter PWM dimming mode
L	L	Keep detecting until one dimming mode is locked

To detect and lock dimming mode correctly, proper timing sequence at power on is required. TI suggests applying V_{IN} at first, followed by the PWM signal, see Figure 4 for a normal power on timing sequence.

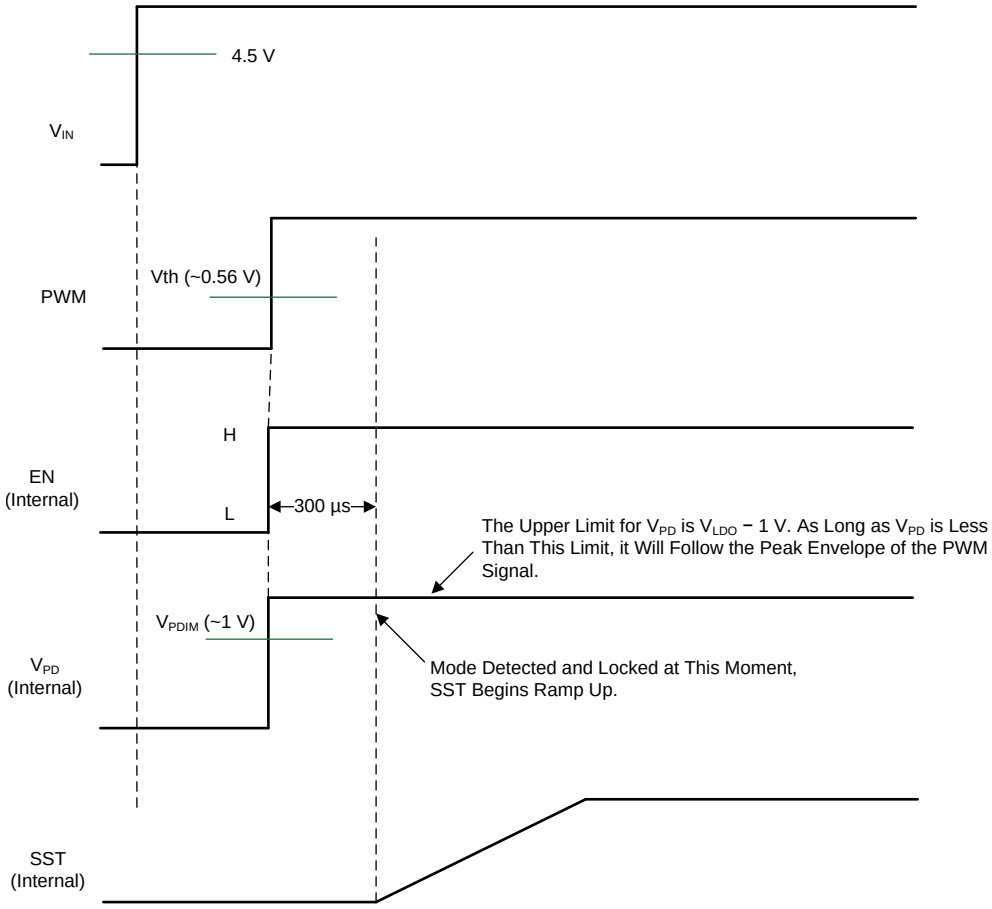

Figure 4. Normal Power On Timing Sequence

2.1.2 Potential Wrong Mode Detection

There are two extreme conditions in which the TPS5420X may fail to enter analog dimming mode correctly. One of these two conditions is that PWM rising speed very slow, for example, less than 5 V / ms. Another condition is that V_{IN} is applied after the PWM signal, and V_{IN} has a very slow rising slew rate. Be careful not to run into these two conditions if analog dimming mode is needed. Refer to Figure 5 and Figure 6 for the timing diagram of these two cases.

In Figure 5, V_{IN} is applied at first, then PWM is applied. PWM has a 3.3-V amplitude, the device should enter analog dimming mode as expected. However, since PWM rising edge is very slow, it is possible to detect dimming mode before V_{PD} reaches the V_{ADIM} threshold (2 V), and thus may cause the device to enter PWM dimming mode falsely.

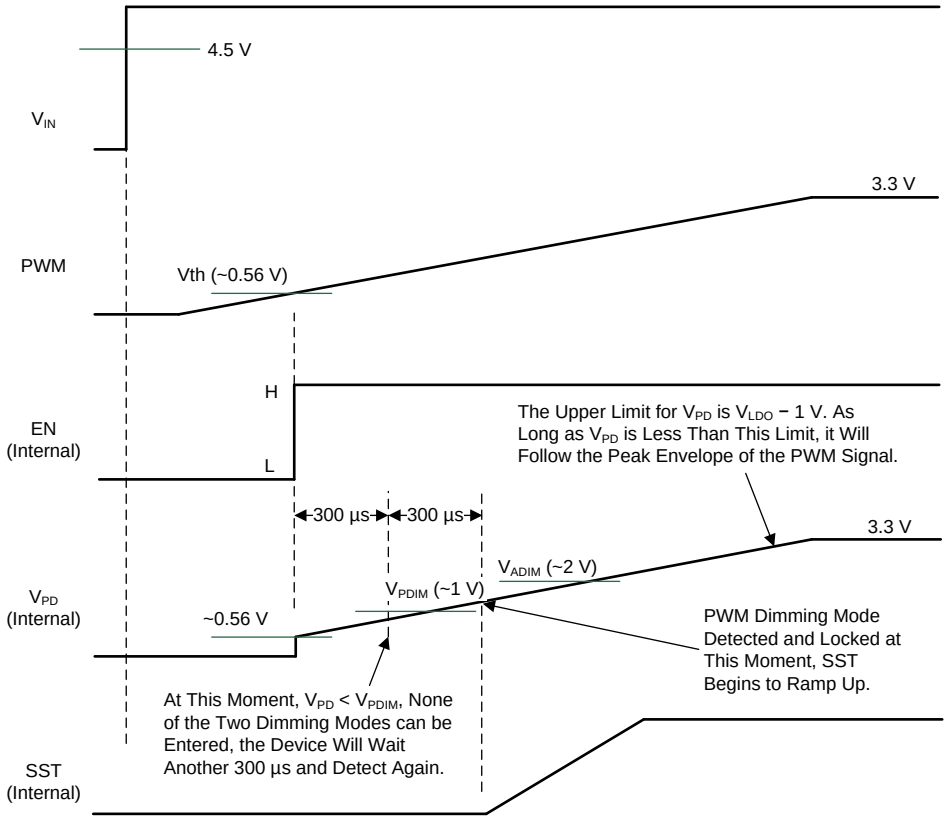

Figure 5. Very Slow PWM Rising Speed May Prevent Device From Entering Analog Dimming Mode

In Figure 6, the PWM signal is applied at first, then V_{IN} is ramped up slowly. Normally the device will be activated when V_{IN} approaches 4.2 V, while in the worst case, the device may be enabled when V_{IN} approaches 3.9 V. Once the device is enabled, the internal LDO output V_{LDO} is approximately 2.5 V due to the minimum voltage drop of LDO. After that, V_{LDO} will ramp up toward 6.5-V steady state all the way as V_{IN} ramps up. Figure 7 shows the relationship between V_{IN} and V_{LDO}.

In this example, the external PWM signal is 5-V amplitude. However, due to the minimum voltage drop between V_{LDO} and V_{PD}, V_{PD} will be only approximately 1.5 V at the moment the device is enabled. After that, V_{PD} will ramp up slowly as V_{IN} and V_{LDO} ramp up. Since V_{IN} ramps up slowly, in turn V_{PD} will also ramp up slowly. It is possible to detect and lock the dimming mode before V_{PD} reaches the V_{ADIM} threshold (2 V), and thus may cause the device to enter PWM dimming mode falsely.

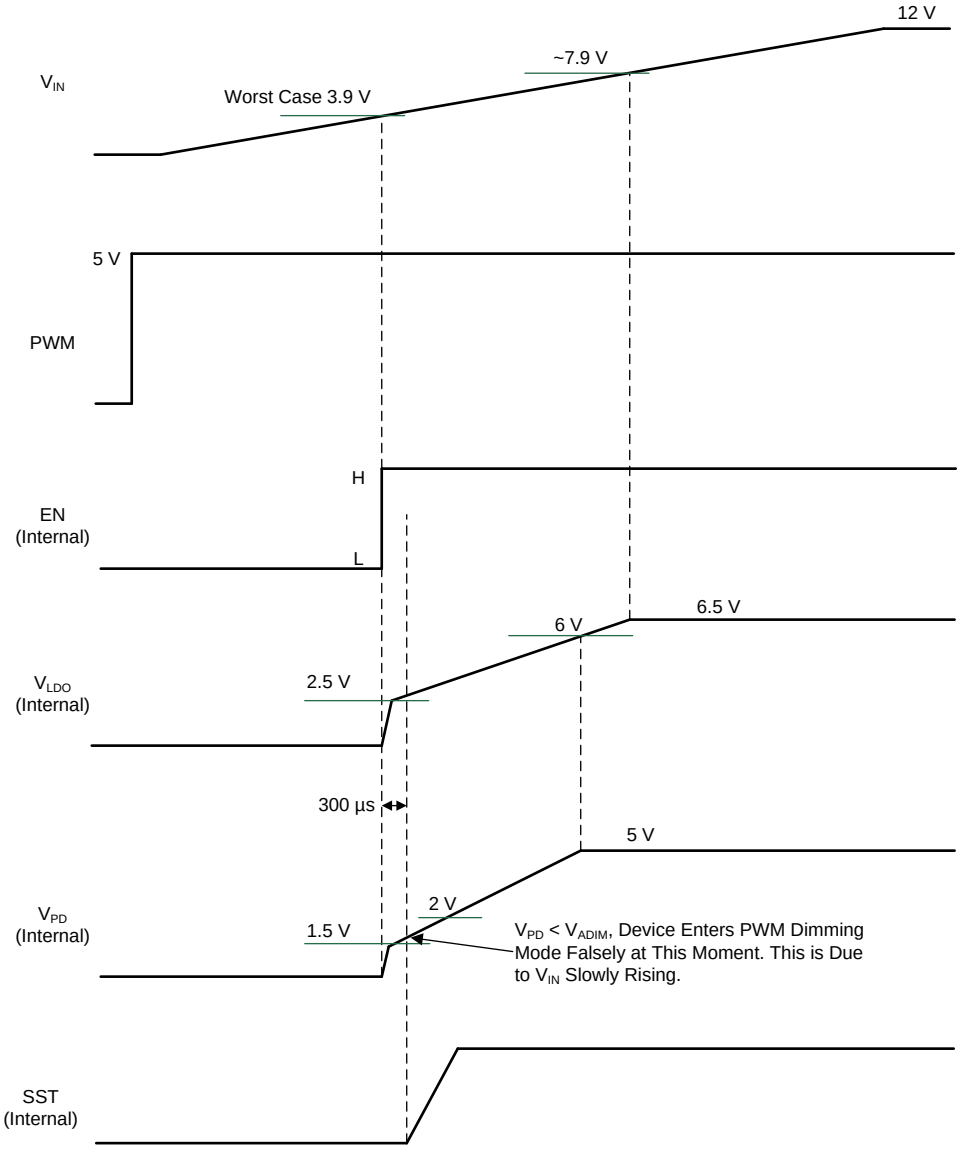

Figure 6. Very Slow V_{IN} Rising Speed May Prevent Device From Entering Analog Dimming Mode

Figure 7 shows the relationship between V_{IN} and V_{LDO}. When V_{IN} < 7.9 V, V_{LDO} is around 1.4 V lower than V_{IN}. When V_{IN} > 7.9 V, V_{LDO} will be fixed at approximately 6.5 V.

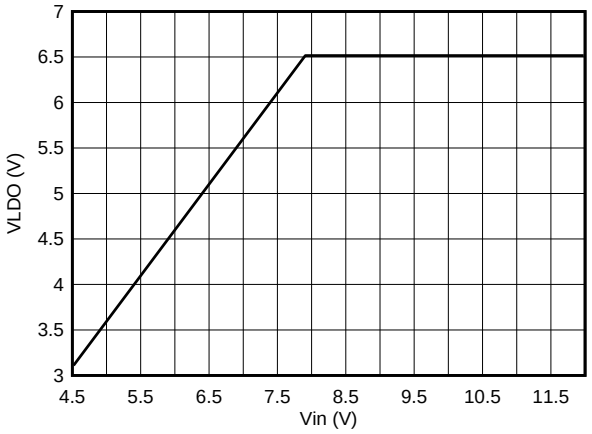

Figure 7. V_{LDO} vs V_{IN}

2.2 Analog Dimming Mode Operation

Once analog dimming mode is entered , the duty cycle of the PWM input signal will be used to generate the internal voltage reference for the FB pin. Figure 8 shows this process. The PWM pin signal is fed to a comparator with 400-mV hysteresis, then an internal PWM signal is generated. To make sure the PWM pin signal is correctly identified, the high level of PWM signal should be higher than 1 V, and the low level should be lower than 0.6 V. Figure 10 shows the relationship between the external PWM and internal PWM signal. The amplitude of the internal PWM signal is fixed at 200 mV. This internal PWM signal will be fed to an RC filter to generate the internal voltage reference, which has an average voltage proportional to the PWM duty cycle as shown in Figure 9. LED current is sensed and compared with this internal voltage reference. The LED current is continuous in this mode, and the current magnitude can be adjusted by changing the PWM duty cycle.

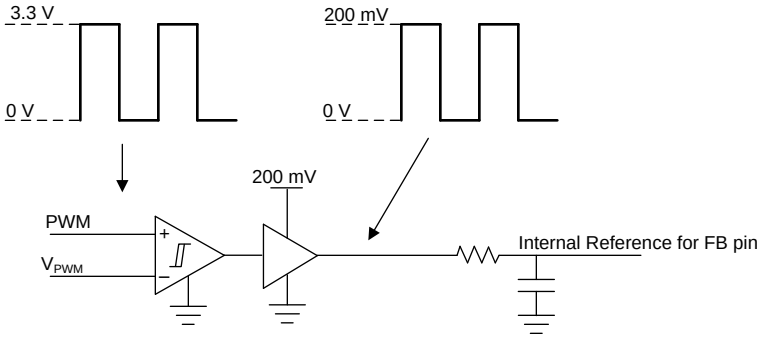

Figure 8. Internal Voltage Reference Generation Circuit

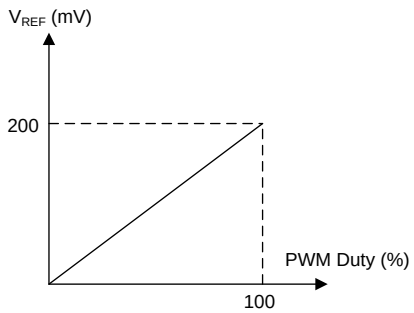

Figure 9. Internal Voltage Reference V_{REF} vs PWM Duty Cycle

Since the internal voltage reference is generated by the RC filter, a PWM frequency that is too low may cause a bigger ripple at voltage reference. To minimize this ripple, TI recommends making the PWM signal frequency 10 kHz, or higher. 50 kHz is suggested as a typical value.

Notice that the PWM signal amplitude is not required to be larger than 2 V once the analog dimming mode is locked. In other words, the PWM signal amplitude can be 1.5 V, for example, after the dimming mode is locked.

2.3 PWM Dimming Mode Operation

In PWM dimming mode, the internal voltage reference for the FB pin will be fixed at 100 mV, LED current will be on or off, corresponding to the internal PWM signal duty cycle, see Figure 10. Due to the limited control loop response, to get a relatively linear dimming performance, the suggested PWM signal frequency should be less than 1 kHz.

Notice that the PWM signal amplitude is not required to be lower than 2 V once the PWM dimming mode is locked. In other words, the PWM signal amplitude can be 3.3 V, for example, after the dimming mode is locked.

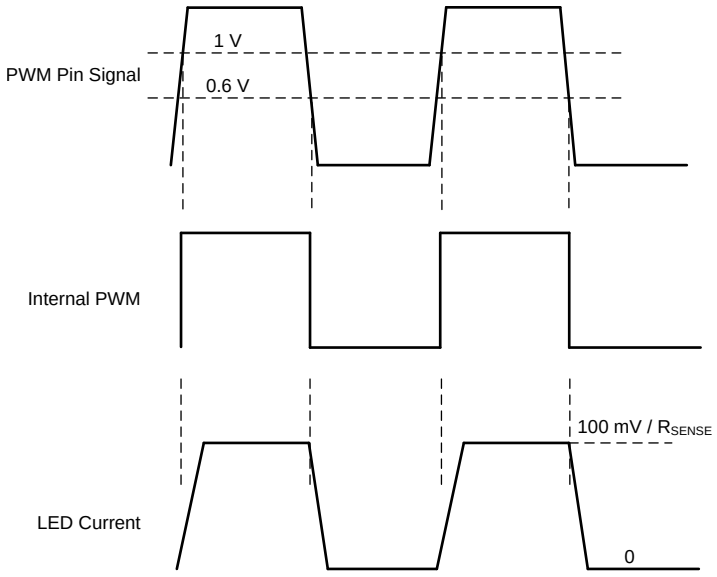

Figure 10. PWM Dimming Operation

3 Dimming Method in Application

3.1 PWM Dimming Mode Application

3.1.1 PWM Signal With Amplitude Higher Than 2 V

As described in *Dimming Mode Detection*, to enter the PWM dimming mode, the PWM signal amplitude should be between 1 V and 2 V. Typically 1.5 V is chosen for the best variation tolerance. If the PWM input signal has an amplitude higher than 2 V, a resistor divider must be added to scale down the PWM amplitude at the PWM pin. Figure 11 shows a typical application circuit for this case.

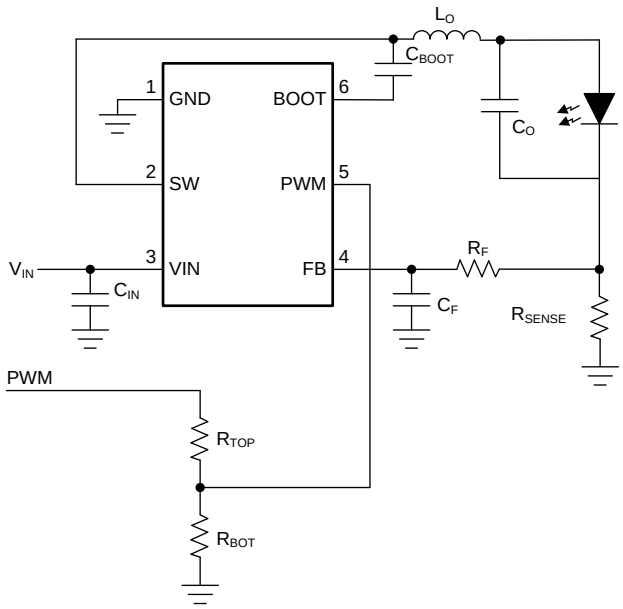

Figure 11. PDIM Operation With Higher Than 2-V Amplitude PWM Signal

TI suggests using less than 100 kΩ for the bottom resistor of the divider, R_{BOT}. Once the value of R_{BOT}, is chosen, Equation 1 can be used to estimate the value of R_{TOP}.

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{PWM}}{1.5} - 1 \right) \quad (1)$$

where

- V_{PWM} is the amplitude of PWM input signal

Table 2 shows the suggested resistor divider for some commonly used logic level PWM inputs.

Table 2. Suggested Resistor Divider for Some Common Logic Level PWM Inputs

PWM Amplitude	R_{TOP}	R_{BOT}
5 V	24 kΩ	10 kΩ
3.3 V	12 kΩ	10 kΩ
2.5 V	6.8 kΩ	10 kΩ

3.1.2 PWM Signal With Amplitude Lower Than 2 V

When the amplitude of the PWM signal is between 1 V and 2 V, this PWM signal can be fed to the PWM pin directly as Figure 1 shows. The device will work in PDIM mode.

3.2 Analog Dimming Mode Application

3.2.1 Analog Dimming on PWM Pin

To enter analog dimming mode, the PWM signal amplitude should be higher than 2.07 V (typical). Most of the commonly used logic levels meet this requirement, such as 5 V, 3.3 V, and 2.5 V. As long as this requirement is met, the PWM signal can be fed to the PWM pin directly to perform analog dimming. See Figure 1 for the typical application circuit.

To make sure the device enters analog dimming mode correctly, at power on, ensure V_{IN} is applied before the PWM input. Also pay attention to the rising slew rate of the PWM signal, which should be higher than 5 V / ms.

Implementing analog dimming by applying the PWM signal to the PWM pin is the preferred method. This gives the end user an excellent dimming linearity, even under deep dimming conditions which means the dimming duty ratio is lower than 1%.

3.2.2 Analog Dimming on the FB Pin

If analog dimming mode is needed, but the high-frequency PWM signal is not available, keep the PWM pin higher than 1 V and apply a variable DC voltage to the FB pin through a resistor. See Figure 12 for this method.

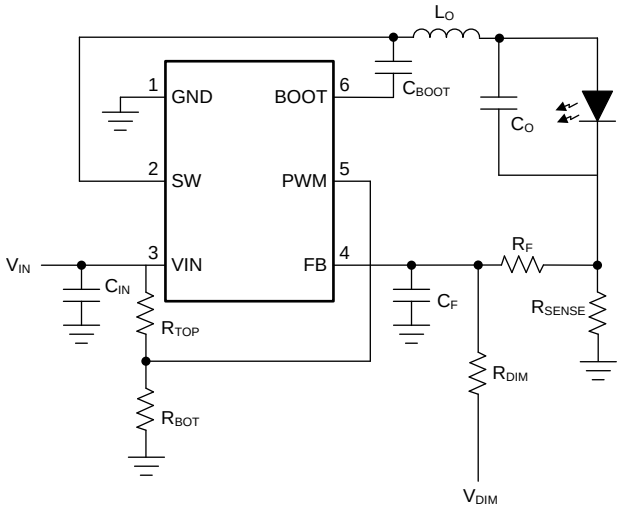

Figure 12. ADIM Operation by Applying DC Bias at the FB Pin

The R_{TOP} and R_{BOT} resistor divider is sized to make the device enter PWM dimming mode. See Section 3.3, *No Dimming Application* for reasons to choose PWM dimming mode, as well as how to choose R_{TOP} and R_{BOT}.

Selecting R_{DIM} and R_{SENSE} is a combined work. Obviously, from the circuit shown in Figure 12, the LED current will be inversely proportional to V_{DIM} voltage. Before starting the design, several parameters must be determined. Table 3 shows the design parameter for this example.

Table 3. Design Parameters for the Example of Analog Dimming at the FB Pin

Parameter	Value
Maximum input dimming voltage, V_{DIM_MAX}	5 V
Minimum input dimming voltage, V_{DIM_MIN}	0 V
Minimum LED current I_{LED_MIN} at V_{DIM_MAX}	0 mA
Maximum LED current I_{LED_MAX} at V_{DIM_MIN}	1500 mA
Resistor of FB filter, R_F	475 Ω

Step 1. When V_{DIM} is maximum, the LED current is 0 mA, which means the voltage across R_{SENSE}, V_{SENSE_MIN}, is 0 V. Use Equation 2 to estimate R_{DIM}.

$$R_{DIM} = \frac{V_{DIM\_MAX} - 0.1}{0.1 - V_{SENSE\_MIN}} \times R_F \quad (2)$$

The calculated R_{DIM} is 23.275 kΩ.

Step 2. Choose the closest standard value for R_{DIM}, here 23.7 kΩ is used. Use Equation 3 and Equation 4 to calculate the minimum and maximum voltage across R_{SENSE}, V_{SENSE_MIN}, and V_{SENSE_MAX}, respectively.

$$V_{SENSE\_MIN} = 0.1 - \frac{\left(V_{DIM\_MAX} - 0.1\right) \times R_F}{R_{DIM}} \quad (3)$$

$$V_{SENSE\_MAX} = 0.1 - \frac{\left(V_{DIM\_MIN} - 0.1\right) \times R_F}{R_{DIM}} \quad (4)$$

The calculated result is V_{SENSE_MIN} = 1.8 mV and V_{SENSE_MAX} = 102 mV.

Step 3. Use Equation 5 to calculate R_{SENSE}.

$$R_{SENSE} = \left(\frac{V_{SENSE\_MAX}}{I_{LED\_MAX}}\right) \quad (5)$$

The calculated R_{SENSE} = 68 mΩ. Here we choose 2-piece 33 mΩ in series.

3.3 No Dimming Application

In applications where dimming is not needed, connect the resistor divider from V_{IN} to the PWM pin as Figure 13 shows.

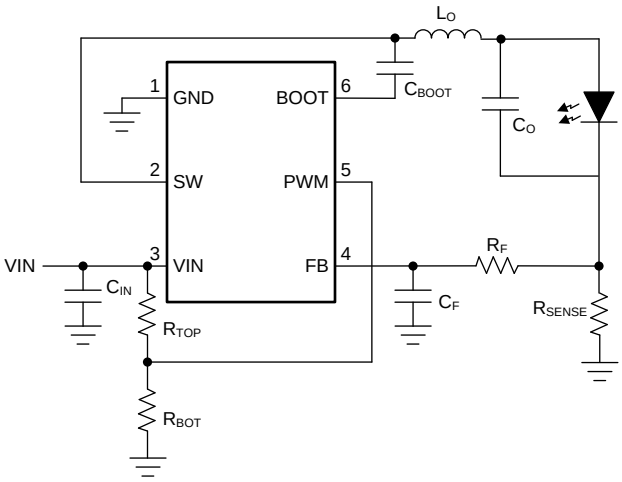

Figure 13. Application Without Dimming

The R_{TOP} and R_{BOT} resistor divider is sized to give a DC voltage between 1 V and 2 V at the PWM pin when V_{IN} reaches its steady-state voltage. The purpose is to make the device enter PWM dimming mode. There are two reasons for choosing PWM dimming mode here. One is for better efficiency (100 mV at the FB pin, instead of 200 mV), another is that entering PWM dimming mode has no requirement about the rising slew rate of V_{IN}, as described in Section 2.1.2, *Potential Wrong Mode Detection*.

10 kΩ is a good starting point for R_{BOT}, then choose R_{TOP} according to Equation 6:

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{IN}}{1.5} - 1\right) \quad (6)$$

Table 4 shows the suggested resistor divider for several commonly used input rails.

Table 4. Suggested Resistor Divider for Some Commonly Used Input Rail

V_{IN} Amplitude	R_{TOP}	R_{BOT}
5 V	24 kΩ	10 kΩ
12 V	68 kΩ	10 kΩ
24 V	150 kΩ	10 kΩ

3.4 Summary

The TPS5420X can support both analog dimming and PWM dimming. Table 5 summarizes these use cases, as well as the advantage of each use case.

Table 5. Dimming Method Summary

Case	LED Current Dimming Mode	Device Dimming Mode	Input Dimming Signal	Ref Circuit	Advantage
1	PWM Dimming	PDIM	PWM, amplitude > 2 V, < 1 kHz	Figure 11	• No color shift effect • Easy for MCU control
2			PWM, amplitude between 1 V and 2 V, < 1 kHz	Figure 1	
3	Analog Dimming (LED Current is Continuous DC Waveform)	ADIM	PWM, amplitude > 2 V, > 10 kHz	Figure 1	• Excellent dimming linearity • Deep dimming (100% to 0.1%) • Easy for MCU control • Excellent uniformity of LED current even under 1% PWM duty • Free from beat frequency interference
4		PDIM	Variable DC voltage	Figure 12	• Easy for DC dimming voltage application • Free from beat frequency interference
5	No dimming	PDIM	No need	Figure 13	• No dimming signal needed, simplest interface for use

Both analog dimming mode and PWM dimming mode have their own limitations in application. For analog dimming mode, the LED is always on, and the brightness is changed by changing the LED current amplitude. Since the LED color temperature has a slight shift under different LED current amplitude, this implies that analog dimming method will cause a color shift problem. For PWM dimming mode, the LED is on and off (flashing) according to the PWM signal. LED brightness is changed by changing the PWM duty cycle. Sometimes, this kind of flashing can be captured by a video system, such as surveillance system, and become visible, this is called beat frequency interference.

A proper dimming mode should be chosen based on the specific system requirements. For the application where color shift is not allowed, that is, an LED-illumination system, then the PWM dimming mode (case 1 and 2) should be chosen. While some applications care more about beat frequency interference, then the analog dimming mode (case 3 and 4) should be used. Especially, for surveillance systems, not only is beat frequency interference important, but they also need a very deep dimming range (100% down to 0.1%), for these situations, case 3 is the best choice. In case 3, the LED current amplitude uniformity can be ensured under low dim ratio in mass production.

4 Test Results

4.1 Analog Dimming Result

4.1.1 Analog Dimming on the PWM Pin

Using Figure 1 as the test circuit, 12-V input voltage, 3-piece IR LED in series as load, R_{SENSE} = 133 mΩ, PWM signal with 3.3-V amplitude is applied to the PWM pin, PWM frequency is 50 kHz. The measurement result of the LED current under different PWM duty is shown in Figure 14. The dimming linearity is very good.

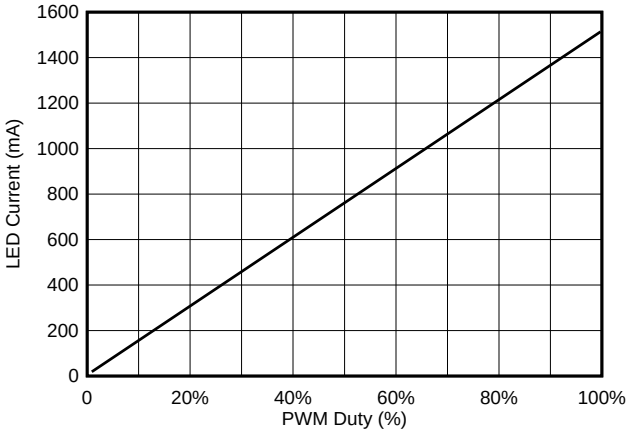

Figure 14. LED Current vs PWM Duty in ADIM Mode

To check the deep dimming performance, the LED current to PWM duty relationship curves are zoomed in the 1% to 5% PWM duty range, see Figure 15. The dimming linearity is very good in low dim ratio range.

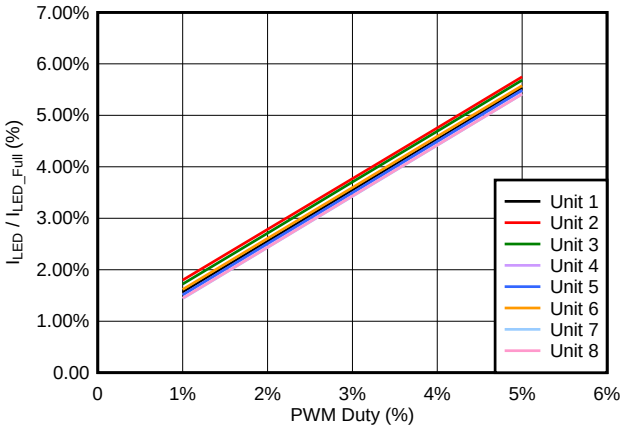

Figure 15. Deep Dimming in ADIM Mode

Figure 15 shows the result of 8 devices, the LED current uniformity is also good under the low dim ratio range.

4.1.2 Analog Dimming on the FB Pin

Figure 16 is the experiment result based on the design in *Analog Dimming on the FB Pin*. 12-V input voltage, 2-piece IR LED in series is used as load, R_{SENSE} = 66 mΩ, 1.5-V DC voltage is applied at the PWM pin. Variable DC voltage V_{DIM} from 0 V to 5 V is applied to the FB pin through a 23.7-kΩ resistor.

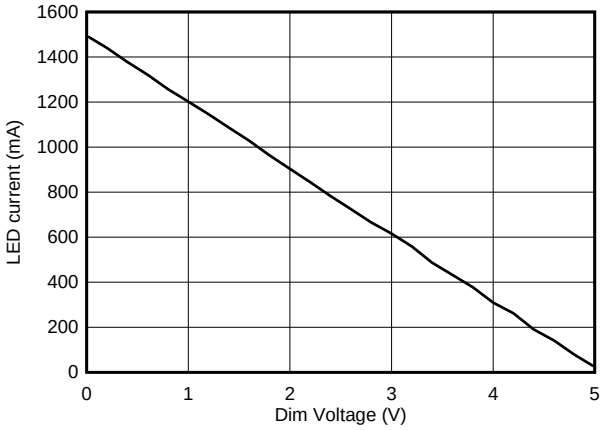

Figure 16. LED Current vs V_{DIM} Voltage

This measurement result matches the design target very well. LED current is inversely proportional with dim voltage. When V_{DIM} is maximum 5 V, the LED current reaches a minimum value of 23 mA which is very close to the design target (0 mA). When V_{DIM} is minimum 0 V, the LED current reaches a maximum value of 1495 mA which is also close to the design target (1500 mA). The small difference between the experiment result and the design target is due to the fact that R_{DIM} can only be a standard resistance value, which is a little different from the calculated value.

4.2 PWM Dimming Waveform

Using Figure 11 as the test circuit: 24-V input voltage, 4-piece white LED, in series, is used as load. L_O and C_O is 10 µH and 10 µF, respectively. R_{SENSE} is 100 mΩ to get a 1-A LED current when PWM duty is 100%. R_F is 200 Ω, C_F is 82 nF.

The amplitude of input PWM signal is 5 V. R_{TOP} and R_{BOT} is 24 kΩ and 10 kΩ, respectively, thus the 5-V input PWM is scaled down to 1.5 V and fed to the PWM pin.

Figure 17, Figure 18, and Figure 19 show the PWM dimming waveform at 2%, 50%, and 99% duty cycle, respectively. CH1 is the input PWM signal, CH3 is the scaled signal fed at PWM pin, and CH4 is the LED current waveform.

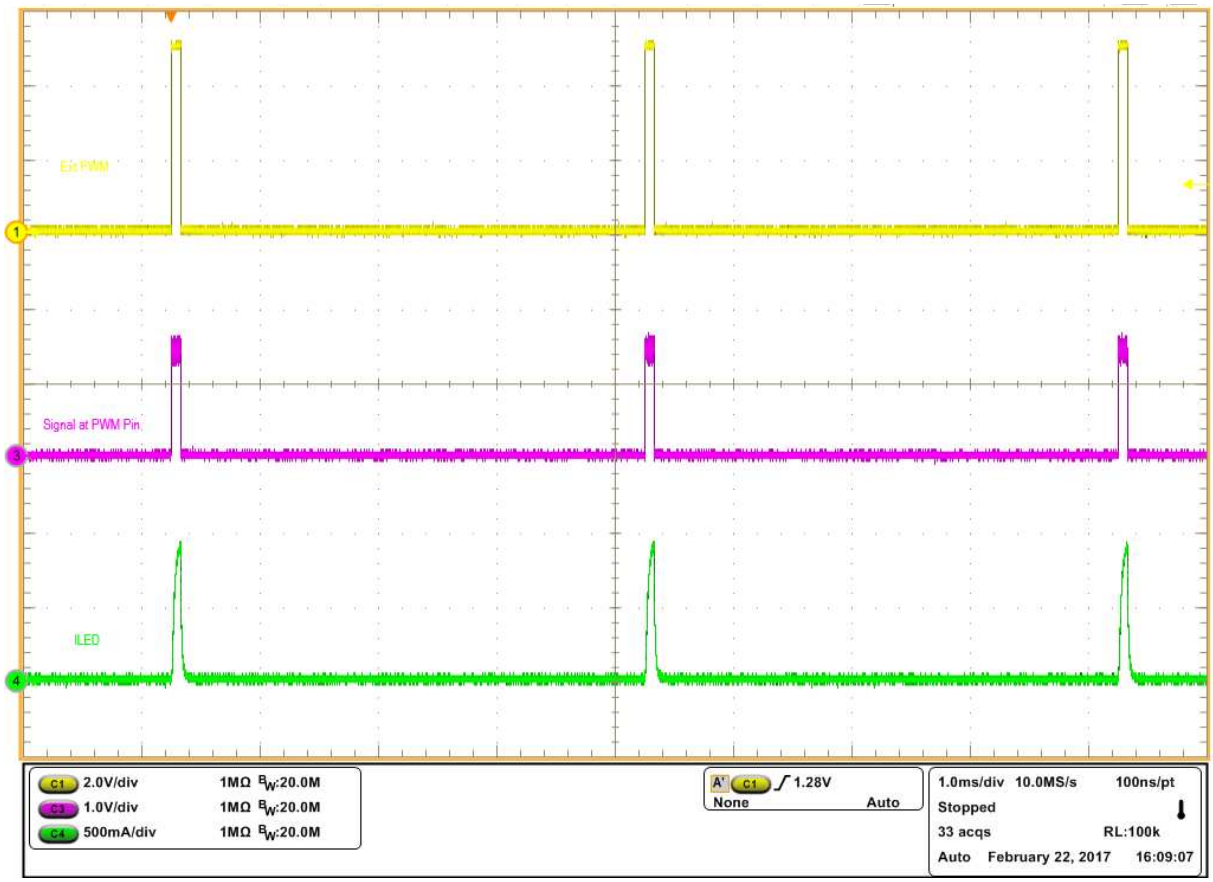

Figure 17. PWM Dimming With 2% Duty, 250 kHz

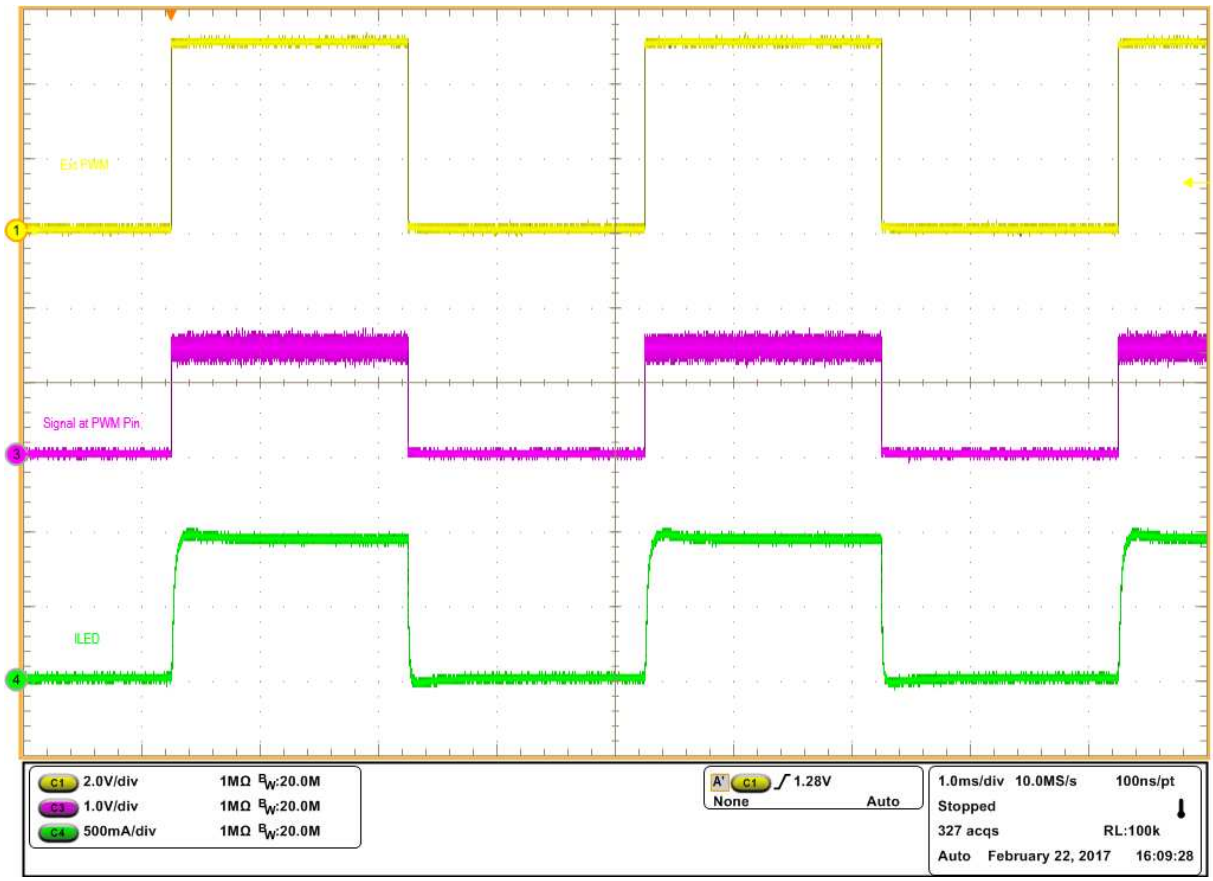

Figure 18. PWM Dimming With 50% Duty, 250 kHz

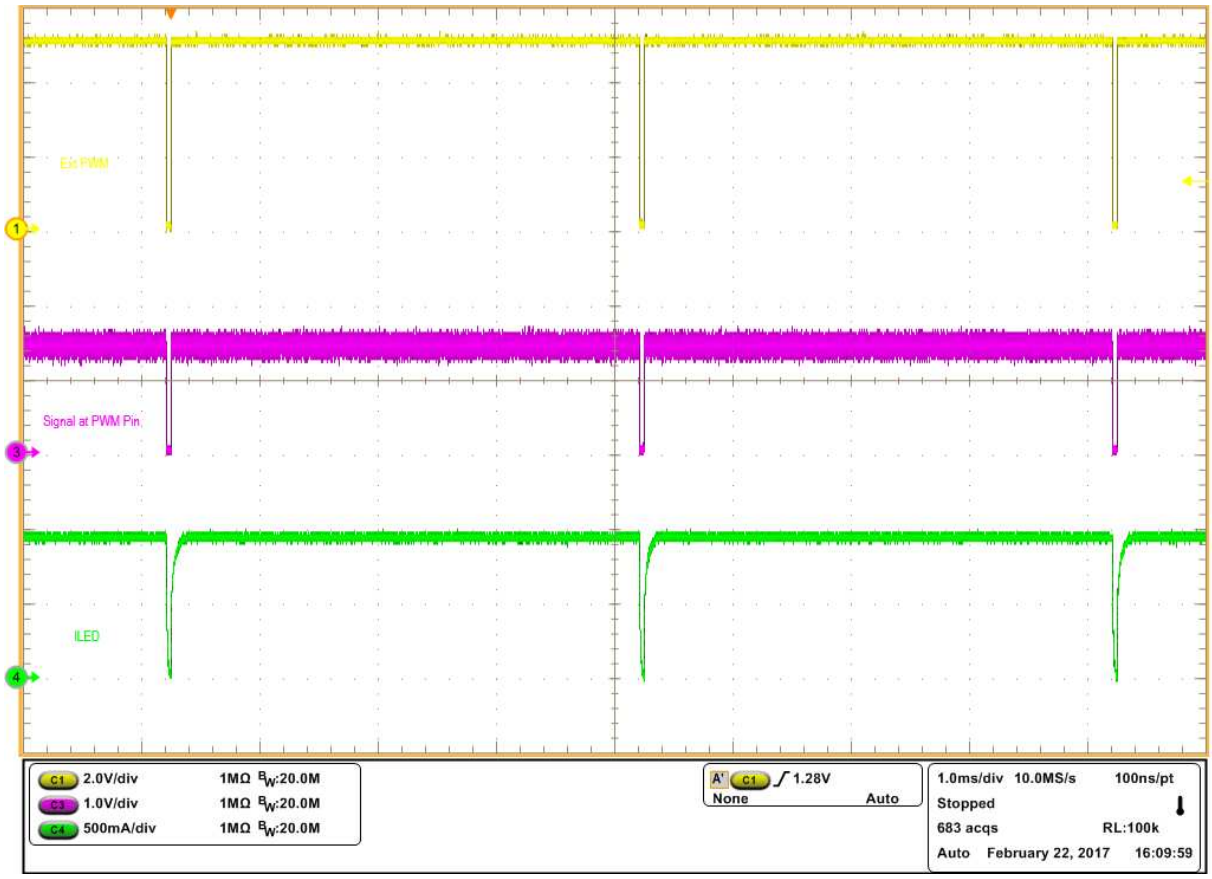

Figure 19. PWM Dimming With 99% Duty, 250 kHz

5 References

1. *TPS54200 and TPS54201 4.5-V to 28-V Input Voltage, 1.5-A Output Current Synchronous Buck WLED Driver* data sheet (SLUSCO8)
2. *TPS54200EVM-818 28-V, 1.5-A Buck LED Driver Evaluation Module* user's guide (SLUUBI2)
3. *TPS54201EVM-818 28-V, 1.5-A Buck LED Driver Evaluation Module* user 's guide (SLUUBM3)

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