Hardware Design Guideline for TPS65987DDH USB Power Delivery Controllers

TPS65987DDH is a 3rd generation of USB Power Delivery Controllers from Texas Instruments. This device is compliant to USB Power Delivery Specification 3.1 and USB Type-C Specification 1.2.

This device integrates power FETs, various power management features, BC 1.2 host and device, 20 GPIOs, a Cortex M0 core and so forth. The integrated FETs inside the device supports up to 60 W of power per port. It includes all the necessary power management and protection circuitry such as reverse current protection (RCP), under voltage protection (UVP), over voltage protection (OVP) and so forth. Most of the GPIOs can be assigned to various events to control various parts of the system such as alternate mode multiplexers, DC-DC converters and so forth. A combination of all these features in a single chip provides a compelling solution for notebooks, docking stations and other space constrained applications.

This application note provides guidelines to design hardware using the TI PD Controller. This application note explains the features, pins, and signals of the device. It also shows how to maintain signal integrity for high speed signals.

For more information on applications and use cases, customers should refer to the data sheet and other application notes for this device.

1 Schematic Design Guidelines

This section provides the guidelines and recommendations to be used while working with the schematic. This section provides details of all the major interfaces available in this device, and how to leverage these interfaces in your design. For more details and a schematic checklist, refer to Appendix A.

1.1 Configuration Channel / VCONN Lines

Configuration Channel (CC) lines are the most important lines in terms of Type-C and PD communication. These lines are responsible for all the Type-C and PD negotiations between the devices. A Type-C/PD port has two CC lines, CC1 and CC2. Only one of the CC line is used for communication when a Type-C device is connected. The remaining CC line converts into VCONN to provide 5-V power to the cable electronics if applicable. VCONN current of up to 600 mA of is supported when Ra is presented. However, in a device with captive cable, the CC line and the VCONN is fixed. The cable is hardwired on one of the end; therefore, high speed signal muxing is not required.

Ensure the CC lines of the PD Controller are directly connected to the Type-C receptacle. Avoid any passive components such as 0-Ω resistance between the CC pin in the PD chip and the CC pin in the Type-C receptacle. CC lines have a stringent eye-diagram requirement and a capacitor is placed between CC line a ground to meet the eye-diagram requirements. The value of these capacitors should be tuned if there is any failure seen on the CC eye-diagram. Refer to the data sheet to find the right value of capacitor to be placed between the CC line and ground. Place the PD controller close to the Type-C receptacles to avoid voltage drop in long traces.

1.2 I²C Lines

There are three I²C ports in this device. See Table 1 to understand the features offered by each of the I²C port. I²C ports can be used as an I²C master to control an I²C slave, like an alternate mode mux, battery charging controller and so forth. At the same time, I²C ports can be used as an I²C slave to provide Host Interface to control the various features of the chip. All the I²C ports can support Fast (400 KHz) and Standard (100 KHz) I²C modes with burst writing. All the I²C lines must have proper pull-ups preferably from the LDO_3V3 rail. Even the unused I²C port must be pulled up using a 10-KΩ resistance.

Table 1. I²C Port Features

Port	Master	Slave	Comments
I²C1	Yes	Yes (Default)	Should be connected to the embedded controller of the PC
I²C2	No	Yes	Should be connected to Thunderbolt controller of the PC
I²C3	Yes	No	Should be used to control the external I2C slave devices like MUX, Battery Chargers, and so on.

1.3 SPI Lines

This device can boot from its ROM and provide 5 most commonly used configurations without using the SPI flash. Proper pin strapping must be done as per the device datasheet to boot the device with right configuration.

However, an external SPI flash can be used if the system requires customized configurations which are not supported by the ROM. SPI Flash must be powered from LDO_3V3 when used and must be able to work at 12 MHz or higher. Place a 0.1-µF capacitor close the supply pin of SPI flash to filter out noise. Add pull-ups on the CS, MISO, WP and HOLD lines. TI suggests “W25X05CL” or similar SPI flash for the system.

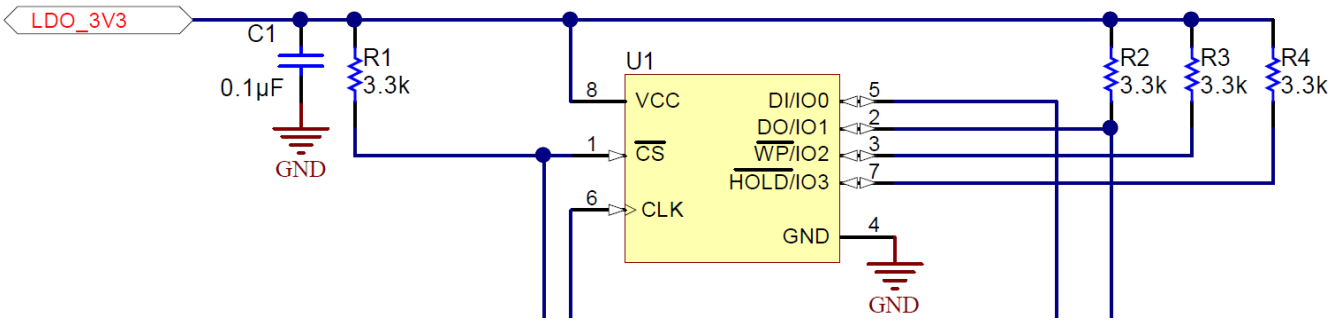

Figure 1. Recommended Pull-ups for SPI Flash

1.4 Cx_USB_y Lines

This device has 2 USB lines which can be used for BC1.2 detection, or as standard GPIOs. Connect these pins to USB 2.0 lines and at the same time use these pins for BC1.2 detection. If lines are not used, any event can be assigned to the lines for BC 1.2 detection.

1.5 Hot Plug Detect or HPD Line

This pin is used for Display Port (DP) communication. The port partners send a HPD message over Type-C communication when connection to a DP device is detected. The PD controller changes the state of its corresponding line after the message is received.

1.6 ADCIN1

This pin is used for boot strap pin for device initialization. In dead battery operation, the chip voltage at the VBUS pin determines how the power is used. This pin along with the SPI_MISO pin with help to pick the right device configuration from the ROM. A potential divider should be used between LDO_3V3 and GND to pick the right configuration. Please refer the device datasheet for more information.

1.7 ADCIN2

This pin is used to set the I²C address of the device. At boot time, the chip determines the voltage and sets the I²C address. A potential divider must be used between LDO_3V3 and GND to get the desired I²C address. I²C address of the I²C port 1 as per Table 2

A potential divider must be used between LDO_3V3 and GND to get the desired I²C address. I²C address of the I²C port 1 as per Table 2.

Table 2. I²C Address of the I²C Port 1

DIV = R2/(R1 + R2)		Default Unique Address I2C1 – Port1 (7-bit)	Default Unique Address I2C1 – Port2
DIV MIN	DIV MAX		
Short ADCIN2 to GND		0x20	0x24
0.20	0.38	0x21	0x25
0.40	0.58	0x22	0x26
Short ADCIN2 to LDO_3V3		0x23	0x27

1.8 GPIOs

This device has multiple GPIOs which could be used to assign PD events from the device configuration tool. These GPIOs supports multiple event options to indicate various states. It can take inputs from the system to make appropriate decisions. All the unused GPIOs should be left floating in the hardware. Some of the GPIOs have specific features and should be used accordingly. Refer to the TPS65987DDH schematic checklist in the Appendix of this document.

1.9 PP_EXT

These signals are used to control the external power FETs. Note that these pins are not high voltage tolerant, and require a driver FET to drive the power FETs.

The PP_EXT pins can be used as GPIOs if external FETs are not used.

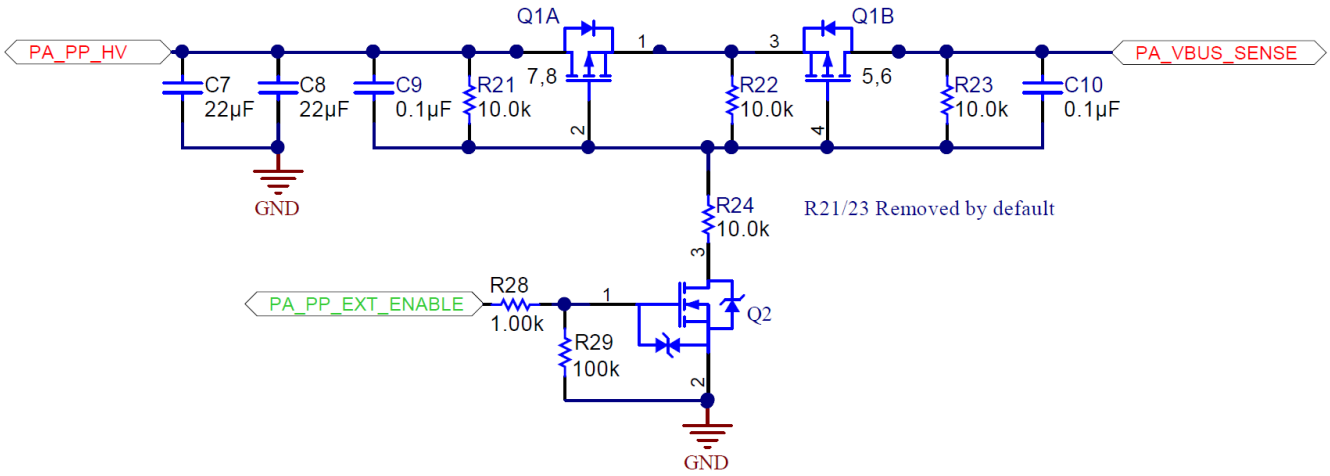

Figure 2. PP_EXT Path With Driver

1.10 PP_CABLE

The 5-V supply to these pins are used to provide VCONN on the unused CC pin. Current passing through these pins is monitored internally. The VCONN FET turns off if current goes above 600 mA. This provides over current protection on VCONN.

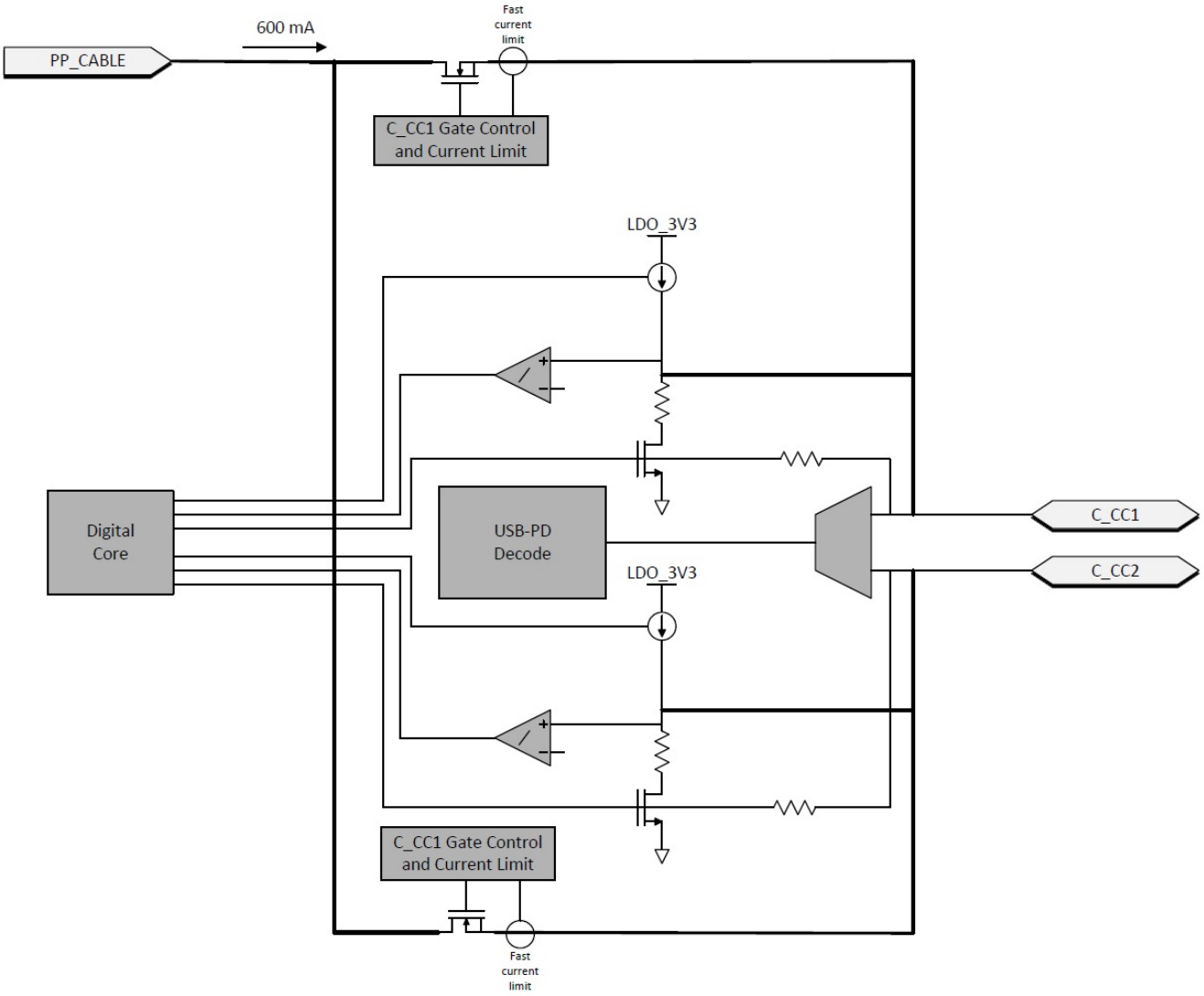

Figure 3. Port Power Switches

1.11 VIN_3V3

This is the main power supply rail for the chip. Provide a clean 3.3 V on this pin. Place a 10-µF capacitor close to this pin. Try to use a DC-DC converter to generate 3.3 V for higher efficiency. A normal LDO can be used, but they are not efficient.

1.12 LDO_3V3

LDO_3V3 is the supply for the core chip. It can be powered from VIN_3V3 output of LDO driven from VBUS. LDO_3V3 is available when the chip is powered. Therefore, this rail can be used to power up the external SPI flash and pull-ups in the system. This line can supply only 25 mA of current to external devices. Do not overload it by connecting un-necessary devices on this rail.

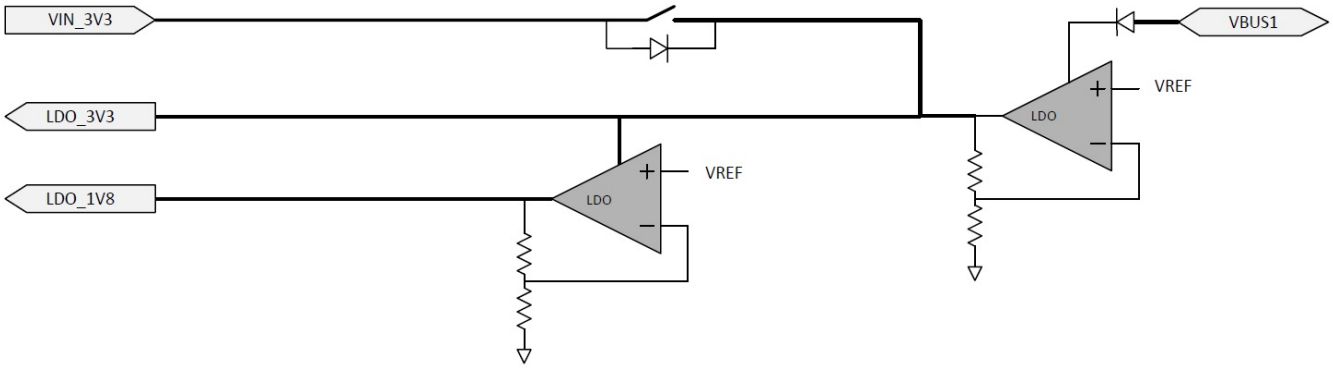

Figure 4. Power Supply Scheme

1.13 Power Path Considerations

It is required to protect the power path on the PD controller from voltage transients that violate the absolute maximum ratings in the datasheet. This helps prevent a system from being damaged in the field. For an external power path, it is recommend to use components that have a voltage rating similar to the PD controller or better to ensure it does not fail due to overvoltage conditions. It is also highly recommended to protect the external power path with reverse current protection (RCP).

For VBUS, it is recommended to place a Schottky diode on the VBUS to absorb GND currents during short or sudden disconnect events. The Schottky diode protects all of the devices connected to the VBUS, and absorbs the current when the VBUS falls below GND. The forward voltage for the Schottky diode must be as low as possible (recommended 500 mV or lower) to protect the internal diodes of the devices connected to the VBUS. Better alternatives to a Schottky diode like a uni-directional Transient Voltage Suppressor (TVS) device, such as the TVS2200, may be used to protect against overvoltage conditions and GND currents. The forward voltage of the TVS device must also be as low as possible.

When connecting an external power supply (barrel jack) directly to the the PPHV1 and PPHV2 paths, it is crucial to protect the power path from transient voltages caused by a hot plug. At minimum, expect to see double the external power voltage during the hot plug (up to 40 V for a 20 V barrel jack). Proper system design must include minimizing the transient voltage to protect the power paths of the PD controller and other devices directly connected to the external supply. There are various protection designs that can be considered: Input power filter (Ferrite Bead and Capacitor), soft-start circuit (Power FET), or input power filter with TVS. For external supplies with very high output capacitance, a combination of these protection schemes may be required. It is also important to have the necessary PPHV1 and PPHV2 bulk capacitance to meet the source requirements and PD specification.

The best practice for supplying power to the PPHV1 and PPHV2 paths is to use a regulated controlled supply. For systems that support 5 V only, the system 5-V supply can be connected directly as long as the turn-on ramp rate is controlled. In the case for systems that supply up to 100 W (5 V/9 V/15 V/20 V), a variable DC/DC converter feeds directly into the PPHV1 and PPHV2 paths, which is also a controlled ramp rate. It is required that the power supplies connected to PPHV1 and PPHV2 (DC/DC or AC/DC converters) do not violate the absolute max voltage ratings of the PD controller.

NOTE: When power path protection is *not* used, it may lead to reliability issues, and can cause irreversible damage to the system. Additional protections on the power path help prevent failures when non-compliant or damaged products are connected to the system.

2 Layout Guidelines

This section includes the recommendations which must be used while designing with the TPS65987DDH PD controllers. Not all the recommendations can be used depending on the design, and therefore the designer is expected to determine the requirements to achieve the design goals. Use the guidelines in Section 10 of the device datasheet for addition information.

2.1 Power Domain

This device is designed for PD power up to 60 W through the internal power paths and can support up to 100 W of power if external power FETs are used. Use these basic guidelines to avoid design issues:

1. The use external FETs with big packages is preferred because they dissipate heat. During rapid temperature rise, smaller FETs can cause damage due to a short circuit. Bigger FETs can dissipate the heat much faster, and stay protected.
2. Provide wide traces for all the high current paths like VBUS, PP_HV, PP_EXT to ensure a low resistance path or power plane for VBUS.
3. Ensure enough free space and copper around the power devices to facilitate heat dissipation.
4. Avoid any vias in high current path, but if required, then provide at least one via for every 500-mA current.
5. Provide at-least 8 mills trace for CC lines to support high currents for VCONN supply.
6. Place decoupling caps close to the power supply pin.
7. Provide at-least eight vias for the ground pad beneath the chip. These vias should run from top layer to the bottom layer. These vias ensure good electrical and thermal conductivity and helps to dissipate heat generated in the chip.
8. For the two split FET pads, provide at least 6 thermal vias underneath each pad. These vias must be electrically isolated (NC). Ensure these vias run from top layer to bottom layer and are preferably tented.

2.2 Hi Speed Lines

In a USB PD system, hi speed signals can reach up to 10 Gbit/s. In a Thunderbolt 3 based system, the data rate can rise to 40 Gbit/s. At high data rates, signal integrity may not be maintained. Use these guidelines to avoid signal quality issues.

1. Ensure SuperSpeed or Alternate Mode multiplexers are placed close to the Type-C receptacle. This is required to avoid signal quality issues as the high speed lines can directly be routed to the multiplexer.

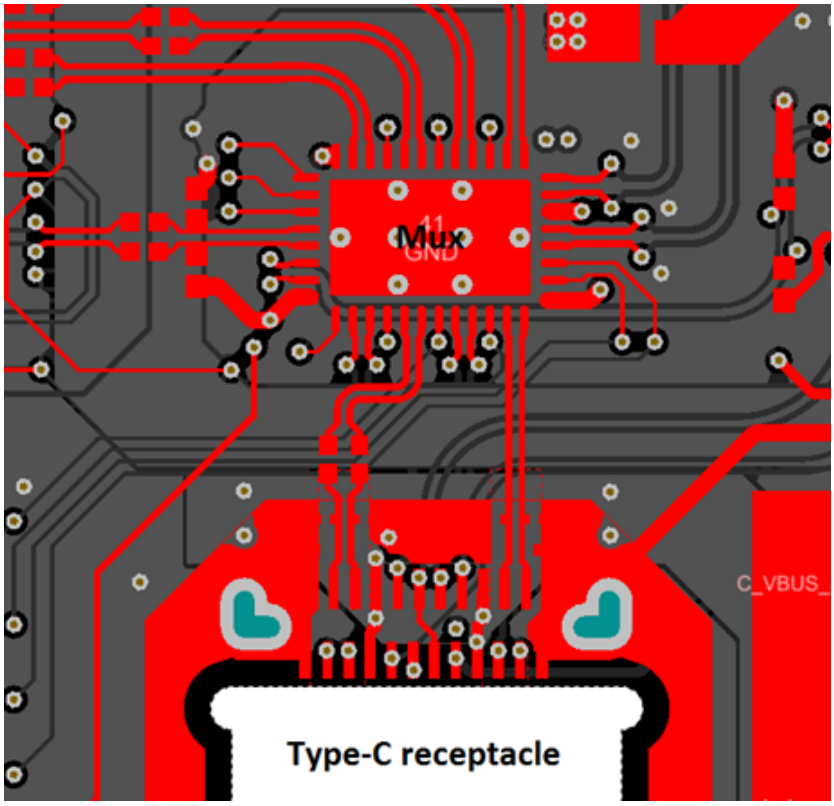

Figure 5. High Speed Signal Routing Example

2. Do not place switching circuits close to the multiplexer and the high speed signal traces to avoid noise coupling in these signals.
3. Maintain 90-Ω differential impedance for high speed signals.
4. Two differential pairs must be separated by at least three times the width of the differential pair and should be uniformly laid out.
5. Intra Pair length of the differential pair traces should be matched within 5 mills.
6. Avoid bents on high speed signals. If required, then use curved bents or 45° bents. Never use 90° bent.

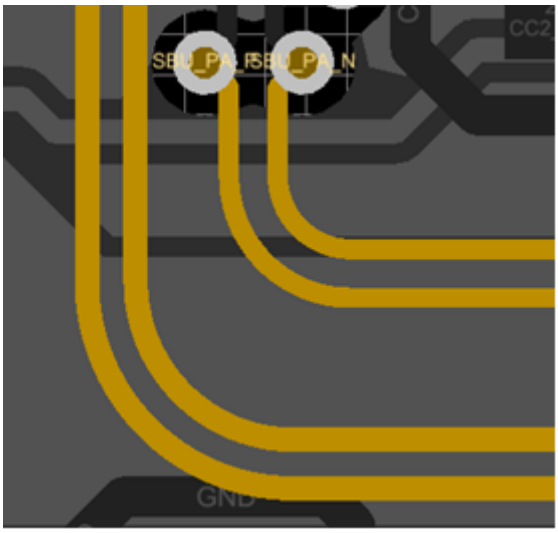

Figure 6. Recommended Signal Bents

7. If two pairs of high speed signals cross each other on two planes, then there must be a ground plane between these two planes.
8. Maintain continuous grounding while changing the layer of high speed signal to ensure uniform impedance. When placing a via on a high speed signal, place GND vias next to them to maintain uniform impedance.

2.3 Other Considerations

This section covers other design considerations such as placement of components and other best practices to be followed.

1. Try to reduce the distance between the Type-C receptacle and the CC pins of the PD Controller. Place the 220-pF capacitor close to the PD Controller. The capacitors on the CC lines help to tune the eye-diagram of CC signals.
2. Place ESD diodes as close as possible to the Type-C receptacle.
3. The ESD components must be placed without stubs in a pass through manner on the differential path.
4. Keep all the power regulators away from the high speed signals and associated components.

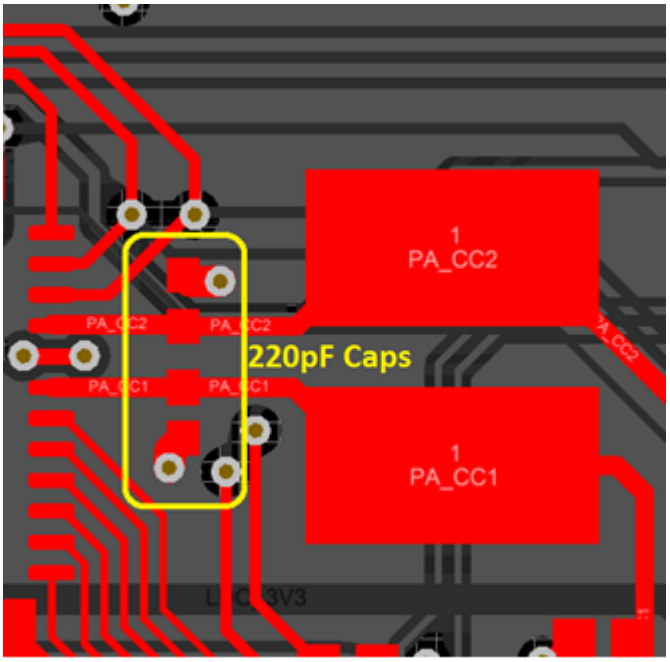

Figure 7. Placement of Capacitors on CC Lines

3 Summary

This application note describes important considerations for schematic and layout design. A system designer is expected to follow all the recommendations mentioned in this application note as well as refer all other relevant application notes and specifications before starting any design with TPS65987DDH PD Controller.

4 References

- TPS65987 USB Type-C and PD Controller with Integrated Power Switches, SLVSDB0

Appendix

A.1 Dead Battery Considerations

In Dead battery condition, the system power is not available. The whole system must run on the VBUS coming in from the source end. TPS65987DDH has a built in LDO which powers it up. A laptop normally requires an embedded controller (EC) to turn on and manage the PD ports as per the system requirements. When the system supply is not available, there should be an additional regulator sitting from the VBUS or PP_HV/PP_EXT to generate 3.3 V to power up the EC and other critical parts of the system. There are two ways this can be done.

1. Using a LDO from VBUS: This device powers up once the VBUS is available and negotiates at least a implicit contract. The VBUS turns on after this and it powers up the LDO which in turn powers up the EC and other required components. This scheme can be used even when the system power comes up only after issuing SRDY command, or BUZPOWERZ configuration is such that the power path is not turned on until instructed by EC.

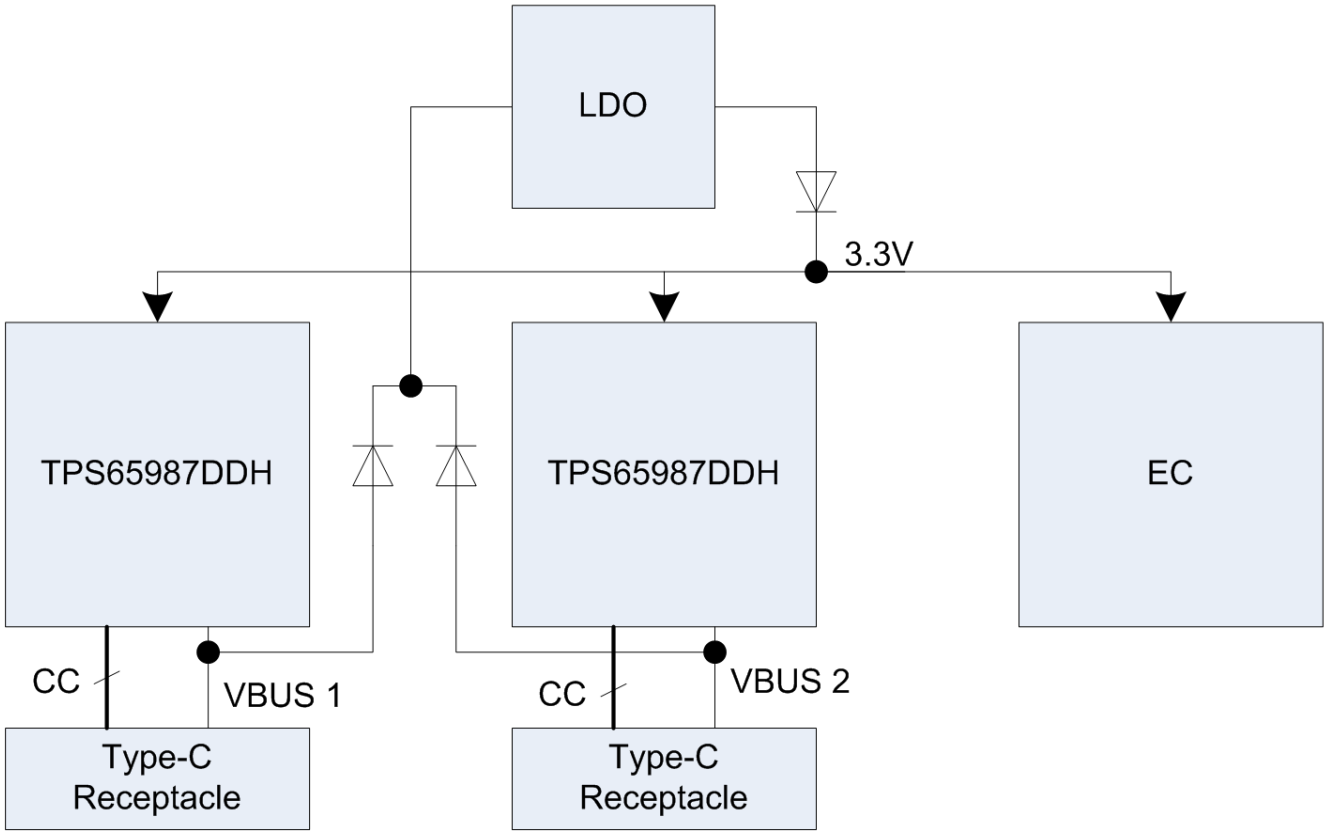

Figure 8. Using a LDO from VBUS

2. Using a LDO from PP_HV/PP_EXT of the PD controller: In this mode, this device turns on from its built in LDO. It negotiates a contract and turns on the power FETs. The moment the FETs are on, they power up the LDO which powers all other required components.

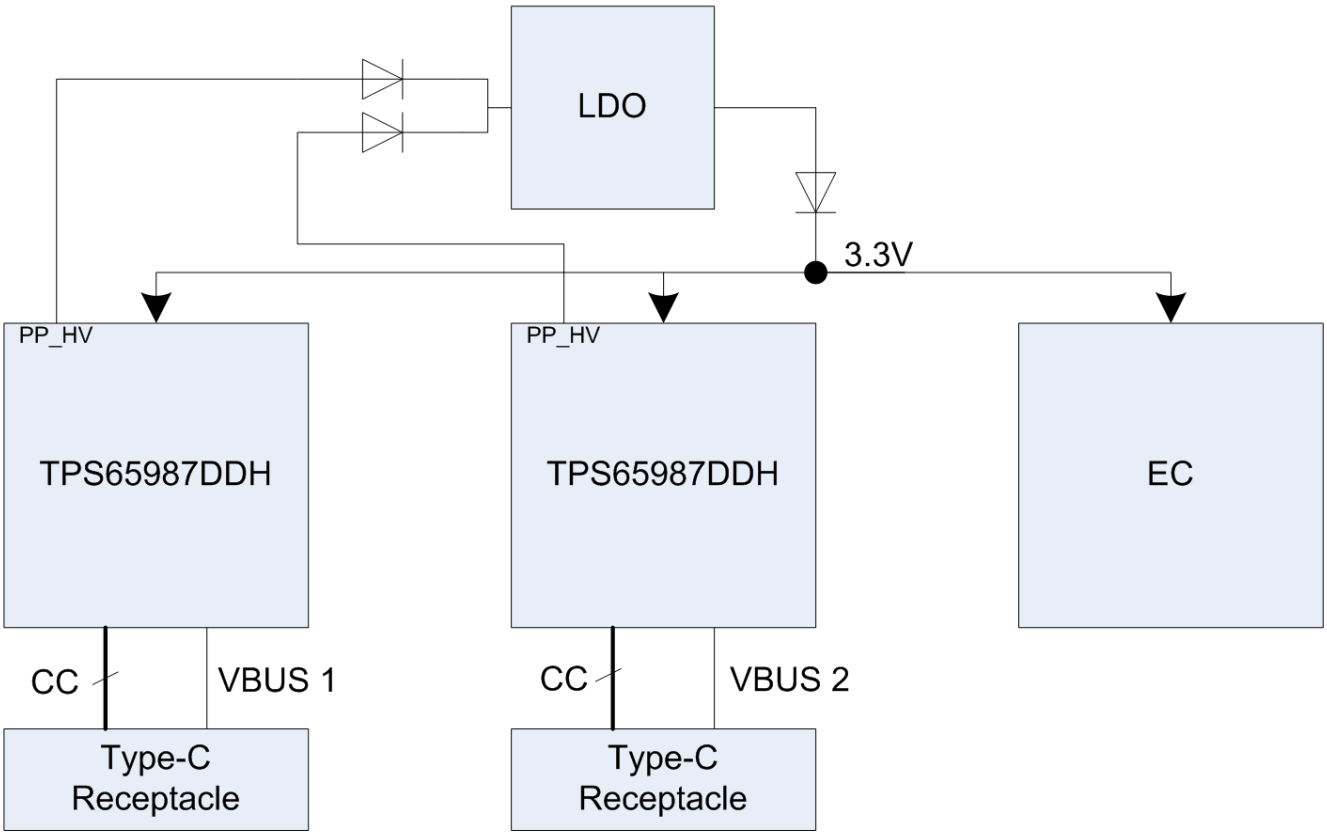

Figure 9. Using a LDO from PP_HV/PP_EXT

A.2 TPS65987DDH Schematic Checklist

Table 3. TPS65987DDH Components and Pins Checklist

Pin name	Pin Number	Description	Min	Typ	Max	Comment
Decoupling caps						
LDO_1V8	35	Bypass with appropriate capacitor	2.2 uF	4.7 uF	6 uF	
LDO_3V3	9	Bypass with appropriate capacitor	5 uF	10 uF	25 uF	
VIN_3V3	5	Bypass with appropriate capacitor	5 uF	10 uF		
PP1_CABLE	25	Bypass with appropriate capacitor	2.5 uF	4.7 uF		
PP_HV1	11,12	Bypass with appropriate capacitor, ground pin if unused	1 uF	47 uF	120 uF	Sink
			2.5 uF	4.7 uF		Source
PP_HV2	1,2	Bypass with appropriate capacitor, ground pin if unused	1 uF	47 uF	120 uF	Sink
			2.5 uF	4.7 uF		Source
VBUS1	13,14	Port side VBUS bypass with appropriate capacitor, tie to ground if unused	500 nF	1 uF	12 uF	
VBUS2	3,4	Port side VBUS bypass with appropriate capacitor, tie to ground if unused	500 nF	1 uF	12 uF	
Application Specific Pins						
SPI_MISO/GPIO8	36	Ground pin if unused				
SPI_MOSI/GPIO9	37	Ground pin if unused				
SPI_CLK/GPIO10	38	Ground pin if unused				
SPI_SS/GPIO11	39	Ground pin if unused				

Table 3. TPS65987DDH Components and Pins Checklist (continued)

Pin name	Pin Number	Description	Min	Typ	Max	Comment
I2C1_SCL	27	Should be always pulled up using a resistance and connected to central processor if available	2.2 KΩ	3.3 KΩ	4.7 KΩ	
I2C1_SDA	28	Should be always pulled up using a resistance and connected to central processor if available	2.2 KΩ	3.3 KΩ	4. 7KΩ	
I2C1_IRQ	29	Should be always pulled up using a resistance		10 KΩ		
I2C2_SCL	32	Should be always pulled up using a resistance and connected to Thunderbolt controller if available	2.2 KΩ	3.3 KΩ	4.7 KΩ	
I2C2_SDA	33	Should be always pulled up using a resistance and connected to Thunderbolt controller if available	2.2 KΩ	3.3 KΩ	4.7 KΩ	
I2C2_IRQ	34	Should be always pulled up using a resistance		10 KΩ		
I2C3_SCL/GPIO5	21	Should be always pulled up using a resistance and connected to external I2C slaves if available	2.2 KΩ	3.3 KΩ	4.7 KΩ	
I2C3_SDA/GPIO6	22	Should be always pulled up using a resistance and connected to external I2C slaves if available	2.2 KΩ	3.3 KΩ	4.7 KΩ	
I2C3_IRQ/GPIO7	23	Should be always pulled up using a resistance		10 KΩ		
ADCIN2/I2C_ADDR	10	Connected to appropriate pullup/pulldown combination	Refer Datasheet			
SWD_CLK/GPIO12	40	Float pin if unused				
SWD_DATA/GPIO13	41	Float pin if unused				
PP_EXT1/GPIO16	48	Signal for external FETs, can be used as a GPIO too, float pin if unused				
PP_EXT2/GPIO17	49	Signal for external FETs, can be used as a GPIO too, float pin if unused				
ADCIN1/BUSPOWERZ	6	Connected to appropriate pullup/pulldown combination	Refer Datasheet			
HRESET	44	Ground pin using a pull-down and cap if used else ground directly				
C1_CC1/C1_CC2	24/26	Connect to Type-C connector, add an ESD protection device and a cap		220 pF		
HPD1/GPIO3	30	Connect to HPD if used in DisplayPort configuration, float pin if unused				
C_USB_P/GPIO18	50	Connect to USB 2.0 lines of connector if BC1.2 is required, can be used as a GPIO if BC1.2 is not required				
C_USB_N/GPIO19	53	Connect to USB 2.0 lines of connector if BC1.2 is required, can be used as a GPIO if BC1.2 is not required				
GPIOs						
GPIO0	16	Resetz pin, should be ties to thunderbolt driver, can also be used as a GPIO				
GPIO1-GPIO2	17,18	General purpose IOs, float if unused				
GPIO4	31					
GPIO14(PWM)	42	General purpose IOs, float if unused				
GPIO15(PWM)	43	General purpose IOs, float if unused				
GPIO20-GPIO21	54,55	General purpose IOs, float if unused				
GND	20,45,46,47,51 ,59	Connet to ground				
DRAIN1	8,15,19,58	Connect all these pins together				Have a pad on the layout for heat dissipation
DRAIN2	7,52,56,57	Connect all these pins together				Have a pad on the layout for heat dissipation

A.3 TPS65987DDH System Checklist

Table 4. System Checklist

Item#	DESCRIPTION	Yes/No
1	Are all the bulk caps connected as per the TPS65987DDH Components and Pins Checklist?	
2	Are all the decoupling caps connected as per the TPS65987DDH Components and Pins Checklist?	
3	Are all the I2C and SPI pull-ups are connected from LDO_3V3 rails?	
4	Is there a protection diode on the VBUS rail?	
5	Is there ESD protection available on all the lines exposed out of the system?	
6	Is proper resistors are used for pin strapping?	
7	All the signals are routed properly to AM mux?	
8	Is all datasheet requirements are met?	
9	Is SPI Flash is powered from LDO_3V3?	

4 Trademarks

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to B Revision **Page**

- Updated power path section 5

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