Application Report
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High-Side Switches Paralleling Channels

Mahmoud Harmouch

ABSTRACT

The *Smart High-Side Switch* family from Texas Instruments can drive a diverse set of loads for different systems. For some systems, the current demand is higher than the capacity for a single channel. One possible solution is to parallel multiple channels within one device. Paralleling channels together provides a means of increasing output current beyond the capabilities of a single channel. This application report details the paralleling process and addresses the limitations to be considered for an optimized solution.

Contents

List of Figures

List of Tables

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1 Introduction

A single channel may have enough current capability to drive a steady-state load at low ambient temperatures and keep the junction temperature below the maximum limit of 150ºC. However, at higher ambient temperatures, the load still may still demand the same load current. The physical limitation of any semiconductor device should be considered due to an increase in on-resistance with temperature, which can lead to even higher power losses. The additional power losses will manifest themselves in the form of heat, and must be dissipated to keep the junction temperature below 150ºC. This may require a heat sink, which is an added cost to the system. The main reason for paralleling channels is to lower the on-resistance, which will translate into lower power losses and will avoid an expensive heat sink. TI's high-side power switches with multiple channels which may be paralleled include:

TPS4H160	TPS2H160
TPS4H000	TPS2H000
TPS2HB08	TPS2HB16
TPS2HB35	TPS2HB50

These smart high-side switches with multiple channels are designed for use in 12-V automotive and 24-V industrial systems. They offer full diagnostics, internal and programmable external current limit, and high accuracy current sensing with no need for system calibration. They have the advantage of driving a single, heavy load by paralleling all channels, multiple medium loads by paralleling some of the channels, and driving light loads with single channels. Paralleling enables these devices to drive LEDs, solenoids, capacitive loads and DC motors that exceed the current rating for a single channel. For complete feature descriptions, refer to the device-specific data sheet.

2 Paralleling Channels: Definition

Paralleling channels means connecting multiple power FETs in parallel to source current to a single load. The load current is shared and each channel carries the load current divided by the number of paralleled channels. By paralleling channels, the equivalent on-resistance value is the on-resistance of a single channel divided by the number of paralleled channels. The following sections highlight features supported in this configuration, as well as limitations.

CAUTION

TI recommends using the external current limiting for safe operation, and the total load current must be limited to the internal specified current limit per channel.

3 Features and Considerations

The standard operation of the device is very similar when paralleling channels together. Table 1 summarizes the features and considerations for the device under this use case:

Table 1. System Features

Feature	Single Channel Operation	Paralleled Channels Operation
Maximum load current: I_{max}	Limited by capability of single channel: $I_{max\ single\ Ch}$	Up to the number of paralleled channels × current of a single channel: $N \times I_{max\ single\ Ch}$
External programmable current limit	Controlled by external resistor	Controlled by external resistor, same limit for each individual channel
Maximum short-circuit current	Limited by capability of single channel	Limited by capability of single channel. Maximum current limit during short-circuit does not scale with number of channels
Current sensing	Reported for individual channel	Reported for individual channel. Full load current will be the addition of each current sense reading
Diagnostics: short to battery, short to ground, open load (on and off state)	Reported for individual channel	Globally reported, as the fault condition affects all channels simultaneously
AECQ100-012 performance	Reported on the device-specific data sheet	Not tested
Inductive load demagnetization energy	Reported on the device-specific data sheet	Not tested

4 Considerations When Connecting Channels in Parallel

The performance of channels connected in parallel is expected to work as the equivalent single channel in terms of both power delivery and diagnostics.

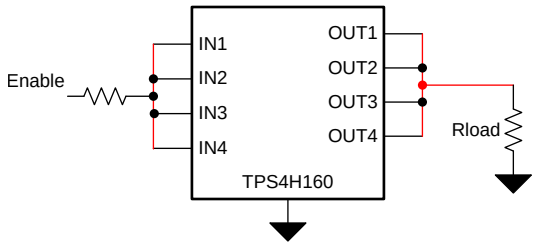


Figure 1. Input and Output Connections Using TPS4H160 as Example

Complete the following for optimal performance:

1. Connect the input pins of all paralleled channels close to the device.
2. Connect the output pins of all paralleled channels close to the device with minimum stray inductance.
3. Parameter tolerances such as on-resistance, current limit ratio, and voltage clamp must be taken into consideration.
4. The programmed, maximum current limit per channel must be less than 1 / (Number of paralleled channels) of the internal current limit of a single channel.

5 Current Sharing

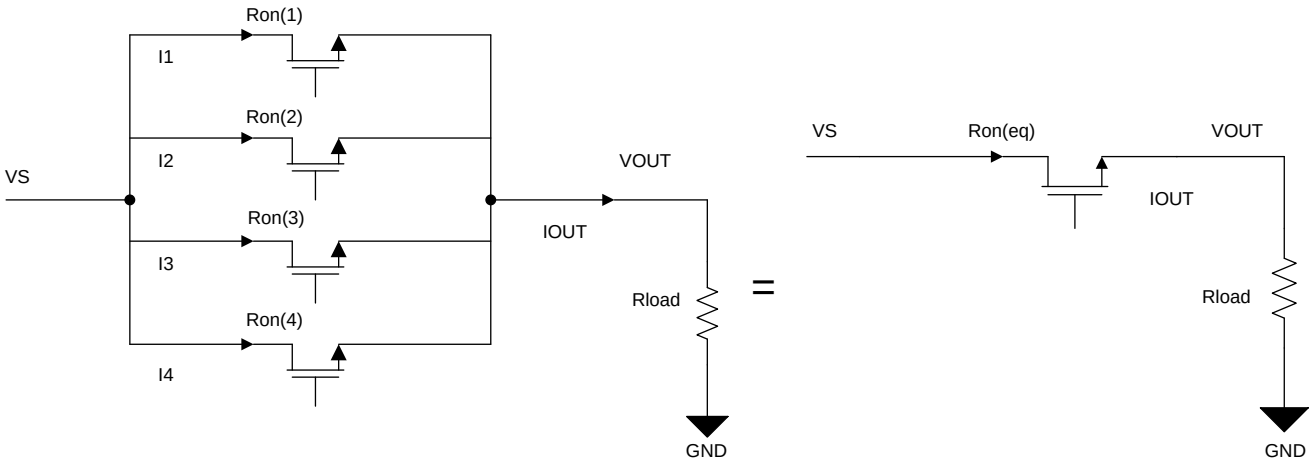


Figure 2. Representative of Using a High-Side Switch With 4 Channels in Parallel

Channels in parallel have the same voltage drop from input to output (VS – VOUT). The total current is the sum of all the currents from each of the individual channels. The total resistance analysis is based on an example with 4 channels in parallel. Figure 2 illustrates the connection of 4 paralleled channels at supply voltage VS node and output VOUT node. The left side of Figure 2 shows 4 individual on-resistances and currents. The right side of Figure 2 shows the equivalent on-resistance and the total current IOUT.

$$VS - VOUT = Ron(1) \times I1 = Ron(2) \times I2 = Ron(3) \times I3 = Ron(4) \times I4 = Ron(eq) \times IOUT, \text{ see Figure 2} \quad (1)$$

$$IOUT = I1 + I2 + I3 + I4, \text{ see Figure 2} \quad (2)$$

In an ideal scenario, the currents are equally shared and the expected load current (IOUT) is 4 times the single channel current. This is only true if the single channel on-resistances are exactly equal, but in reality this is not the case. There is always some channel-to-channel on-resistance deviation, ΔR, which causes an unbalanced load sharing. This deviation is due to process variation within the same device.

If the on-resistance of a single channel has a maximum tolerance of ΔR / Ron(typ), the maximum individual current tolerance is 2× ΔR / Ron(typ). The nominal current in an individual channel is IOUT / 4, where IOUT is the total output current going into the load. The lowest individual channel current is calculated as Equation 3 shows, derived from Equation 1 and Equation 2:

$$\frac{IOUT}{4}\left(1-2\left|\frac{\Delta R}{Ron(typ)}\right|\right) \quad (3)$$

The highest individual channel current is calculated as Equation 4 shows, derived from Equation 1 and Equation 2:

$$\frac{IOUT}{4}\left(1+2\left|\frac{\Delta R}{Ron(typ)}\right|\right) \quad (4)$$

For reference, see Figure 2.

Process deviation within one device may be up to 10%. This leads to 10% on-resistance variation from channel to channel.

With 4 paralleled channels, the lowest current in one individual channel, using Equation 3, is estimated using Equation 5:

$$(1-0.2)\frac{IOUT}{4} = 0.2 \times IOUT \quad (5)$$

The highest individual current, using Equation 4, is found using Equation 6:

$$(1+0.2)\frac{IOUT}{4} = 0.3 \times IOUT \quad (6)$$

where

- IOUT = the total load current

Refer to Appendix A for detailed analysis on n paralleled channels.

6 Setting the External Current Limit

To provide the expected total current to the load, each individual channel must deliver its portion of current. For that reason, the tolerances of different parameters must be considered while setting the external current limit. When an individual channel reaches its current limit, the corresponding FET goes into saturation region. Since all drains and sources of the FET are connected, the other FETs from the remaining channels are forced into the saturation region as well. If the tolerances are not considered, the load current can be switched off prematurely before the expected overcurrent or short-circuit limit has reached.

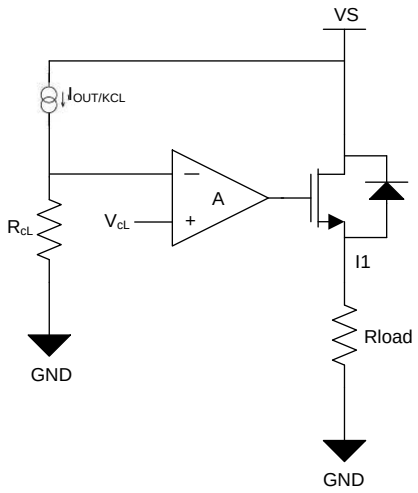


Figure 3. Individual Current-Limit Function

The current limit function is a closed loop with a precise internal band-gap reference V(cL). The individual channel load current is mirrored with a typical ratio of K(cL). By adding an external pulldown resistor, R(cL), the closed loop equates the voltages at the inputs of the error amplifier. This results in Equation 7:

$$V(cL) = R(cL)\frac{I}{K(cL)} \quad (7)$$

where

- I represents an individual channel load current

The current ratio, K(cL), has a deviation of dK(cL) due to process variation. The maximum tolerance (dK(cL) / K(cL)) is specified in the data sheet. The individual current limit is set by the external resistor R(cL), and it can be calculated using Equation 8:

$$R(cL) = V(cL)\frac{K(cL)}{I} \quad (8)$$

The following analysis is based on 4 channels in parallel. The parameters needed to calculate the tolerance are the individual channel load current I, and the ratio K(cL). This gives Equation 9:

$$R(cL) = V(cL) \frac{K(cL)\left(1 + \frac{dK(cL)}{K(cL)}\right)}{\frac{IOUT}{4}\left(1 + 2\frac{\Delta R}{Ron(typ)}\right)} \tag{9}$$

To deliver the expected load current before reaching the current limit, R(cL) should be calculated with the worst-case tolerances (see Equation 10):

$$\text{The max value of } R(cL) = V(cL) \frac{K(cL)\left(1 - \left|\frac{dK(cL)}{K(cL)}\right|\right)}{\frac{IOUT}{4}\left(1 + 2\left|\frac{\Delta R}{Ron(typ)}\right|\right)} \tag{10}$$

The load current lower limit from Equation 10 is shown in Equation 11:

$$IOUT = 4\frac{V(cL)}{R(cL)} \frac{K(cL)\left(1 - \left|\frac{dK(cL)}{K(cL)}\right|\right)}{\left(1 + 2\left|\frac{\Delta R}{Ron(typ)}\right|\right)} \tag{11}$$

At this limit, the expected current is delivered to the load while the FETs are in the linear region, before any individual channel hits current limit. Equation 12 is derived from Equation 10:

$$\text{The total load current upper limit is } IOUT = 4\frac{V(cL)}{R(cL)} \frac{K(cL)\left(1 + \left|\frac{dK(cL)}{K(cL)}\right|\right)}{\left(1 - 2\left|\frac{\Delta R}{Ron(typ)}\right|\right)} \tag{12}$$

At this limit, there is an increase in junction temperature while the FETs are in linear and before any individual channel hits current limit.

7 Diagnostics

Integrated diagnostic features report faults to the MCU. The types of faults detected include open load, short to battery, overcurrent, thermal shutdown, thermal swing, and reverse polarity. Some high-side switches have the option to report faults through an open drain status pin or through an analog current sense pin. See the device-specific data sheet for details.

For devices that feature an analog current sense pin, the load current status is reported by selecting an individual channel through logic input pins. Since the channels are paralleled, the diagnostics can be simplified as Table 2 shows:

Table 2. Diagnostics Features

Diagnostics Feature	Behavior When Channels are Paralleled
Open load	No need to select individual channel for diagnostics. Since all channels are connected together, the fault will be present on all channels.
Short to battery	
Overcurrent	
Reverse polarity detection	
Thermal swing	Individual channel selection is required. A particular channel may reach the fault independently from others.
Thermal shutdown	

Table 2. Diagnostics Features (continued)

Diagnostics Feature	Behavior When Channels are Paralleled
Load current in nominal condition	Each individual channel reports load current independently. The current sense pin provides the status of individual channels only. To report the total load current to the MCU, each individual current must be selected and added.

8 Inductive Load-Switching Off Clamp

When switching off an inductive load, the inductive reactance pulls the output voltage negative due to high L(dI / dt). Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal Vds clamp (between the drain and source for an individual channel) is implemented. The channel-to-channel clamp voltage has a big tolerance, and by paralleling channels the demagnetization energy may not be shared across all channels. The worst case is when only one channel clamp is activated. This causes all demagnetization energy to be dissipated in only one channel and that stress may damage it. For example, if the demagnetization energy per channel is 100 mJ, the paralleled channels demagnetization energy is 100 mJ as well. It is not the number of paralleled channels multiplied by 100 mJ.

If the inductive load demagnetization energy ($½LI^2$) is expected to be higher than the individual channel switch-off energy, TI recommends dissipating the demagnetization energy externally by adding an external clamp circuit.

For an external clamp, TI recommends using TVS and Shottky diodes between output paralleled channels and system ground. Equation 13 helps to choose the correct TVS diode based on the supply voltage and individual channel voltage clamp.

$$Vz(max) < Vclamp(min) – VS \quad (13)$$

where

- VS is the supply voltage
- Vclamp(min) is the individual channel voltage clamp lower limit
- Vz(max) is the TVS maximum clamp voltage

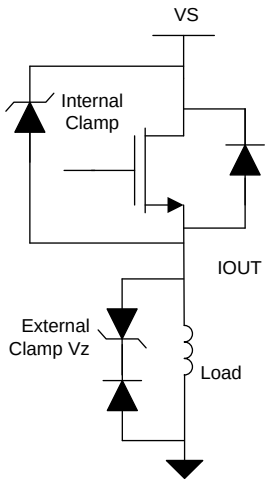


Figure 4. Inductive Load External Clamp

9 Thermal in Short-Circuit Conditions

Parallel channels by connecting all FET drains and sources together. The voltage across all FETs is the same. The current limit for individual channels cannot be the same due to process variation. Once one channel hits the current limit, the current is forced into other channels and they, in turn, enter the current limit one by one. For a short time, the short-circuit current flows entirely in the lowest impedance channel. This may cause a tremendous temperature rise in one channel. To avoid this issue, the load current should be externally limited to the single-channel maximum internal current limit. For example, in a 4-channel device where the single-channel internal current limit is 14 A, the total load current must be limited to 14 A.

10 Design Example Using TPS4H160

This section describes how to configure the 4-channel TPS4H160-Q1 device in parallel to increase load-current capacity.

10.1 Example Design Requirements

Table 3. Design Requirements

Supply Voltage, VS	13.5 V
Ambient temperature, T_A maximum	105°C
Total load current, IOUT	4 A

10.2 Circuit Design

The TPS4H160-Q1 device features a typical $R_{DS(on)}$ of 165 mΩ per channel at 25°C ambient and 280 mΩ at a junction temperature of 150ºC. The channel-to-channel deviation (ΔR) is ±10% due to process variation. As this design features a 4-channel high-side switch and the design requirements call for 4 A of total load current, each channel needs to drive a typical current-per-channel of 1 A. The TPS4H160-Q1 device is a good selection for this design because the junction-to-ambient thermal resistance, θ_{JA}, is 32.7ºC/W and the maximum on-resistance is 280 mΩ per channel at a junction temperature of 150ºC.

The maximum power dissipation at 4 A is $Pd = \frac{Ron}{4} \times IOUT^2 = \frac{0.28}{4}\,\Omega \times 4A^2 = 1.12\ W$.

The junction to ambient temperature increase is $\theta_{JA} \times P_d$ = 32.7°C/W × 1.12 W = 36.6°C.

The maximum junction temperature at 105°C ambient is $T_J = T_A + \theta_{JA} \times P_d$ = 105°C + 36.6°C = 141.6°C.

Next, calculate the minimum and maximum current per channel:

The maximum current per channel is $\frac{IOUT}{4}\left(1 + 2\left|\frac{\Delta R}{Ron(typ)}\right|\right) = \frac{4A}{4}(1 + 2 \times 0.1) = 1.2A$.

The minimum current per channel is $\frac{IOUT}{4}\left(1 - 2\left|\frac{\Delta R}{Ron(typ)}\right|\right) = \frac{4A}{4}(1 - 2 \times 0.1) = 0.8A$.

This means that after taking the tolerances on each individual channel, the load current can vary anywhere between 0.8 A and 1.2 A. This channel-to-channel current variation is still within the device specification in terms of current capability and junction temperature.

Equation 10 is then used to calculate the value of the external current-limiting resistor. The values for KcL, dKcL/KcL, V(cL) and Ron(typ) are found in the device-specific data sheet.

Table 4. Device Parameters

KcL	2500
dKcL/KcL	15%
V(cL)	0.8 V

Table 4. Device Parameters (continued)

Ron(typ)	165 mΩ
Ron maximum at T_J = 150ºC	280 mΩ
Maximum junction temperature T_J	150ºC
Junction-to-ambient temperature θ_{JA}	32.7ºC/W

The external current limit resistor, RcL, is calculated as Equation 14:

$$V(cL)\frac{K(cL)\left(1-\left|\frac{dK(cL)}{K(cL)}\right|\right)}{\frac{IOUT}{4}\left(1+2\left|\frac{\Delta R}{Ron(typ)}\right|\right)}=0.8\ V\ \frac{2500\left(1-0.15\right)}{\frac{4\ A}{4}\left(1+2\times0.1\right)}=1416.6\ \Omega \quad (14)$$

After paralleling all 4 channels, the effective minimum and maximum short-circuit current limits for the system must be calculated.

The short-circuit current upper limit is formula is shown in Equation 15:

$$4\frac{V(cL)}{R(cL)}\frac{K(cL)\left(1+\left|\frac{dK(cL)}{K(cL)}\right|\right)}{\left(1-2\left|\frac{\Delta R}{Ron(typ)}\right|\right)}=4\frac{0.8\ V}{1416.6\ \Omega}\frac{2500\left(1+0.15\right)}{\left(1-2\times0.1\right)}=8.12\ A \quad (15)$$

The short-circuit current lower limit is calculated by using Equation 16:

$$4\frac{V(cL)}{R(cL)}\frac{K(cL)\left(1-\left|\frac{dK(cL)}{K(cL)}\right|\right)}{\left(1+2\left|\frac{\Delta R}{Ron(typ)}\right|\right)}=4\frac{0.8\ V}{1416.6\ \Omega}\frac{2500\left(1-0.15\right)}{\left(1+2\times0.1\right)}=4.001\ A \quad (16)$$

Table 5 shows the summary of the calculated performance for this system. Table 6 shows actual measured performance.

Table 5. Design Target Parameters

Supply Voltage	External Limiting Resistor	Load Current	Current per Channel		Short-Circuit Current	
			MIN	MAX	MIN	MAX
13.5 V	1416.6 Ω	4 A	0.8 A	1.2 A	4.01 A	8.12 A

Table 6. Design Target Parameters

Supply Voltage	External Limiting Resistor	Load Current	Current per Channel		Short-Circuit Current
			MIN	MAX	
13.5 V	1.4 kΩ	4 A	0.951 A	1.01 A	5 A

NOTE: Consider equipment tolerances when taking measurements.

In Figure 5, scope probe 1 is the output voltage measuring 13 V. Scope current probe 2 is the highest individual current channel measuring 1.01 A. Scope current probe 3 is the lowest individual current channel measuring 0.951 A. Scope current probe 4, set to 5 A/V, is total load current measuring 4.03 A. Individual channel currents are within the design target.

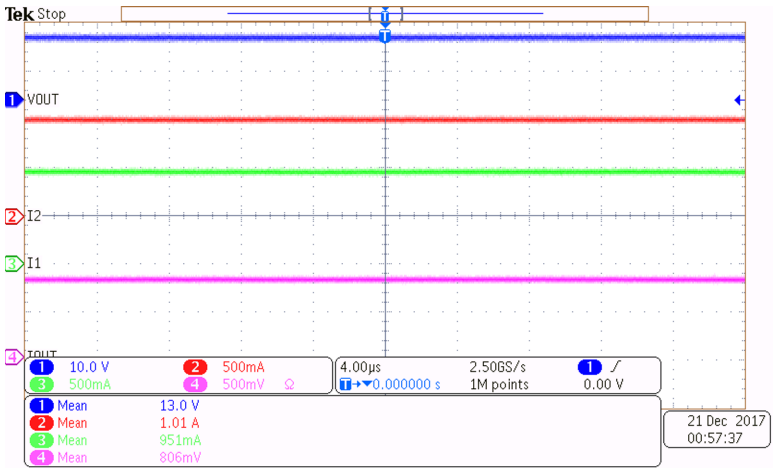
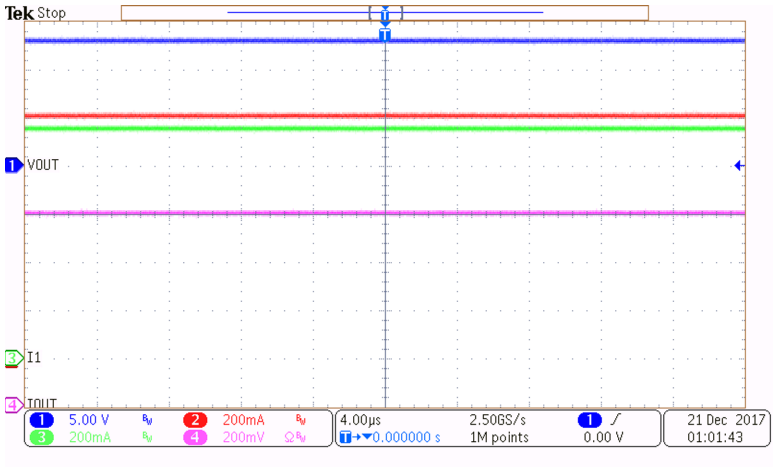


Figure 5. Scope of Output Voltage, Individual Load Currents, and Total Load Current

Figure 6 is the same as Figure 5. It is made more visual by expanding the voltage and current scales and also referencing the individual current to the same ground.



Expanded voltage and current scales and also referenced the individual current to the same ground.

Figure 6. Different View of Output Voltage, Individual Load Currents, and Total Load Current

Figure 7 shows the overload trip. The total load current limit is 5 A and it is as expected within the design target.

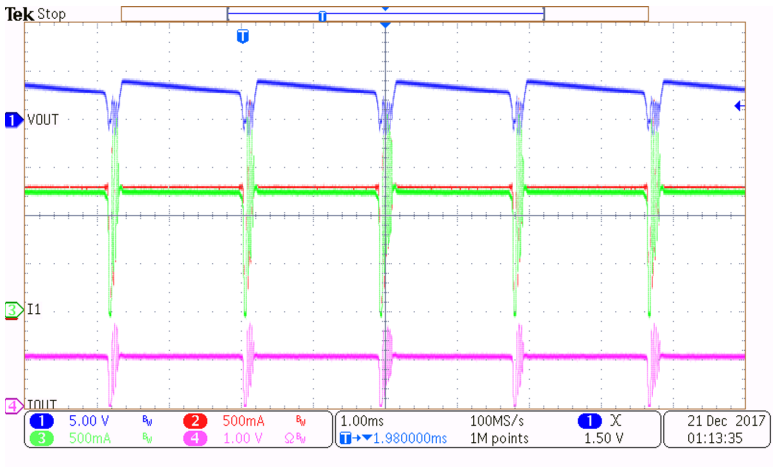


Figure 7. Design Example Overload Load Current Trip Point

11 Summary

Higher load current can be achieved by paralleling channels across multi-channel high-side power switch devices. For optimal design, parameter tolerances and device specification must be taken into consideration. Overall design parameters should be calculated following the provided equations in this document.

A.1 Four Paralleled Channels

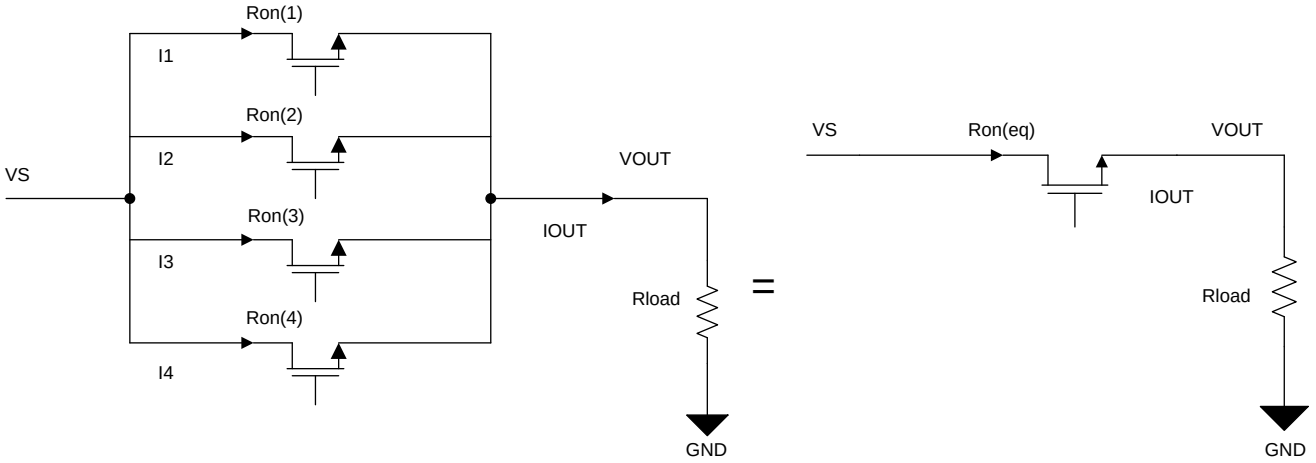


Figure 8. Using a High-Side Switch With 4 Channels in Parallel

Voltage difference across channels in parallel:

VS – VOUT = Ron(1) × I1
VS – VOUT = Ron(2) × I2
VS – VOUT = Ron(3) × I3
VS – VOUT = Ron(4) × I4
.
.
.
VS – VOUT = Ron(n) × In
VS – VOUT = Ron(eq) × IOUT

Equivalent on-resistance:

$$\frac{1}{Ron(eq)} = \frac{1}{Ron(1)} + \frac{1}{Ron(2)} + \frac{1}{Ron(3)} + \frac{1}{Ron(4)} \ldots + \frac{1}{Ron(n)} \quad (17)$$

Ron(1), Ron(2), Ron(3), and Ron(4) have a maximum variation of ΔR relative to the individual channel Ron(typ):

$$\frac{1}{Ron(eq)} = \frac{1}{Ron(typ) + \Delta R} + \frac{1}{Ron(typ) + \Delta R} + \frac{1}{Ron(typ) + \Delta R} + \frac{1}{Ron(typ) + \Delta R} \ldots + \frac{1}{Ron(typ) + \Delta R} \quad (18)$$

ΔR / Ron(typ) is the tolerance of the individual channel on-resistance relative to Ron(typ):

$$\frac{1}{Ron(eq)} = \frac{1}{Ron(typ)}\left(\frac{1}{1+\frac{\Delta R}{Ron(typ)}} + \frac{1}{1+\frac{\Delta R}{Ron(typ)}} + \frac{1}{1+\frac{\Delta R}{Ron(typ)}} \ldots + \frac{1}{1+\frac{\Delta R}{Ron(typ)}}\right) \tag{19}$$

Because ΔR / Ron(typ) is small relative to 1, the Taylor formula can be applied.

$$\frac{1}{1+\frac{\Delta R}{Ron(eq)}} = 1 - \frac{\Delta R}{Ron(typ)} \tag{20}$$

Equation 19 and Equation 20 are resolved as Equation 21:

$$\frac{1}{Ron(eq)} = \frac{1}{Ron(typ)}\left(n - n \times \frac{\Delta R}{Ron(typ)}\right) = \frac{4}{Ron(typ)}\left(1 - \frac{\Delta R}{Ron(typ)}\right) \tag{21}$$

The equivalent on-resistance in terms of individual channel typical on-resistance and variation is:

$$Ron(eq) = \frac{Ron(typ)}{n}\left(1+\frac{\Delta R}{Ron(typ)}\right) \tag{22}$$

Any individual channel current calculation:

$$I1 = \frac{Ron(eq)}{Ron(1)} \times IOUT = \frac{Ron(typ)}{n}\left(1+\frac{\Delta R}{Ron(typ)}\right) \times \frac{1}{Ron(typ) \times \left(1+\frac{\Delta R}{Ron(typ)}\right)} IOUT \tag{23}$$

$$I1 = \frac{Ron(eq)}{Ron(1)} \times IOUT = \frac{IOUT}{n}\left(1+\frac{\Delta R}{Ron(typ)}\right) \times \left(\frac{1}{\left(1+\frac{\Delta R}{Ron(typ)}\right)}\right) \tag{24}$$

The individual current channel in terms of load current, typical on-resistance and its variation is:

$$I1 = \frac{IOUT}{n}\left(1+2\frac{\Delta R}{Ron(typ)}\right) \tag{25}$$

A.2 Four Paralleled Channels

The individual current channel is: $I1 = \frac{IOUT}{4}\left(1+2\frac{\Delta R}{Ron(typ)}\right)$

A.3 Three Paralleled Channels

The individual current channel is: $I1 = \frac{IOUT}{3}\left(1+2\frac{\Delta R}{Ron(typ)}\right)$

A.4 Two Paralleled Channels

The individual current channel is: $I1 = \frac{IOUT}{2}\left(1+2\frac{\Delta R}{Ron(typ)}\right)$

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