External or internal FETs for motor drive in automotive applications

Automotive Systems

ABSTRACT

Modern automobiles use electric motors to drive an increasing number of applications, such as power windows, locks, seats, mirror adjustments, blowers, and trunk lifts. Transistor-based solid-state drive circuits are used to switch the current to the motors used in these applications. Designers can choose motor drive integrated circuits (IC) with either external field-effect transistors (FETs) or internal FETs for the final drive stage. This document discusses some of the tradeoffs in choosing the external-FET or internal-FET approach. Additionally, this application report focuses on key comparisons in terms of board size and thermal performance.

Contents

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1 Introduction

In today's automotive industry, many electric motors are added to cars due to the benefits of automation, enhanced safety, and luxury features. Motors are found in applications such as electric power steering, brakes, engine and transmission, power seats, windows, doors and trunks. Figure 1 shows an overview of some of the areas where electric motors are used in a car.
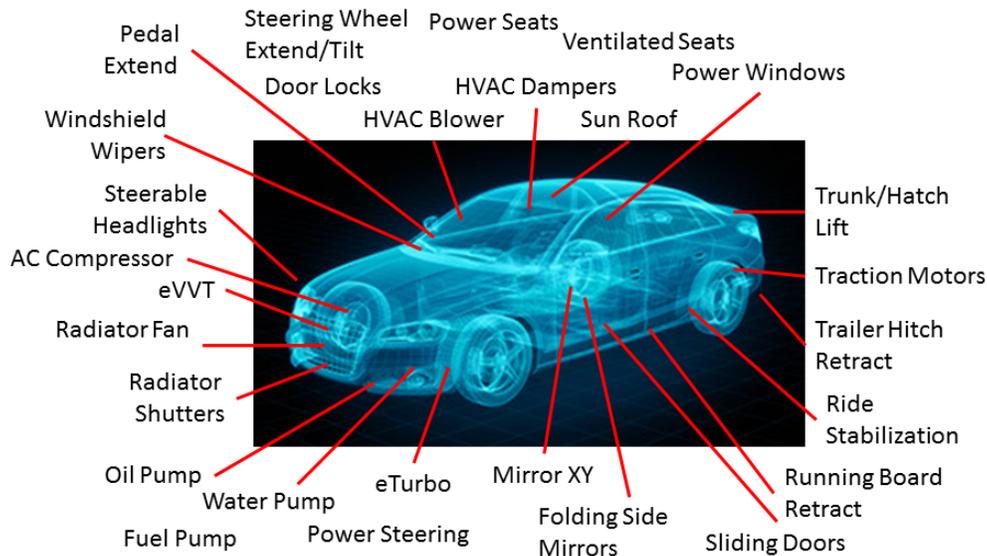
Figure 1. Automotive Electric Motor Application Examples

These electric motors can be brushed DC, brushless DC, or stepper motors. This document focuses on brushed DC (BDC) motors because they are the most common. But most of the tradeoffs involving internal or external design also apply to driving brushless DC motors or stepper motors.

The circuit arrangement for a brushed DC motor driver typically consists of a drive stage made up of two high-side switches and two low-side switches, all of which are controlled by logic. In general the two high-side switches and two low-side switches are implemented as n-channel field-effect transistors (FETs). N-channel FETs are more common than p-channel FETs due to the higher effective current density which, in turn, is due to the higher mobility of electrons (n-channel charge carriers) compared to holes (p-channel charge carriers). This arrangement is typically called a full-bridge motor driver, or sometimes an H-bridge motor driver, due to the shape typically drawn of the electrical schematic.

The full-bridge motor driver is typically implemented using one of the following three topologies:

1. **Gate Driver external-FET topology:** In this topology, the drive FETs and the FET controller are in different IC packages. Figure 2 shows an implementation of the motor driver circuit with a controller chip that includes gate driver, charge pump, control circuits, diagnostics and current sense, along with four external FETs; that is, the FETs are not in the same IC package as the controller chip. This arrangement allows the designer to select the controller and the FETs independently, which gives flexibility to optimize the motor driver design.

2. **Multi-chip Module Internal-FET Topology:** In this topology, the drive FETs and the FET controller are in different semiconductor chips, but are encapsulated in the same package in the form of a multi-chip module (MCM) as Figure 3 shows. In some MCM implementations, some (but not all) of the final drive-stage FET chips are in the same chip as the controller chip.

3. **Monolithic Internal-FET Topology:** In this topology, the drive FETs and the FET controller are in the same IC package. Moreover, all of the drive FETs and the FET controller are in same semiconductor chip; that is, it is a monolithic chip as Figure 4 shows. This topology is typically used for low motor current applications.

The discussion in this document focuses on the *Gate Driver External-FET topology* or *Multi-chip Module Internal-FET Topology* choice.

Topology	Comment
Figure 2. Gate Driver External-FET Topology	Drive FET chips and FET controller chip are in different IC packages
Figure 3. Multi-Chip Module Internal-FET Topology	Drive FET chips and the FET controller chip are in the same IC package. However, there are multiple chips.
Figure 4. Monolithic Internal-FET Topology	Drive FETs and the FET controller are in the same IC package and the same chip.
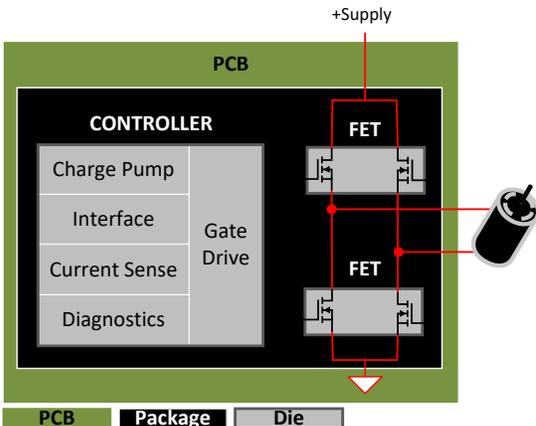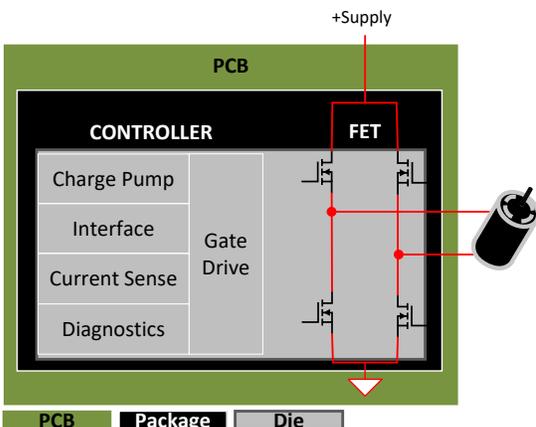
2 Flexibility and Simplicity

In general, there is a tradeoff between the design flexibility of using external FETs and the design simplicity of an internal-FET approach. Which choice is better depends on the requirements of the application as well as the priorities of the circuit designer.

2.1 External-FET Topology Offers Flexibility

External FETs give a designer the flexibility to use one circuit design for a variety of different applications, simply by allowing designers to choose drive FETs which best suit the requirements of the application. FETs with larger geometry tend to have lower on-resistance, or $R_{DS(on)}$, for a given gate voltage. Lower $R_{DS(on)}$ reduces the losses due to the motor current causing voltage drop across the drive FETs. This leads to power dissipation in each FET, which is given by the product of the square of the FET current and the FET $R_{DS(on)}$. Note that the maximum current rating of a FET is closely related to $R_{DS(on)}$ of the FET and the thermal properties of the package.

One possible drawback of choosing larger size FET packages is the overall printed-circuit board (PCB) size. Perhaps counter-intuitively, Section 3 shows that external-FET implementations are similar in size to internal-FET devices with comparable performance. Designers should consider both the current rating and the thermal specification for the FET package; this tradeoff is discussed more in Section 4.

2.2 Internal-FET Topology Offers Simplicity

A motor driver with internal FETs can simplify the design process by providing an all-in-one solution. Texas Instruments offers several motor drivers with internal FETs, with peak drive current capabilities ranging from 1 Amp to 10 Amps. These devices minimize the design effort needed for getting started with a motor drive application, as the internal transistor characteristics are already selected to match the requirements of the specified motor current.

With the drive FETs in the same IC package as the controller, complete testing of the whole drive circuit during production assures the device will perform as expected. Having the FETs in the same package as the drive logic also simplifies monitoring the temperature of the FETs for diagnostic purposes. Additionally, the internal-FET approach simplifies the bill of materials and layout of the circuit board. Especially for applications with relatively low motor current, motor drivers with internal FETs can be an attractive solution.

3 Board Area Comparisons

In many cases the physical size of the PCB is constrained. When board size is limited, internal-FET drivers may seem to have an inherent advantage due to the reduced number of semiconductor packages. However, the actual size of the external-FET and internal-FET topologies depends on several variables; in the following sections we compare board area for the *Gate Driver External-FET Topology* solution in Figure 2 and the *Multi-chip Module internal-FET Topology* solution in Figure 3.

3.1 Board Area Considerations

When comparing the board area for various implementations, there are several factors to consider. These include:
- Maximum motor current - this is related to $R_{DS(on)}$
- Maximum motor voltage
- Uni-directional or bidirectional motion - we focus on bidirectional solutions, recognizing that uni-directional motion solutions will be a subset of the full-bridge implementation
- Method of current sensing
- Diagnostic and protection features
- Number of external components needed
- Component spacing rules for manufacturing

In addition to the FET and the controller chips, several external components are typically required to implement a complete motor drive solution. These external components may include:

- Decoupling capacitors to stabilize the power supply for the motor driver control circuits
- Bulk capacitors to stabilize the power supply for the internal drive FETs during motor transients
- Resistor to scale the motor current sense signal to a desired voltage range
- Resistor and capacitor to filter the motor current sense signal
- FET, diodes, and resistors to provide reverse battery voltage protection
- Resistors on each signal line to the microcontroller
- Transient voltage suppressor for load dump transients

3.2   Board Area for External-FET Topology

Since the drive FETs can be selected independent of the controller, there are many options to consider when determining the size of the motor driver solution with external FETs. FET packages are available in a variety of sizes and configurations. This document discusses the trends in package size versus $R_{DS(on)}$ for both single-FET implementations and dual-FET implementations of a full-bridge drive circuit.

In addition to the drive FETs forming the full-bridge, the external-FET implementation includes a controller chip, which typically integrates the necessary gate driver circuits, charge pumps, diagnostic features, and in many cases current sense amplifiers.

For the *Gate Driver external-FET topology* in Figure 2, one implementation is to use four single external FETs for the full-bridge. Figure 5 shows a scatter plot of the data for several FETs, with the board area for four single FETs plotted on the vertical axis, versus the $R_{DS(on)}$ for one high-side and one low-side FET plotted on the horizontal axis. The horizontal scale is logarithmic, to better show the wide range of $R_{DS(on)}$ values available with external FETs. To remove the effect of other factors on these data points, all of the transistors represented are single n-channel silicon FETs with automotive ratings, and they all have a maximum V_{DS} rating of 60 V.
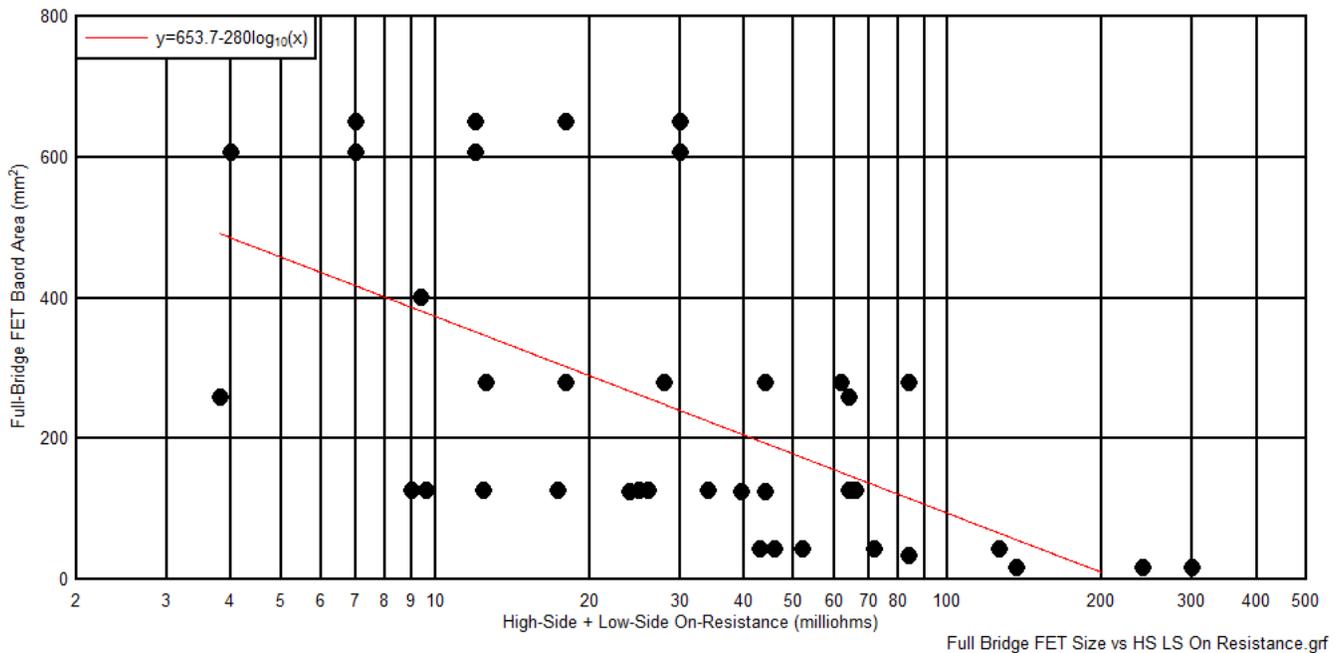

Figure 5. Full-Bridge Board Area vs High-Side + Low-Side $R_{DS(on)}$, Single External FETs

Although a wide variety of options available exist, the general trend is that if only a small board area is available, the active $R_{DS(on)}$ will be towards the higher values. Conversely, if a high-current application requires very low $R_{DS(on)}$, the board size will not be as small as lower-current (higher $R_{DS(on)}$) cases. Single FETs are also available in packages such as the TO-220, which offer additional flexibility in layout. The TO-220 can be mounted with the large dimension vertically, so that only the board area used for the three pins is needed. This also provides another dimension for mounting a heat sink, if needed.

Another option to consider when board space is limited, is to use dual-FET devices, which combine two FETs in a single package. This can reduce the board size needed for a motor driver without restricting the available options to only the limited number of motor drivers with internal FETs. Although there are fewer choices for dual-FET package size, Figure 6 shows the same general trend of increasing board size as the $R_{DS(on)}$ specification decreases.
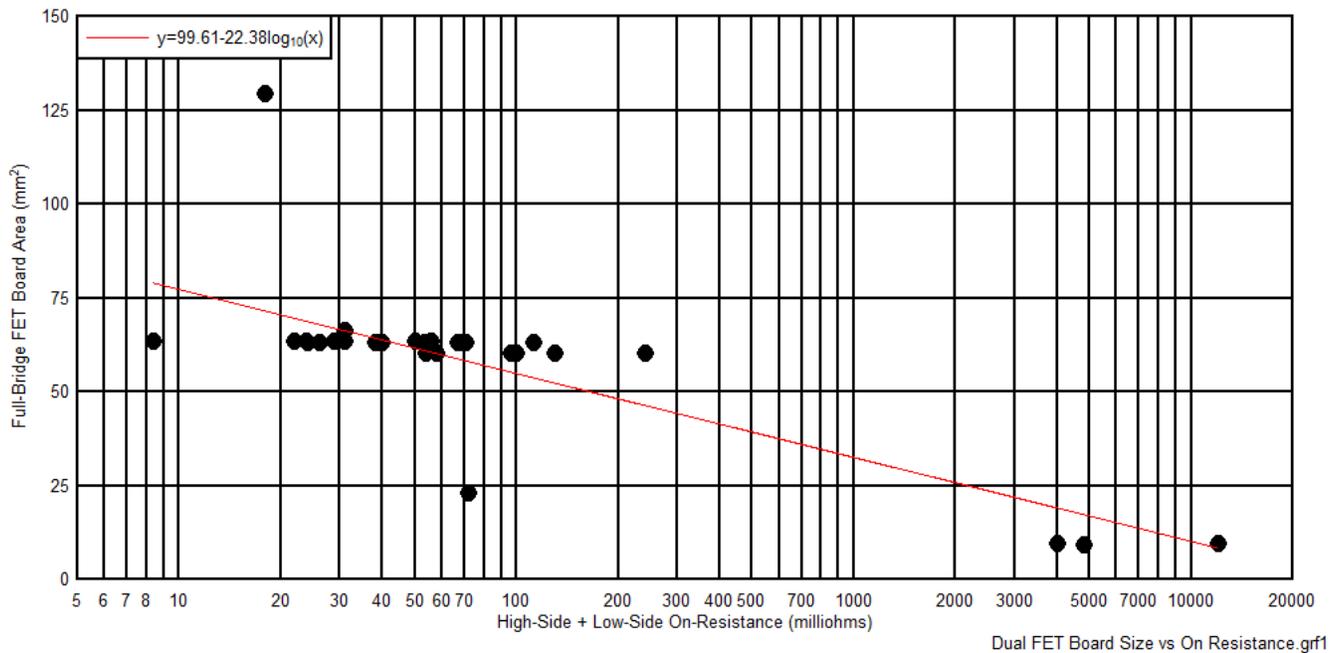

Figure 6. Full-Bridge Board Area vs High-Side + Low-Side $R_{DS(on)}$, Dual External FETs

3.3 Board Area for Internal-FET Topology

Figure 7 illustrates the data for internal-FET topologies. This figure includes both the multi-chip module and monolithic topologies and shows that the package size for full-bridge devices must increase significantly to provide $R_{DS(on)}$ reduction. This is primarily due to the larger semiconductor chip size needed to provide low $R_{DS(on)}$.


Figure 7 equation label: $y = 349 - 4.359x + 0.01791x^2$
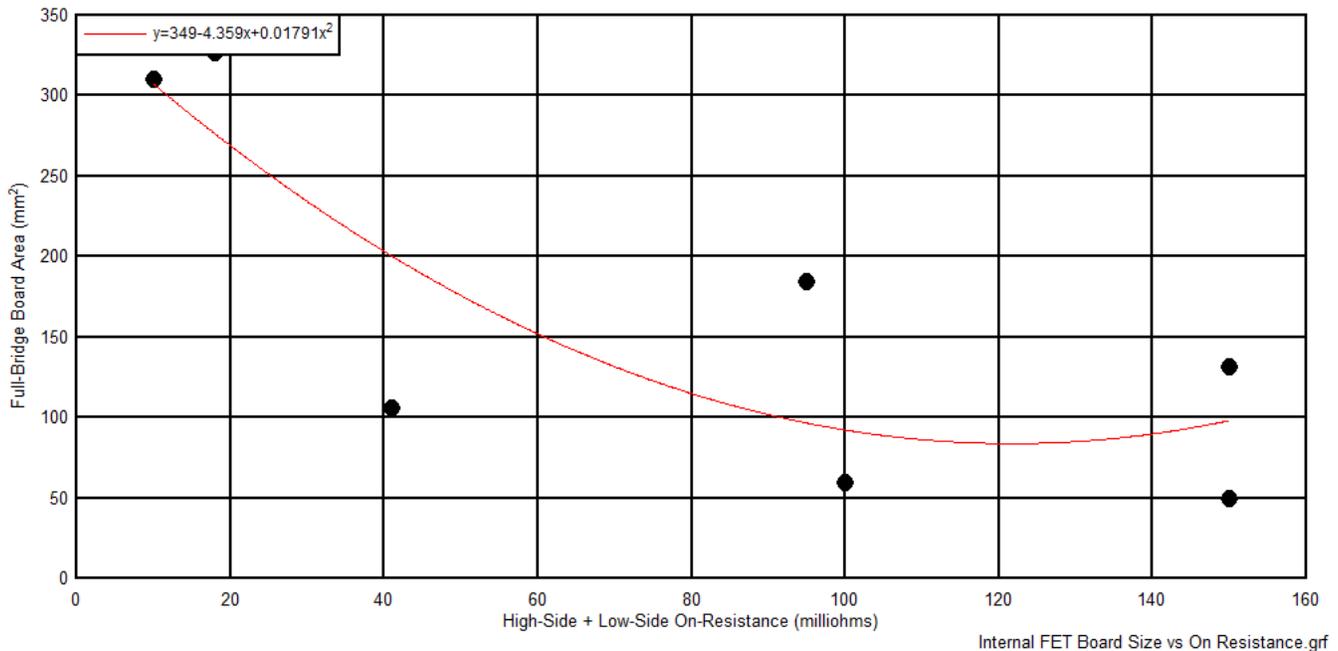
Figure 7. Full-Bridge Board Area vs High-Side + Low-Side $R_{DS(on)}$, Internal-FET Devices

Table 1 summarizes the data used to generate Figure 7. It is noted that Table 1 lists some of the automotive motor drive solutions with internal drive FETs which are available from Texas Instruments and other semiconductor manufacturers. The selection is limited to devices with voltage ratings of 40 V, consistent with automotive battery supply systems due to the typical load-dump voltage requirement. The dimensions are for this motor driver component only, not including any necessary ancillary components. The listed $R_{DS(on)}$ values used for this comparison are for a path through the driver, including one high-side FET and one low-side FET.

Table 1. Package Sizes for Examples of Motor Drivers With Internal FETs

Example	Package	Dimensions (including pins)	Board Area (mm²)	$R_{DS(on)}$ per H+L pair	Voltage Rating
1	24-pin Thin Small Outline	7.8 mm × 6.4 mm	49.9	150 mΩ (typical) 310 mΩ maximum	40 V absolute maximum
2	16-pin Small Outline	9.9 mm × 6 mm	59.4	100 mΩ (typical) 200 mΩ maximum	38 V absolute maximum, 40 V with external clamp
3	36-pin Small Outline Power	10.3 mm x 10.3 mm	106.1	41 mΩ (typical) 80 mΩ maximum	38 V absolute maximum, 40 V with external clamp
4	36-pin	12.8 mm x 10.3 mm	131.8	150 mΩ (typical) 295 mΩ maximum	45 V absolute maximum
5	28-pin Small Outline	17.9 mm x 10.3 mm	184.4	95 mΩ (typical) 190 mΩ maximum	41 V absolute maximum
6	7-pin Transistor Outline (two required)	10 mm x 15 mm (two required)	310	10 mΩ (typical) 28.7 mΩ maximum	40 V absolute maximum
7	30-pin Small Outline	17.2 mm x 19 mm	327	18 mΩ (typical) 38 mΩ maximum	41 V absolute maximum

3.4 *Summary of Board Area Comparison*

Figure 8 and Figure 9 compare *Gate Driver external-FET topology* and *Multi-chip Module internal-FET Topology* motor driver solutions. The external-FET implementation is documented in TI Design TIDA-020008 and uses the DRV8703-Q1 gate driver with two external dual-FET devices. The internal-FET implementation uses a multi-chip module device available from another manufacturer; it is listed in Table 1 as Example device 3.
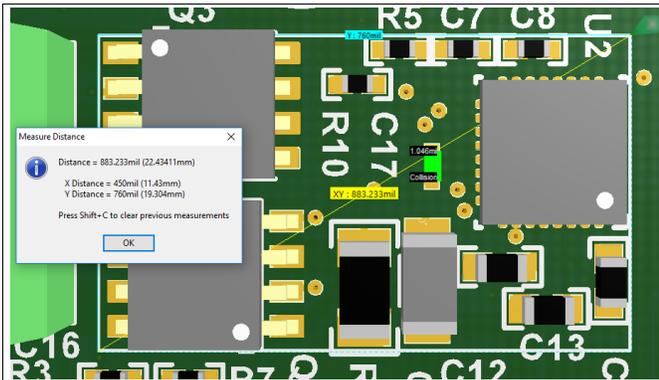
Figure 8. High Current Gate Driver External-FET Example
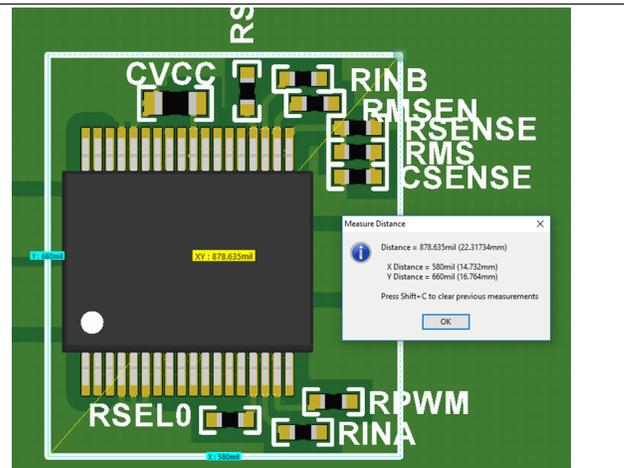
**Figure 9. High Current Multi-Chip Module Internal-FET Example**

Figure 8 shows a full-bridge motor driver with a gate driver and external FETs, with the accompanying passive components. In this external-FET example, the rectangle dimensions are 11.4 mm × 19.3 mm, an area of 220 mm^2. The external FETs can be selected with low $R_{DS(on)}$, thus reducing the power dissipation and allowing high drive currents. For the dual-FET packages shown, automotive-grade FETs are available with maximum combined resistance of 23 mΩ and a junction-to-ambient thermal resistance of 95°C/W for each dual-FET package. Because there are two packages to distribute the power dissipation, the effective junction-to-ambient thermal resistance is halved. The maximum junction temperature is 175°C, so the maximum power dissipation is 1.9 W, and a maximum steady-state current of 9.1 A.

Figure 9 shows an internal-FET MCM example with accompanying passive components in the white rectangle. The rectangle dimensions are 16.8 mm × 14.7 mm, an area of 247 mm^2. This particular motor driver is promoted by the manufacturer as being capable of 35 A of output current. However, when the thermal properties of the design are considered, the actual steady-state motor current is considerably less than 10 A. The internal FETs of this example device have a typical combined high-side and low-side $R_{DS(on)}$ of 41 mΩ, with a maximum combined resistance specification of 80 mΩ. The junction-to-ambient thermal resistance can be used for a coarse estimate of the thermal properties, and this parameter is in the range of 45°C/W for this device. Assuming a maximum ambient temperature of 85°C, and a maximum junction temperature of 150°C, the maximum power dissipation is 1.44 W. For a combined $R_{DS(on)}$ of 80 mΩ, the power equation gives a maximum steady-state current of 4.2 A.

In Table 2 the results are presented in tabular form. The gate driver external-FET topology is slightly more compact than the multi-chip module internal-FET Topology. The thermal characteristics of these solutions are compared in Section 4.

Table 2. Board Size Comparison Results

Figure	Solution	Board Size (mm × mm)	Board Area (mm^2)
Figure 8	Gate Driver external-FET topology	11.4 × 19.3	220
Figure 9	Multi-Chip Module internal-FET Topology	14.7 × 16.7	247

In summary, the Gate Driver external-FET topology can be equivalent in PCB area as the Multi-Chip Module internal-FET topology. In addition, the external-FET topology may have significantly higher steady-state current capability if external FETs with low R$_{DS(on)}$ are selected.

NOTE: Many automotive applications require relatively high peak and continuous motor currents; examples include windshield wipers, power windows, and power sliding doors. For these high-current applications, the R$_{DS(on)}$ of the drive FETs is significantly low. When driving motors with maximum currents greater than 10 A, the size of the FETs becomes a dominant part of the integrated device size. Many automotive applications have motor currents up to 30 A, or more. Some manufacturers do offer multi-chip module motor drivers with internal FETs promoted for these high-current applications; the package size of these devices can be quite large. The key characteristics which cause the package size to increase are the R$_{DS(on)}$ and voltage ratings of the FETs. The FET size increases as the R$_{DS(on)}$ decreases, and similarly the size increases as the voltage rating increases.

Designers may assume that motor driver solutions using internal drive FETs provide a smaller overall size, but in some cases, especially for high-current applications, the layout area may be very similar. Designers should also carefully compare the specifications of the components to ensure the two options are truly equivalent.

NOTE: For motor drive applications with relatively low current demands, drive stage transistors with low R$_{DS(on)}$ values are not needed, and therefore, the FET size can be relatively small. For example, some motors may have a motor winding resistance in the range of a few Ohms, with a stall current of 10 A or less, and a normal operating current less than 5 A. This size motor is used for automotive applications such as power head rests, power sun shades, or side-mirror folding. A monolithic motor driver with integrated FETs, such as the DRV8873-Q1 device, is a good fit for this type of application. It includes FETs with R$_{DS(on)}$ of 150 mΩ for the high-side plus low-side transistors, which are active when driving the motor in either direction. Figure 10 shows the size of this device is about 50 mm^2. This device has a very compact package, and is represented by the data point in the lower right corner of Figure 7.

Compared to the integrated FET solution for low-current applications, it is difficult to implement an equivalent solution with external FETs in the same compact size. Referring to Figure 6, even using dual FET devices, most of the available devices with comparable on-resistance (less than 200 mΩ) use a 5 mm × 6 mm package as Figure 11 shows, so the board area for the FETs alone (2 dual FET packages) are over 60 mm^2. The complete solution also requires a gate driver and current sense resistor plus amplifiers, all of which are integrated into the DRV8873-Q1, along with advanced diagnostics and fault tolerant features.

Thus for low-current applications, devices with integrated FETs can provide a benefit in terms of reduced board space requirements.

Figure 10. Package Size of Fully-Integrated Monolithic Motor Driver for 10-A Peak Current

Figure 11. Package Size of Dual-FET Capable of 10-A Peak Current
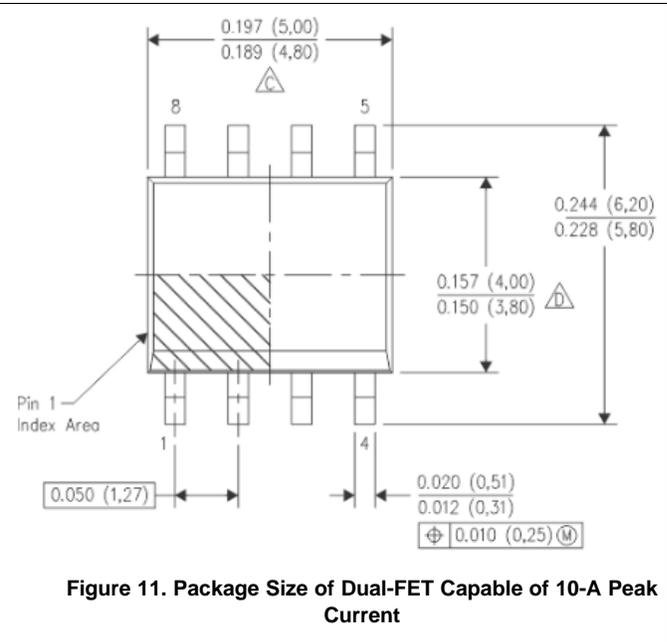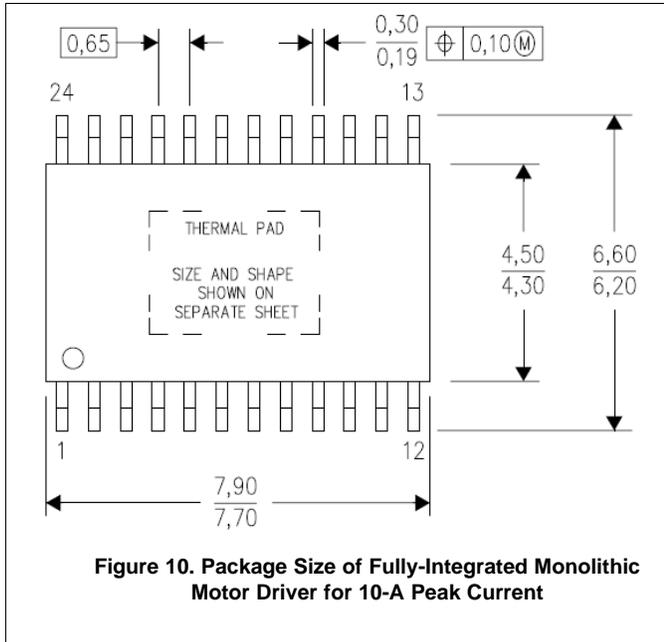
4 Thermal Comparisons

For the relatively low motor current, thermal considerations are typically not as critical as those for higher power applications. Therefore, this discussion focuses on thermal comparisons for the higher current applications. Specifically, the thermal performance of *Gate Driver external-FET topology* and *Multi-chip Module internal-FET Topology* is examined.

4.1 Thermal Considerations

For high-power applications, the dissipation of internal heat becomes a significant consideration. When driving a high-current load, the power dissipation of the controller chip is negligible compared to the power dissipation of the final drive stage FETs. The power dissipated in the drive FETs depends on the motor current and the resistance of the FET channel from drain to source ($R_{DS(on)}$). For a typical full-bridge drive circuit, the FET power dissipation is calculated as:

$$\text{Power} = I^2_{MOTOR} \times (R_{DS(on)\text{High-Side FET}} + R_{DS(on)\text{Low-Side FET}}) \tag{1}$$

when a high-side FET and a low-side FET are used to drive the motor current. Further discussion of power dissipation calculations is given in the *Calculating motor driver power dissipation* application report.

The path for heat dissipation from the active circuits to the external environment depends on the implementation of the motor driver as well as the board design. Table 3 shows the thermal paths for different example implementations. Figure 12, , Figure 13 and Figure 14 show the thermal paths for *Gate Driver external-FET topology*, *Multi-chip Module internal-FET Topology*, and *Monolithic internal-FET Topology* respectively.

Table 3. Heat Flow Paths
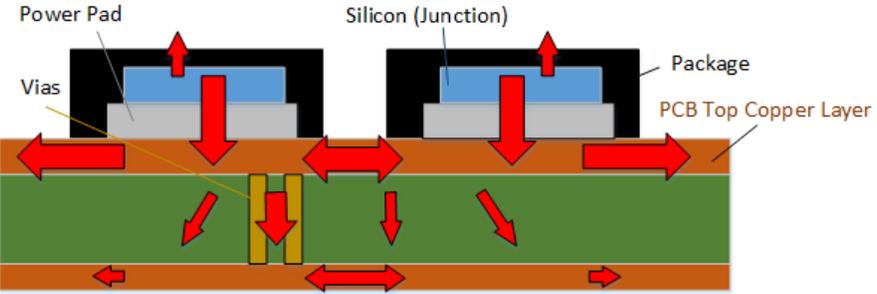
Topology	Comment
Figure 12. Heat Flow for Gate Driver External-FET Topology	The separate FET packages will have thermal paths through their respective power pads to the PCB.
Figure 13. Heat Flow for Multi-Chip Module Internal-FET Topology	There can be additional heat flow between the chips inside the package.
Figure 14. Heat Flow for Monolithic Internal-FET Topology	For a monolithic device, the primary thermal flow paths are from the active device through the power pad to the top layer copper.
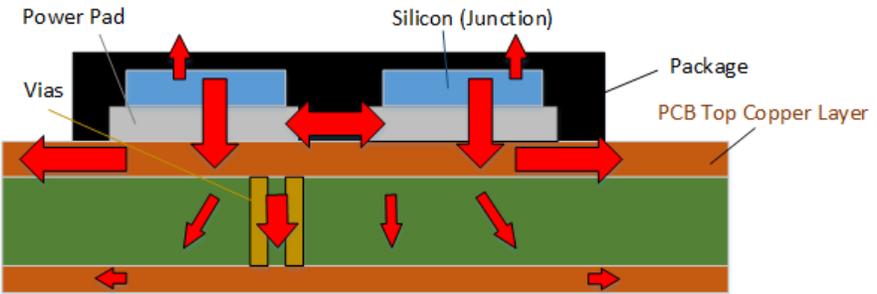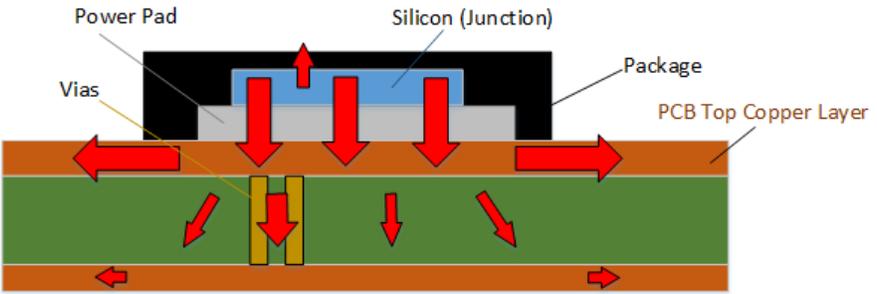
In all three cases, there is a full-bridge motor driver with either internal FETs or external FETs. During motor operation, one of the high-side FETs and one of the low-side FETs will be simultaneously turned on to provide a path for the motor current. The other FETs, making up the complementary path through the full-bridge, are off. The controller chip typically contributes little to the overall power dissipation. When the drive FETs are small, sized for lower motor currents, the inclusion of the package area for the controller chip can provide a significant thermal benefit in terms of a lower thermal resistance. When, the drive FETs are large compared to the controller chip, the inclusion of the package area for the controller chip is much less significant.

Thus, the package that includes the controller chip and drive FETs can be more of an advantage for relatively low motor currents than for high-current applications. TI takes this approach with integrated FET motor driver devices such as the DRV8873-Q1 for peak drive currents up to 10 A, and with gate driver devices such as the DRV8703-Q1 for peak currents above 10 A.

For motor driver designs in automotive applications, the thermal constraints will often be the limiting factor in designing compact, high-current solutions. Table 4 gives thermal parameters for several of the typical package products and package types used for automotive motor drivers.

In general, the larger the package, the lower the thermal resistance, thereby allowing better conduction of heat generated in the device into the circuit board. For multi-chip modules such as are common with internal-FET drivers, the thermal analysis becomes quite complex with various thermal paths between the chips as well as from each chip to the board. The specified junction-to-ambient thermal resistance is only a coarse indicator of the thermal performance that will occur for any specific design, but it is useful for comparison of the various packages available for motor drivers.

Table 4. Package Thermal Parameters

Example	Package	Dimensions (mm)	Theta JA (°C/W)	Theta JC (°C/W)
1	24-pin thin small outline	7.8 × 6.4	27.8	18.8 (top) 1.0 (bottom)
2	16-pin small outline	9.9 × 6	40.7 (high-side) 55.4 (low-side)	$R_{thj-pin}$: 32 (high-side) 45 (low-side)
3	Power SSO-36 TP	10.3 × 10.3	45 ± 25	4 to 4.3
4	36-pin small outline	12.8 × 10.3	46	29
5	28-pin small outline	17.9 × 10.3	35 to 55 (each chip)	20 (high-side) 20 (low-side)
6	7-pin transistor outline (two required)	10 × 15 (two required)	19 per device	0.55 (high-side) 1.1 (low side)
7	Power SO-30	17.2 × 19	15 to 22[(1)]	1.7 (high-side) 3.2 (low-side)
Dual n-channel FET	LFPAK56D (SOT1205)	5 × 6	95 (per package)	3.96

[(1)]   2 half-bridge FETs in parallel, each with Theta JA of 30 to 45°C/W

Another good source of information is found in the TI Training web site; for example, see *Power loss and thermal considerations for gate drivers*.

4.2   *Thermal Estimates for Gate Driver External-FET Topology*

To directly compare the thermal performance of internal and *Gate Driver external-FET* solutions, the board size, layer count, and load current can be made the same for both solutions. In Figure 15 and Figure 16 the two solutions are implemented on a two-layer board with the same overall size. In both figures, the active circuit is driving a 4-Ω resistive load with a supply voltage of 12 V, giving a steady-state load current of 3 A. The background temperature in both cases is ambient room temperature, about 22°C.

4.2.1   Steady-State 3-A Load Current

With a 3-A load current and typical $R_{DS(on)}$ of 21.25 mΩ for BUK7K25-40E dual FETs, this gives an internal power dissipation of about 190 mW in each dual-FET package, or about 380 mW total. Using the Theta JA for the dual-FET package listed in Table 4, the junction-to-ambient temperature delta for each FET package can be estimated as:

$$\Delta T_{\theta JA} = 95°C/W \times 0.19\ W = 18.05°C \tag{2}$$

For the ambient temperature of 22°C, this gives an estimated junction temperature of 40°C.

Then, using the Theta JC for the dual-FET package, the junction-to-case temperature delta can be estimated as:

$$\Delta T_{JC} = 3.96°C/W \times 0.19\ W = 0.75°C \tag{3}$$

which gives an estimated case temperature of about 39°C.

4.2.2 Steady-State 6-A Load Current

With a 6-A load current and typical $R_{DS(on)}$ of 21.25 mΩ, this gives an internal power dissipation of about 765 mW in each dual-FET package, or about 1.53 W total. Using the Theta JA for the dual-FET package listed in Table 4, the junction-to-ambient temperature difference for each FET package can be estimated as:

$$\Delta T_{JA} = 95°C/W \times 0.765\ W = 73°C \tag{4}$$

Then using the Theta JC for the dual-FET package, the junction-to-case temperature delta can be estimated as:

$$\Delta T_{JC} = 3.96°C/W \times 0.765\ W = 3°C \tag{5}$$

which gives an estimated ambient-to-case temperature rise of about 70°C.

4.3 Thermal Estimates for Multi-Chip Module Internal-FET Topology

4.3.1 Steady-State 3-A Load Current

With a 3-A load current, for a *Multi-Chip Module internal-FET* device with combined high-side plus low-side typical $R_{DS(on)}$ of 41 mΩ, the internal power dissipation of about 370 mW.

Using the Theta JA for the integrated FET MCM example 3 package, the junction-to-ambient temperature delta can be estimated as:

$$\Delta T_{JA} = 45°C/W \times 0.37\ W = 16.65°C \tag{6}$$

Then, using the Theta JC for the device, the junction-to-case temperature delta can be estimated as:

$$\Delta T_{JC} = 4.15°C/W \times 0.37\ W = 1.5°C \tag{7}$$

which gives an estimated ambient-to-case temperature rise of about 15°C.

4.3.2 Steady-State 6-A Current

With a 6-A load current , for a *Multi-Chip Module internal-FET* device with combined high-side plus low-side typical $R_{DS(on)}$ of 41 mΩ, the internal power dissipation is about 1.48 W. Following the same previous calculations, this gives an estimated ambient-to-case temperature rise of about 60°C. The maximum case temperature is identified in the image as 77.7°C, about 55°C above the ambient temperature.

4.4 Summary of Thermal Comparisons

Figure 15 and Figure 16 show the thermal comparison for a 3-A load current between the *Gate Driver external-FET topology* solution and the *Multi-Chip Module internal-FET Topology*. Note that the measurements are in agreement with the theoretical estimates calculated in Section 4.2 and Section 4.3.
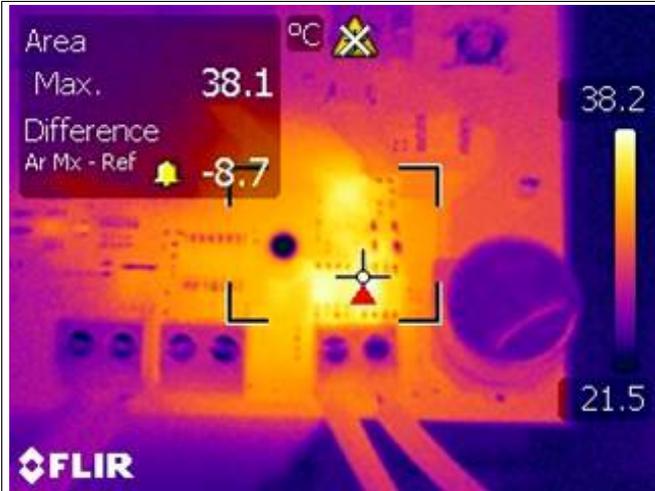
Figure 15. Gate Driver External-FET Topology With Steady-State 3-A Load

Figure 16. Multi-Chip Module Internal-FET Topology With Steady-State 3-A Load

Figure 17 and Figure 18 show the thermal comparison for a 6-A load current between *Gate Driver external-FET topology* solution and *Multi-Chip Module internal-FET Topology*. Note once again that the measurements are in agreement with the theoretical estimates calculated in Section 4.2 and Section 4.3.
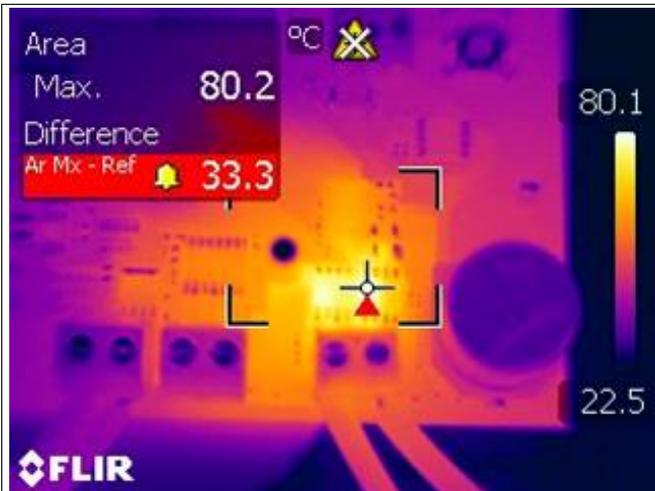
Figure 17. Gate Driver External-FET Topology With Steady-State 6-A Load

Figure 18. Multi-Chip Module Internal-FET Topology With Steady-State 6-A Load

In Table 5 measurement results are presented in tabular form. Specifically, the column with the heading "Maximum Measured Temperature (°C)" show the maximum measured temperature on the board.

Table 5. Thermal Comparison Results

Figure	Solution	Board Area (mm²)	Test Load Power (W)	Ambient Temperature (°C)	Maximum Measured Temperature (°C)	Ambient-to-Case Temperature Rise (°C)
Figure 15	Gate driver and external FET with 42-mΩ FETs	220	36	21.5	38.1	16.6
Figure 16	Small 41-mΩ multi-chip module internal-FET device	247	36	21.7	36.0	14.3
Figure 17	Gate driver and external FET with 42-mΩ FETs	220	72	22.5	80.2	57.7
Figure 18	Small 41 mΩ multi-chip module internal-FET device	247	72	22.5	77.7	55.2

In summary, the external FET solution is slightly more compact than the multi-chip module internal-FET solution, and has similar thermal characteristics when using FETs with equivalent $R_{DS(on)}$. The external-FET solution can have significantly better thermal performance due to the availability of lower $R_{DS(on)}$ of the external FETs.

> **NOTE:** One additional factor when comparing internal-FET solutions to external-FET solutions is the maximum allowable junction temperature for the devices. The maximum allowable junction temperature for the internal-FET devices is 150°C, while the maximum allowable junction temperature for the automotive-qualified external dual-FETs is 175°C, which gives an additional 25°C of rated temperature margin.

5 Summary

Motor drive solutions using the internal-FET MCM topology simplify the design in terms of component selection, layout, and bill of materials. For applications with motor currents less than 10 A, integrated FET motor drivers may also provide size advantages.

Motor drive solutions using the gate driver and external-FET topology offer more flexibility in optimizing the FET parameters to the particular application. For motor currents greater than 10 A, external FETs may provide thermal design benefits in terms of spreading the power dissipation into separate packages.

6 References

1. Texas Instruments, *MOSFET slew rate control training*
2. Texas Instruments, *Fundamentals of MOSFET and IGBT gate driver circuits application report*
3. Texas Instruments, *Calculating motor driver power dissipation application report*
4. Texas Instruments, *Reducing EMI radiated emissions with TI smart gate drive tech note*
5. Texas Instruments, *Understanding motor driver current ratings application report*
6. Texas Instruments, *Semiconductor and IC package thermal metrics application report*
7. Texas Instruments, *Load switch thermal considerations application report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2019) to A Revision   **Page**

- Changed 4-mΩ to 42-mΩ in third row of *Solution* column in the *Thermal Comparison Results* table. ....

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