Application Report
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How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors

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ABSTRACT

Multi-layer ceramic (MLCC), aluminum electrolytic, tantalum, and polymer are the capacitor types most widely used in DC/DC switching regulator circuits. In practical applications, a power designer can use a hybrid capacitor network, formed by combining different capacitor types, in an effort to achieve low ESR and high capacitance. This can be a very effective method of reducing output ripple and improving load transient performance. This application report provides a method to analyze how the hybrid capacitor network affects the loop. The *Section 1* section introduces the key characteristics of each of the different types of capacitors. The *Section 2* section discusses peak current mode power stage small signal modeling with a hybrid output capacitor network. Finally, the *Section 3* section verifies the analysis with bench test results on TPS65400EVM.

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Trademarks

1 Introduction

Output capacitors are critical components for a switch-mode power supply. To select output capacitors for a DC/DC switching regulator application, the basic parameters you must pay attention to include capacitance, equivalent series resistance (ESR), rated voltage, and size. Table 1 compares the four types of capacitors.

Table 1. Comparison of Different Types of Capacitors

	CAPACITANCE	ESR	RATED VOLTAGE	SIZE
Multi-layer Ceramic Capacitor	Low	Low	Medium	Small
Aluminum Electrolytic Capacitor	High	High	Various	Large
Tantalum Capacitor	Medium	Medium	Medium	Medium
Polymer Capacitor	High	Medium	Medium	Medium

Generally speaking, MLCC provides very low ESR, which is critical to compress the resistive output ripple. Aluminum electrolytic capacitors provide a large amount of capacitance, but have the highest ESR among the four capacitor types. Tantalum and polymer capacitors have medium-range capacitance values, ESR, and rated voltage. By using a hybrid capacitor network, designers can take advantage of the benefits of each capacitor type. In applications where small ripple, overshoot, and undershoot are required, hybrid output capacitor networks are very common.

Loop stability is another important topic for DC/DC switching regulator circuit design. In DC/DC converter small signal modeling, the capacitance and ESR values of the output capacitor have a direct effect on the poles and zeros in the open loop transfer function. With the presence of a hybrid output capacitor network, new poles and zeros are introduced into the loop by the network itself. This application report discusses how hybrid output capacitors influence the loop, and then verifies the analysis using the TPS65400EVM.

2 Current Mode Power Stage Small Signal Modeling

Figure 1 shows the simplified functional block diagram of a peak current mode DC/DC circuit.

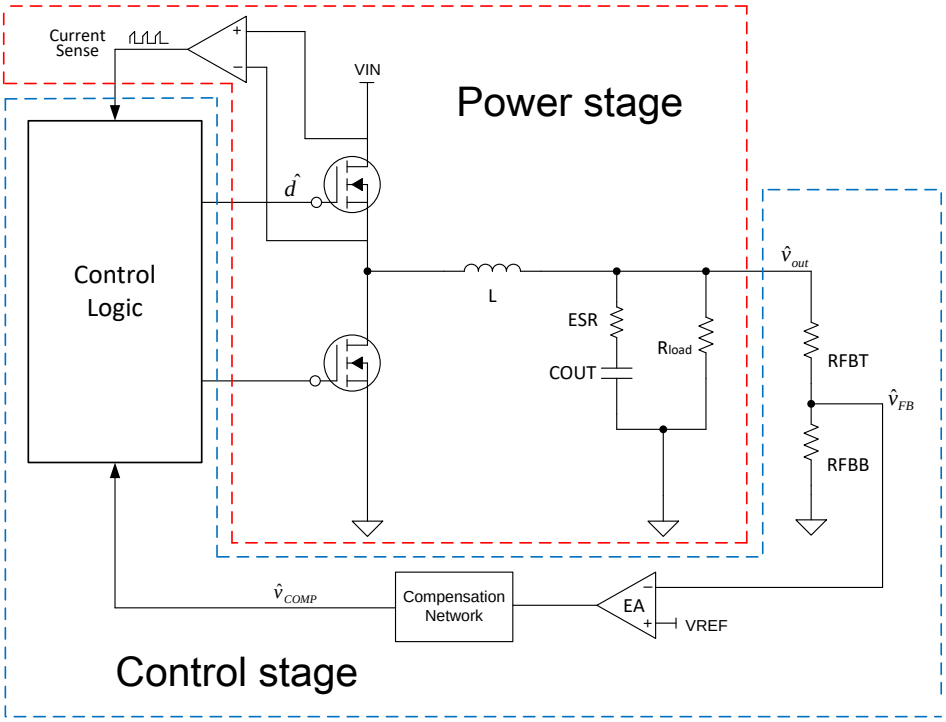

Figure 1. Simplified Current Mode Functional Block Diagram

To analyze and judge the loop stability by open loop transfer function and Bode plot, the loop is split into two components:

$$G_{open}(s) = G_{dv}(s) \cdot H_{vd}(s) \quad (1)$$

where

- $G_{dv}(s)$ are the transfer function from control to the output ($\hat{d}$ to $\hat{v}_{out}$), including the PWM modulator and power stage.
- $H_{vd}(s)$ is the transfer function from the output to control ($\hat{v}_{out}$ to $\hat{d}$), including the feedback path, compensation network.

Poles and zeros in power stage have a direct effect on the loop transfer function. To understand how the hybrid output capacitor network affects the loop, calculate the poles and zeros in the power stage. The calculation can vary in the different control mode, as they have different control to output transfer function $G_{dv}(s)$. This application report shows how to do the calculation based on a current mode DC/DC converter circuit. Impedance of hybrid output capacitor network is discussed first. Based on that, the effect of the network on current mode DC/DC circuit is analyzed.

2.1 Impedance of Hybrid Output Capacitor Network

Figure 1 shows that the output capacitor in the functional block diagram is simplified as a single capacitor. Impedance of a single capacitor with a specific ESR is:

$$Z_{cap}(s) = \frac{1 + s \cdot ESR \cdot C}{sC} \tag{2}$$

When the output capacitor is substituted by an output capacitor network, the situation can be different. Figure 2 shows two capacitors with same or different capacitance and ESR that are put in parallel.

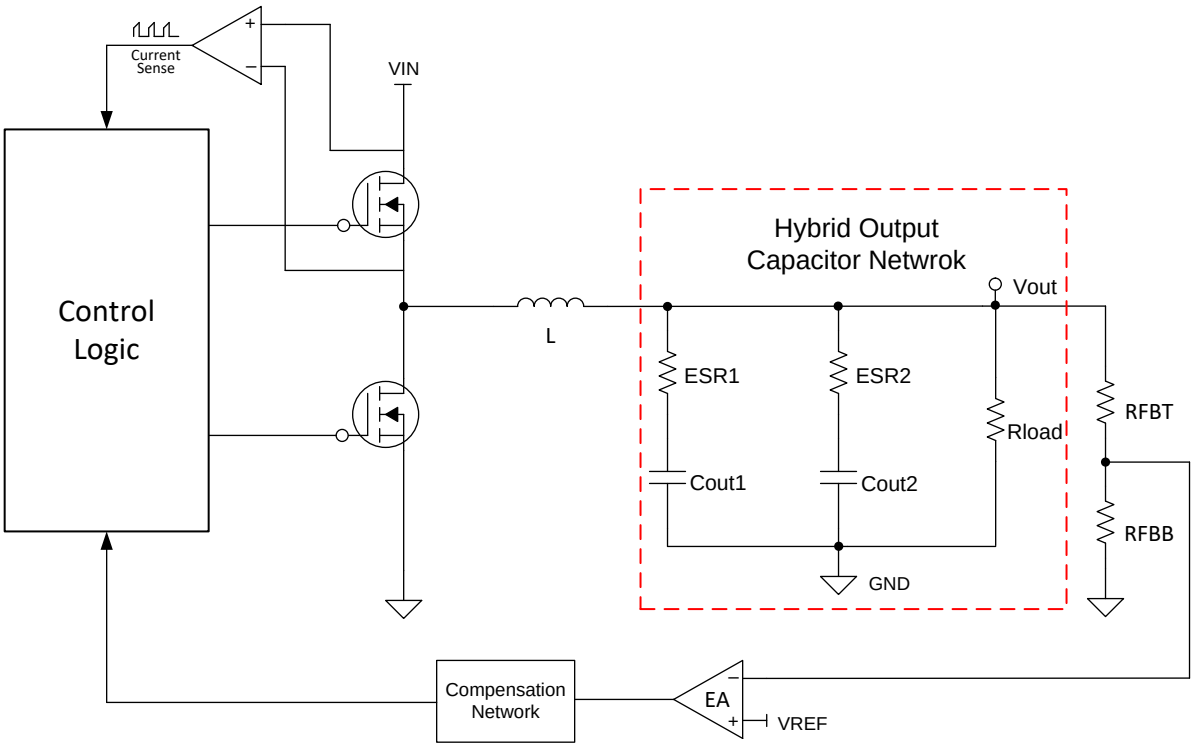

Figure 2. Current Mode Buck Converter Circuit With Hybrid Output Capacitor Network

Impedance of the hybrid capacitor network $Z_{cap}(s)$ can be expressed as:

$$Z_{cap}(s) = (R_1 + \frac{1}{sC_1}) // (R_2 + \frac{1}{sC_2}) \tag{3}$$

where

- R_1 is the ESR of C_1
- R_2 is the ESR of C_2

If you expand Equation 3, you have:

$$Z_{cap}(s) = \frac{(1 + sR_1C_1) \cdot (1 + sR_2C_2)}{s(C_1 + C_2) \cdot \left[1 + s \cdot (R_1 + R_2) \cdot \frac{C_1C_2}{C_1 + C_2}\right]} \tag{4}$$

Equation 4 indicates when the capacitance and ESR are different. There is an initial pole, a parallel pole, and two ESR zeros in the impedance expression.

A specific situation is where the two capacitors are same, C1 = C2 = C, R1 = R2 = R. Equation 4 can be further simplified as:

$$Z_{cap}(s) = \frac{1 + sRC}{s \cdot 2C} \tag{5}$$

In this situation, two of the same output capacitors can be equalized to one single capacitor with two times capacitance and half ESR.

2.2 Pole and Zero Calculation in Current Mode Power Stage

The distribution of poles and zeros in the loop transfer function depends on both power stage characteristic and control mode. As discussed in the *Current-Mode Modeling for Peak, Valley and Emulated Control Methods Application Report*, the transfer function of peak current mode buck converter power stage is:

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{1}{\frac{R_i}{R_o} + \frac{1}{K_m}} \cdot \frac{1 + \frac{s}{\omega_{ESR}}}{(1 + \frac{s}{\omega_0}) \cdot (1 + \frac{s}{\omega_L})}$$

where

- R_o is the loading resistance
- K_m is the modulator voltage gain, which is given by $K_m = \frac{VIN}{V_{ramp}}$
- R_i is the product of current sense gain and current sense resistance
- ω_0 is the dominant pole
- ω_L is the inductor pole
- ω_{ESR} is the ESR zero of the output capacitor (6)

The dominant pole locates at the frequency where the impedance of output capacitor equals to the loading resistance:

$$\omega_{ESR} = \frac{1}{ESR \times C_{OUT}} \tag{7}$$

The inductor pole locates at the frequency where the impedance of the inductor equals to the current-loop gain:

$$\omega_L = \frac{K_m \cdot R_i}{L} \tag{8}$$

In most cases, $K_m \times R_i \gg 1$, so ω_0 can be simplified as:

$$\omega_0 = \frac{1}{C_{out} \cdot R_o} \tag{9}$$

Also, as $K_m \times R_i \gg 1$, ω_L is usually much higher than the bandwidth, which means the pole has limited effect on the loop stability and can be ignored in the following analysis.

The ESR zero of output capacitor locates at:

$$\omega_{ESR} = \frac{1}{ESR \times C_{OUT}} \tag{10}$$

Equation 6 is further simplified as:

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{R_o}{R_i} \cdot \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{\omega_0}} \tag{11}$$

Figure 3 shows the simplified Bode plot.

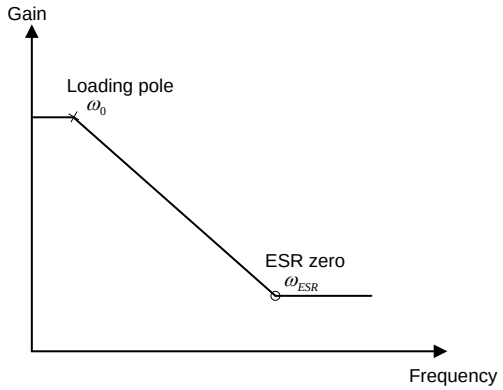

Figure 3. Simplified Power Stage Bode Plot of Single Output Capacitor Configuration

When the output capacitor is substituted by a hybrid capacitor network, modify Equation 11 as:

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{R_o}{R_i} \cdot \frac{(1 + \frac{s}{\omega_{ESR\,1}})(1 + \frac{s}{\omega_{ESR\,2}})}{(1 + \frac{s}{\omega_0})(1 + \frac{s}{\omega_p})}$$

where

- ω_0 is the dominant loading pole in current mode, given by $\omega_0 = \frac{1}{R_o \cdot (C_1 + C_2)}$
- ω_p is the parallel pole introduced by the parallel capacitors, given by $\omega_p = \frac{1}{(R_1 + R_2) \cdot \frac{C_1 C_2}{C_1 + C_2}}$
- ω_{ESR1} and ω_{ESR2} are the ESR zeros of the capacitors, given by

$$\omega_{ESR1} = \frac{1}{ESR_1 \cdot C_1} \quad \omega_{ESR2} = \frac{1}{ESR_2 \cdot C_2} \tag{12}$$

Figure 4 shows the simplified Bode plot.

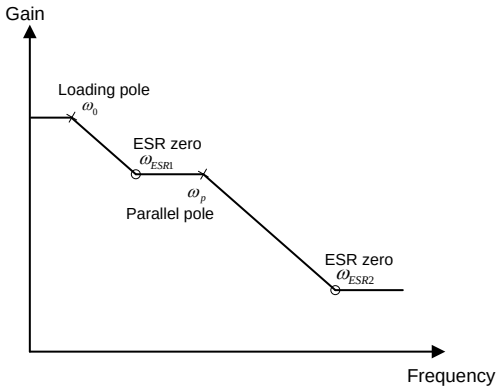

Figure 4. Simplified Power Stage Bode Plot of Hybrid Output Capacitor Network Configuration

If you compare Equation 11 and Equation 12, you have:

- The dominant pole ω_0 is determined by loading resistance and the sum of all capacitance in the power stage.
- ESR zero of the electrolytic capacitor remains at the same frequency.
- An additional pole ω_p is introduced by the two different capacitors in output capacitor network.

Take these poles and zeros into consideration when designing the loop compensation with a hybrid output capacitor network. These results are verified on a TPS65400EVM in *Section 3*.

3 Bench Verification

3.1 TPS65400 Introduction

The TPS65400 is a 4.5-V to 18-V, synchronous quad buck converter with PMBus/I^{2}C interface. The device works in peak current mode with an external loop compensation network. To support high output capacitance in this test, compensation zero formed by R_{comp} and C_{comp} is placed at 0.6 kHz. The rolling pole formed by R_{comp} and C_{roll} locates at 141.6 kHz. The test is performed on the first channel of the TPS65400EVM. Table 2 lists some of the basic configurations. See the *TPS65400 EVM User's Guide* for other detailed descriptions and configurations.

Table 2. Basic Configurations of TPS65400EVM

VIN	12 V
VOUT	3.3 V
Switching Frequency	500 kHz
Loading Current	1.5 A
Loading Pole	0.33 kHz
Compensation Zero	0.6 kHz
Rolling pole	141.6 kHz

3.2 Bench Test

To verify the calculation in the previous section, a Bode plot is done for the output capacitor network formed by all MLCC, hybrid, and single polymer capacitors.

3.2.1 All MLCC

Figure 5 shows the output capacitor network is formed all by MLCC. The part number of the capacitor is GRM31CR61A476KE15L. Taking the DC bias effect into consideration, the total effective capacitance is about 224.8 µF. Figure 6 shows the Bode plot of all MLCC configuration as the output capacitor.

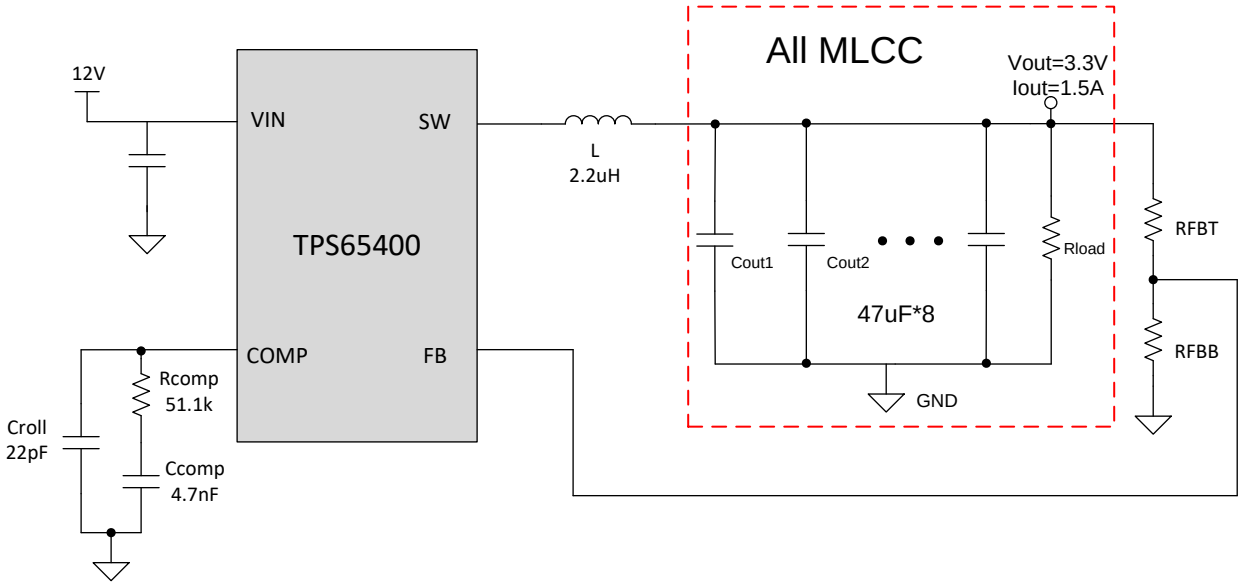

Figure 5. Simplified Schematic of All MLCC Output Capacitor Configuration

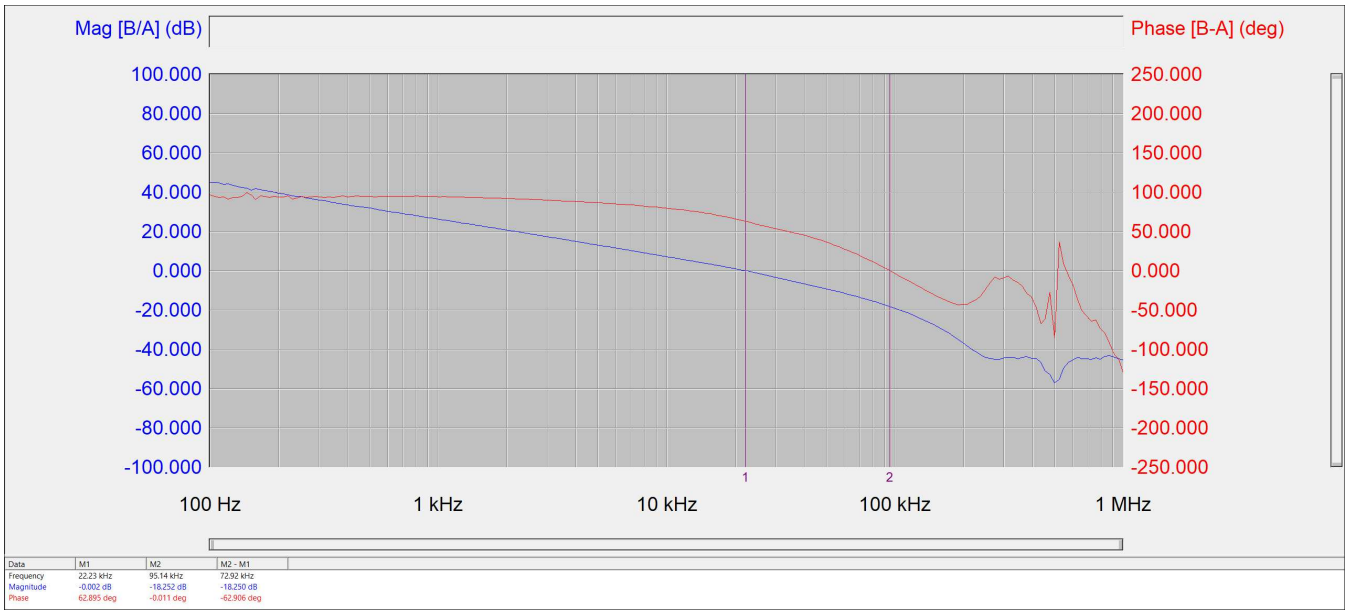

Figure 6. Bode Plot of All MLCC Output Capacitor Configuration (V_{OUT} = 3.3 V, I_{OUT} = 1.5 A)

According to the characteristic curve, the capacitor ESR is about 3 mΩ. ESR zero of single capacitor locates at about 1.95 MHz, which is much higher than the bandwidth. As in the previous analysis, putting the capacitors in parallel has no effect on the frequency of ESR zero. That is to say, besides the error amplifier pole, the loading pole and the compensation zero, there is no any other pole nor zero within the bandwidth. The gain curve keeps going down with a –20 dB/dec slope after the loading pole and compensation zero. The bandwidth is about 22.2 kHz, and the phase margin is 62.9 degrees.

3.2.2 Hybrid Output Capacitor Network

Figure 7 shows the hybrid output capacitor network is formed by one polymer capacitor and four MLCCs. Total effective output capacitance is about 222 µF. Table 3 lists the parameters of the components.

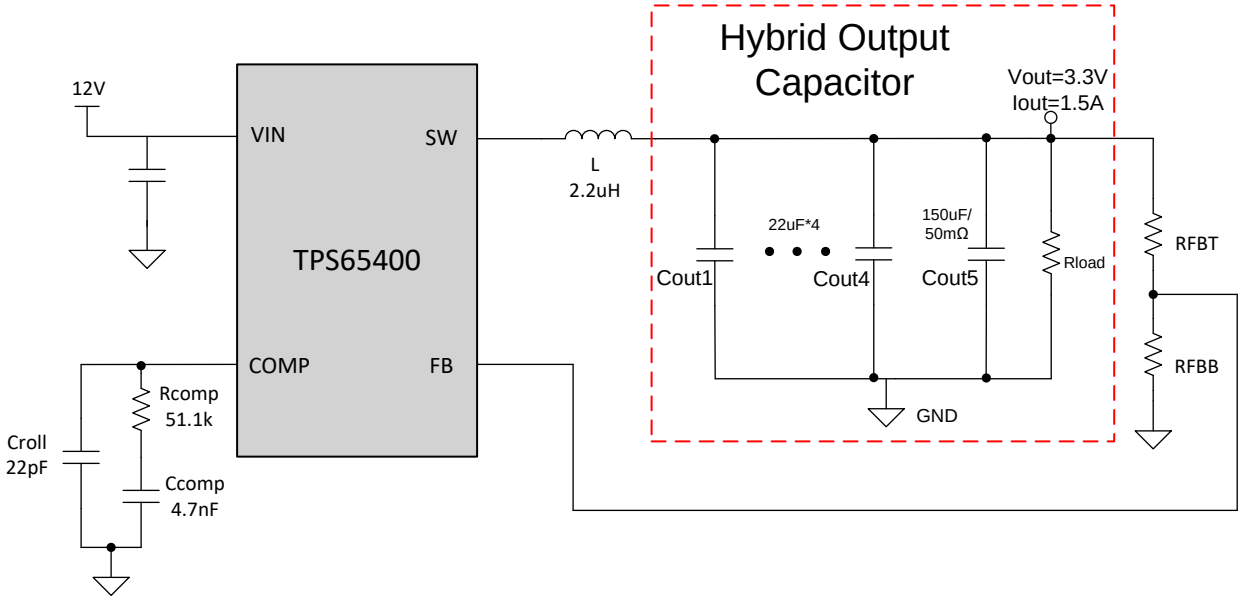

Figure 7. Simplified Schematic of Hybrid Output Capacitor Configuration

Table 3. Parameters of Capacitors Used in Output Capacitor Network

PART NUMBER	CAPACITANCE/µF	ESR /mΩ	COUNT
16TQC150MYF	150	50	1
GRM31CR71A226KE 15L	22	3	4

To analyze this hybrid network, the same four MLCC can be equalized to one single MLCC by Equation 5. Then, according to the Equation 12, in the hybrid output capacitor network, ESR zero of the polymer capacitor locates at Equation 13.

$$f_{ESR1} = \frac{1}{2\pi \cdot ESR_1 \cdot C_1} = 21.2kHz \tag{13}$$

The pole formed by putting different capacitors in parallel locates at Equation 14.

$$f_p = \frac{1}{2\pi \cdot (ESR_1 + ESR_2) \cdot (C_1 // C_2)} = 61.8kHz \tag{14}$$

Figure 8 shows the Bode plot. The existence of the polymer capacitor ESR zero f_{ESR1} and the parallel pole f_p extends the bandwidth to 43 kHz, with a phase margin of 79.7 degrees. Judging from the gain curve, the zero and pole can be identified at the calculated frequency above. At a higher frequency, the parallel pole together with the rolling pole formed by R_{comp} and C_{roll} keeps the gain curve rapidly going down.

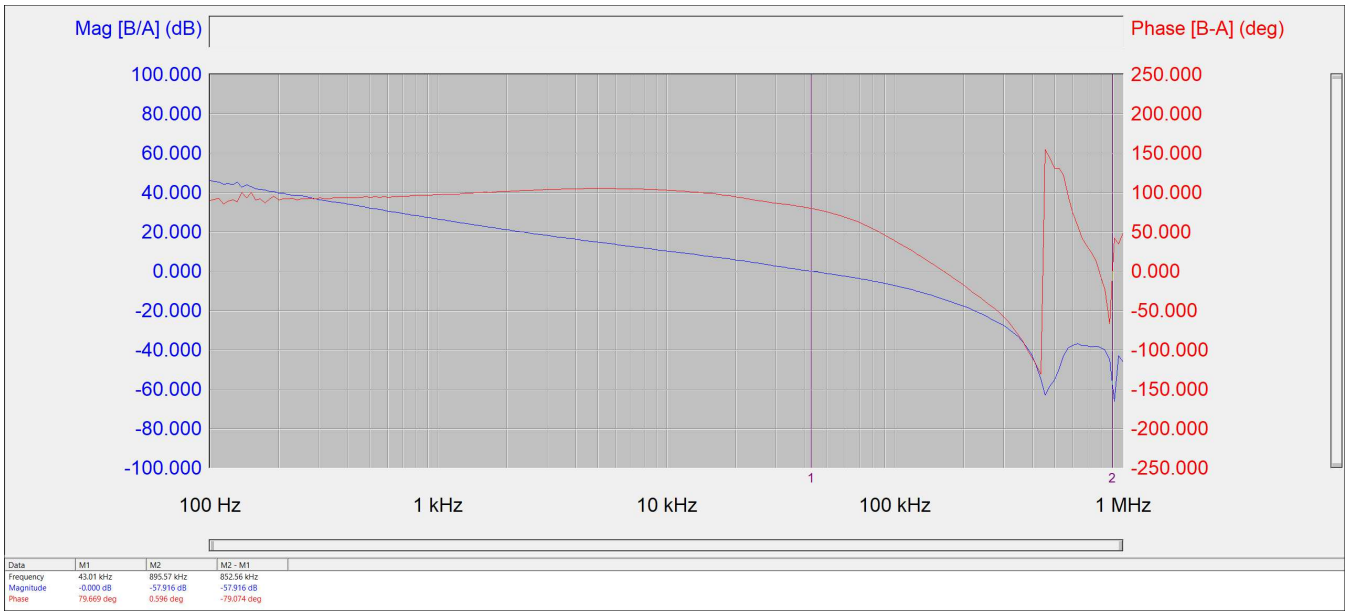

Figure 8. Bode Plot of Hybrid Output Capacitor Configuration

3.2.3 Single Polymer Capacitor

Figure 9 shows the output capacitance consists of only one polymer capacitor with high ESR value.

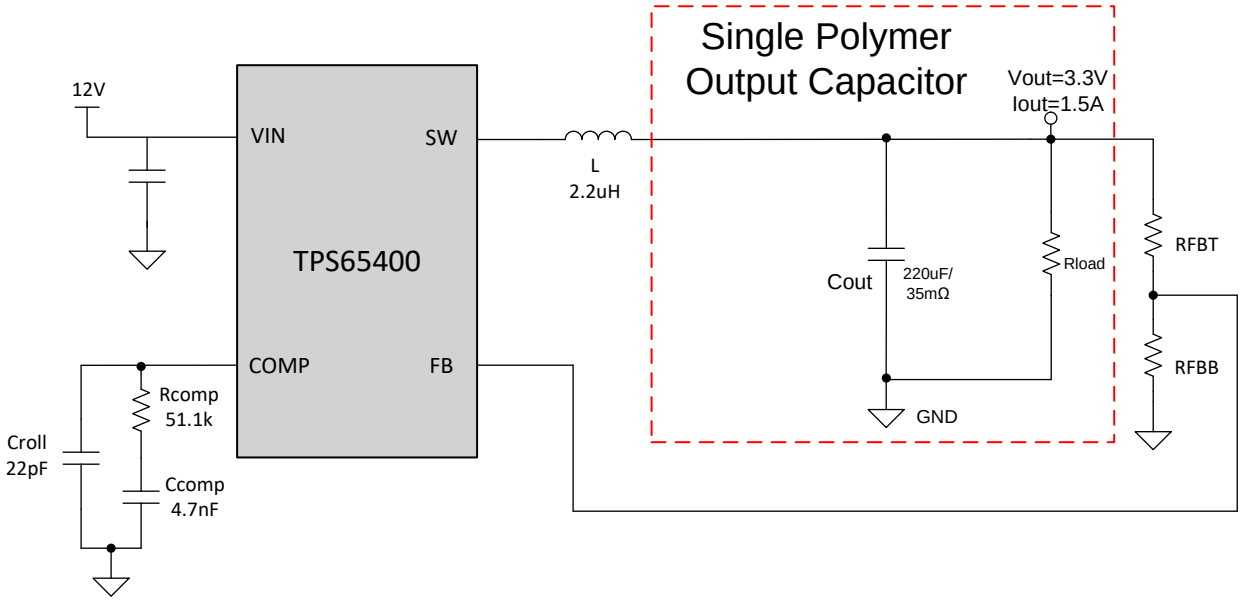

Figure 9. Simplified Schematic of Single Polymer Output Capacitor Configuration

The part number of the polymer capacitor is 6TPE220MAZB. It has a capacitance of 220 µF, with 35 mΩ ESR. ESR zero locates at Equation 15.

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C} = 20.7kHz \quad (15)$$

To make the comparison more convincing, the total effective output capacitance is set to be almost the same with the previous test. Figure 10 shows the Bode plot.

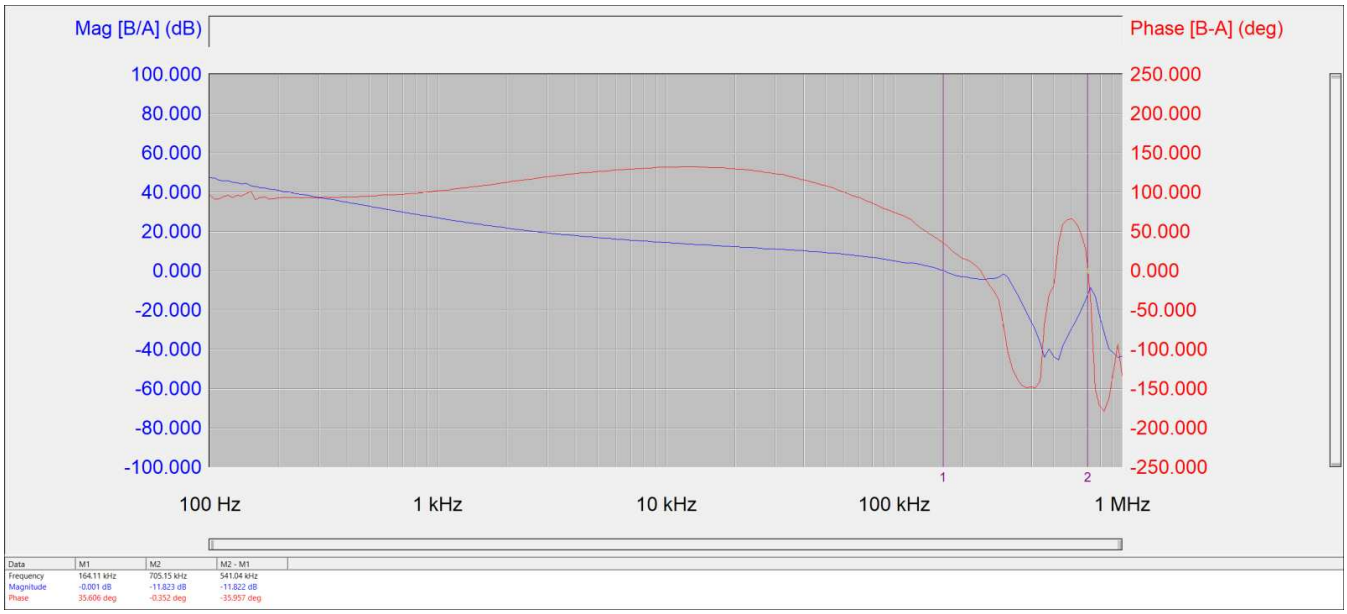

Figure 10. Bode Plot of Single Polymer Output Capacitor Configuration (V_{OUT} = 3.3 V, I_{OUT} = 1.5 A)

Because of the low frequency ESR zero, the gain curve is going down very slowly until the rolling pole (141 kHz) takes effect. The bandwidth is extended to 164 kHz, which has exceeded 1/5 switching frequency. Phase margin is about 35.6 degree. Obviously, the compensation network designed for other configurations is not doing well in this situation.

3.2.4 Comparison

To show how the hybrid configuration affect the loop, the Bode plot of three configurations are drawn together. Figure 11 shows the gain-frequency response curves.

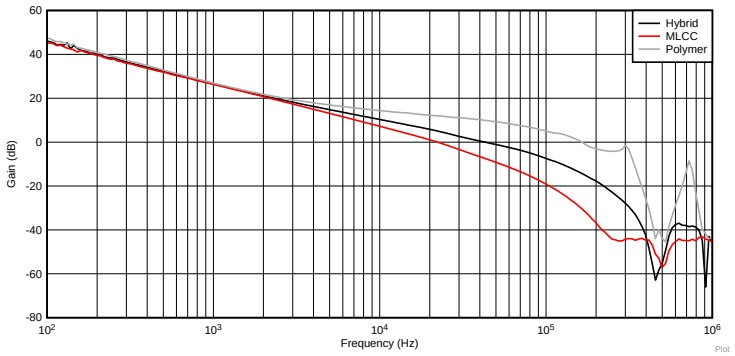

Figure 11. Gain Frequency Response Comparison Among Hybrid, MLCC, and Polymer Output Capacitor Configuration

Effective output capacitance is almost the same among the three configurations. However, MLCC configuration has the smallest bandwidth because there is no ESR zero introduced by the high ESR capacitor. For the hybrid configuration consisting of MLCC and polymer capacitors, the ESR zero locates at the same frequency with the standalone polymer capacitor configuration. As calculated in Equation 14, the parallel pole introduced by hybrid configuration locates at 61.8 kHz. It is the parallel pole which leads to the significant difference between the hybrid configuration and the standalone polymer capacitor.

3.3 Conclusion

From the analysis and bench verification, three conclusions can be drawn.

- The frequency of loading pole depends on the total effective capacitance of the output capacitor network.
- In the parallel output capacitor network, ESR zero of each capacitor is still taking effect independently. Also, by putting two output capacitors in parallel, a parallel pole is introduced into the loop.
- The effect brought by the ESR zero and parallel pole depends on how close they are on the frequency axis. In most cases, due to the DC bias degrading of MLCC, solution size, and cost, the total effective capacitance of MLCC is usually much smaller than that of electrolytic or other capacitor with higher capacitance and ESR. See the expression of ω_p, $\omega_p = \frac{1}{(R_1 + R_2) \cdot C_1 // C_2}$.

It can be identified that the bigger difference between C1 and C2, the further the parallel pole and the ESR zero are, and the less cancellation between ESR zero and parallel pole. This means its Bode plot curve looks more like single output capacitor with high ESR. Take this into consideration when doing the loop compensation design.

4 Summary

Hybrid output capacitor network with high capacitance is widely used to support applications with strict limitation on ripple, overshoot and undershoot. This application report analyzed the poles and zeros in the power stage when using a hybrid output capacitor network theoretically. Furthermore, the analysis is verified on TPS65400EVM. The conclusion can be a guidance for the compensation design of DC/DC circuit with hybrid output capacitor network.

5 References

- Texas Instruments, *TPS65400 4.5- to 18-V Input Flexible Power Management Unit with PMBus/I2C Interface Data Sheet*
- Texas Instruments, *TPS65400EVM 4.5- to 18-V Input Flexible Power Management Unit with PMBus/I2C Interface Evaluation Module User's Guide*
- Texas Instruments, *Current-Mode Modeling for Peak, Valley and Emulated Control Methods Application Report*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2018) to A Revision	Page
• Edited the application report for clarity.	1

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