

# MOSFET Driver Circuit Design Guide for TPS512xx

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## ABSTRACT

The driver circuit parameters are critically important for a controller. A better selection of parameters not only increases the system safety, but also improves the efficiency. First, this application report talks about MOSFET parameters and the turning on/off procedure. Then, the IC driver capability and bootstrap circuit are introduced. Lastly, the document uses the TPS51285B as an example to explain how to adjust driver parameters.

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## 1 Introduction

When the controller IC of TPS512xx (including TPS51225, TPS51275, TPS51285, TPS51220, and others) is applied in a circuit, the selection of MOSFET and driver parameters are necessary. The more reasonable MOSFET and driver parameters have a better effect on efficiency, system safety, and EMI. Driver parameters for the controller include bootstrap resistor, bootstrap cap, and gate resistor.

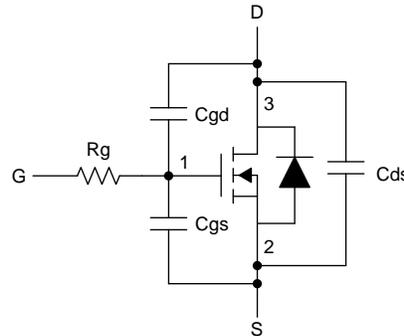
## 2 MOSFET

### 2.1 MOSFET Parameters

This section mainly introduces the parameters of MOSFET and how they affect circuit performance. The MOSFET CSD87330Q3D [CSD87330Q3D Synchronous Buck NexFET Power Block Data Sheet](#) is introduced as an example.

$BV_{DSS}$ ,  $I_{DSS}$ ,  $I_{GSS}$ ,  $V_{GS(th)}$ , and  $Z_{DS(on)}$  are easily understood. Enough  $BV_{DSS}$  (drain to source voltage) is required. A lower  $Z_{DS(on)}$  is better because it consumes lower power loss.  $I_{DSS}$  and  $I_{GSS}$  are leakage current, which is always very small.

Dynamic characteristics including  $Q_g$ , parasitic cap, and rising time are more important for circuit. These parameters affect switching time and switching loss. [Figure 1](#) shows the switching model of the MOSFET and the most important parasitic components that influence switching performance.



**Figure 1. MOSFET Model**

There is a parasitic cap,  $C_{GD}$ , between the drain and gate.  $C_{GS}$  is between the gate and source.  $C_{DS}$  is between the drain and source. In the MOSFET data sheet, these capacitors are not mentioned directly. Their values are given indirectly by  $C_{ISS}$ ,  $C_{OSS}$ , and  $C_{RSS}$  capacitor values. [Equation 1](#), [Equation 2](#), and [Equation 3](#) show how to calculate these values.

$$C_{GD} = C_{RSS} \tag{1}$$

$$C_{GS} = C_{ISS} - C_{RSS} \tag{2}$$

$$C_{DS} = C_{OSS} - C_{RSS} \tag{3}$$

When the switch mode operation of the MOSFET is considered, the goal is to switch between the lowest and highest resistance states of the device. The switching time between two states is influenced by the parasitic cap. Ultimately, the switching performance of the MOSFET is determined by how quickly the voltages can be charged across these capacitors. If the parasitic cap is larger, it needs a stronger driver and takes more time to charge the cap. It consumes more switching loss, and the efficiency is lower. Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the MOSFET.

MOSFET also gives a parameter  $Q_g$  that indicates MOSFET switch performance from practical turning on or off side. In the MOSFET EC table,  $Q_{gd}$ ,  $Q_{gs}$ ,  $Q_{g(th)}$ , and  $Q_{oss}$  are also given.  $Q_g$  is the total gate charge. If  $Q_g$  is larger, it needs a stronger driver and more charge. [Figure 2](#) shows the relationship between  $Q_g$  and  $V_{gs}$  voltage and how much charge the gate of MOSFET requires at different gate voltage. For example, if  $V_{GS}$  wants to get 5 V, the gate of MOSFET need to be charged about 4 nc.  $V_{GS,miller}$  voltage can also be derived from [Figure 2](#). In this example, it is about 2.5 V.

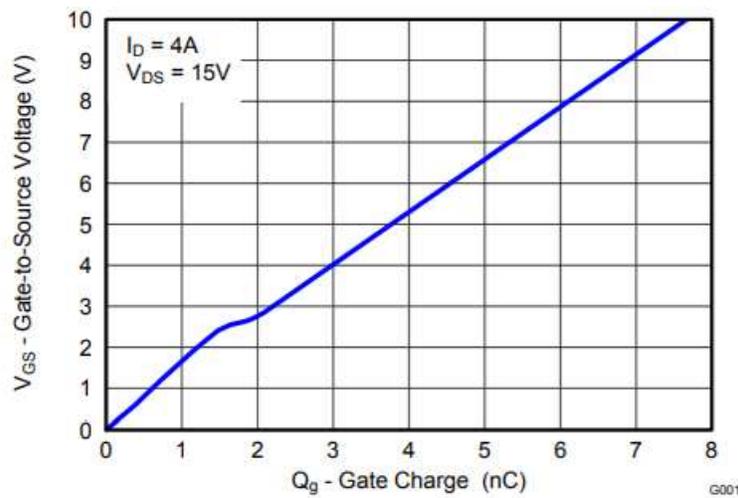


Figure 2. MOSFET Gate Charge

The next important parameter to mention is the gate resistance,  $R_G$ . This parasitic resistance describes the resistance associated by the gate signal distribution within the device. Its importance is critical in high speed switching applications because it is located between the driver and the input capacitor of the device, directly impeding the switching times and the  $dv/dt$  immunity of the MOSFET.

Rising time is introduced in turning on procedure.

## 2.2 MOSFET Turnon and Turnoff Procedure

Figure 3 shows the MOSFET turning on procedure. The left side shows a simple driver circuit and MOSFET. It also gives current direction when the MOSFET turns on. The right side gives the waveforms of  $V_{GS}$ ,  $I_G$ ,  $V_{DS}$ , and  $I_D$ .

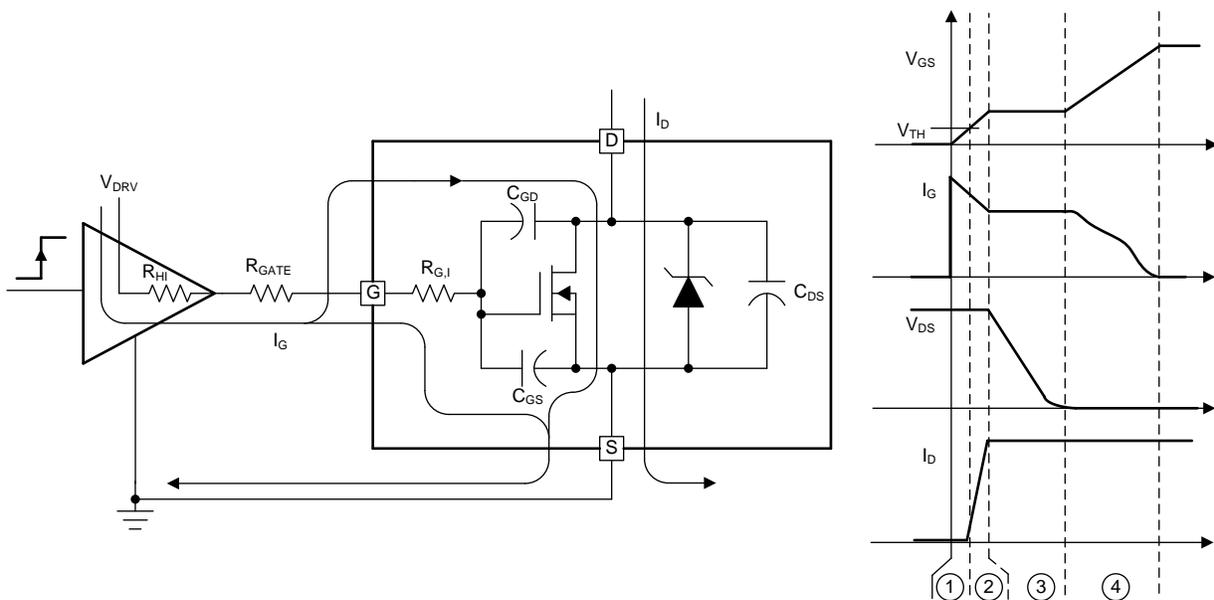


Figure 3. Turnon Procedure

In the first interval, the input capacitance of the device is charged from 0 V to  $V_{TH}$ . During this interval, most of the gate current is charging the  $C_{GS}$  capacitor. At this time, a small current is flowing through the  $C_{GD}$  capacitor. As the voltage increases at the gate terminal, the  $C_{GD}$  voltage of the capacitor has to be slightly reduced. This period is called the turnon-on delay. In the MOSFET data sheet,  $t_{d(on)}$  indicates this time. During this time, it cannot produce switching loss, because there is no current that goes through the MOSFET.  $Q_{g(th)}$  is the required charge of MOSFET gate. If  $C_{GS}$  is large, then  $Q_{g(th)}$  requires an increased charge.

Once the gate is charged to the threshold level, the MOSFET is ready to carry current. In the second interval, the gate voltage is rising from  $V_{TH}$  to the Miller plateau level,  $V_{GS,Miller}$ . This is the linear operation of the device when the current is proportional to the gate voltage. On the gate side, the current is flowing into the  $C_{GS}$  and  $C_{GD}$  capacitors, just like in the first time interval and the  $V_{GS}$  voltage is increasing. On the output side of the device, the drain current is increasing, while the drain-to-source voltage keeps at the previous level.  $Q_{gs}$  is the required charge when the gate voltage rises from 0 to  $V_{GS,Miller}$ . This interval time depends on the  $C_{ISS}$ . Switching loss is produced during this interval and the value is the area that voltage and current overlap. Normally, the voltage and current depends on external conditions. So to reduce switching loss largely, use a smaller  $C_{RSS}$  and  $Q_{gd}$  MOSFET.

Entering into the third interval of the turnon procedure, the gate is charged to the sufficient voltage  $V_{GS,Miller}$  to carry the entire load current. That now allows the drain voltage to fall. While the drain voltage falls across the device, the gate-to-source voltage stays steady. This is the Miller plateau region in the gate voltage waveform. All the gate current available from the driver is diverted to discharge the  $C_{GD}$  capacitor to facilitate the rapid voltage change across the drain-to-source terminals. The drain current of the device stays constant since it is now limited by the external circuitry, that is, the DC current source.  $C_{RSS}$  and  $Q_{gd}$  are the main influences on this interval. Switching loss is also produced in this interval.

The last step of the turnon is to fully enhance the conducting channel of the MOSFET by applying a higher gate drive voltage. The final amplitude of  $V_{GS}$  determines the ultimate on-resistance of the device during its on-time. Therefore, in this fourth interval,  $V_{GS}$  is increased from  $V_{GS,Miller}$  to its final value,  $V_{DRV}$ . This is accomplished by charging the  $C_{GS}$  and  $C_{GD}$  capacitors, so the gate current is now split between the two components. While these capacitors are being charged, the drain current is still constant, and the drain-to-source voltage is slightly decreasing as the on resistance of the device is being reduced.

$T_r$  is the rising time which includes last three intervals.

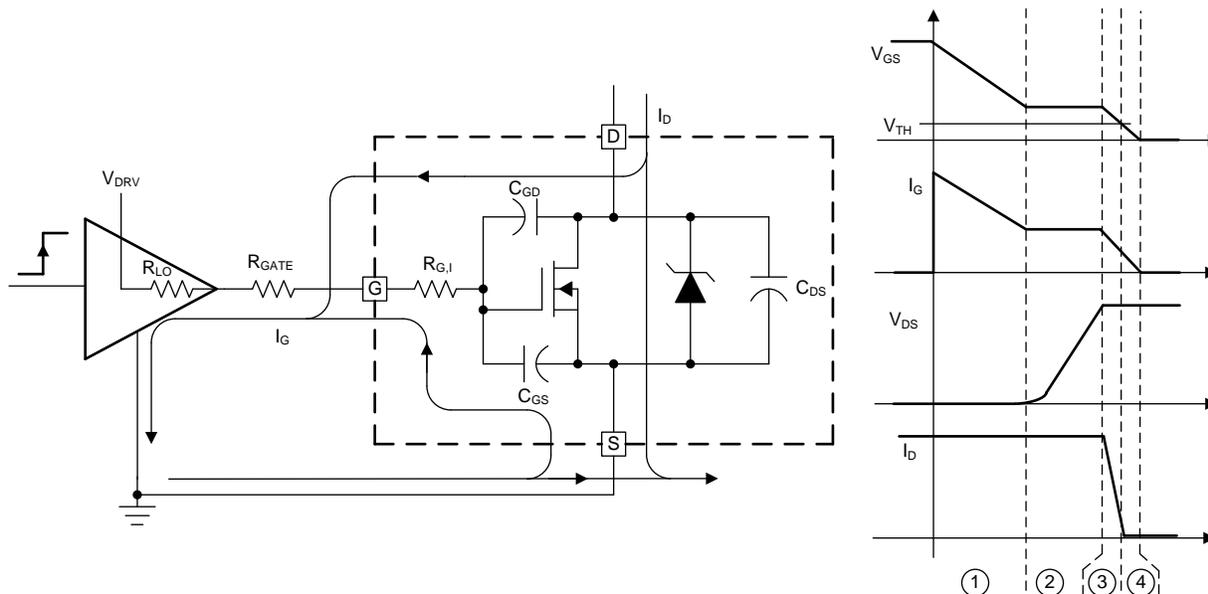


Figure 4. Turnoff Procedure

The description of the turnoff procedure for the MOSFET transistor is basically back tracking the turnon steps from the previous section. Figure 4 shows the turnoff procedure. It is not introduced here in detail.  $Q_{OSS}$ ,  $t_{d(off)}$ , and  $t_f$  indicate the turnoff parameters.

### 3 Controller IC

#### 3.1 IC Driver Resistance

In the [Ultra-Low Quiescent \(ULQ\) Dual Synchronous Step-Down Controller with 5 V and 3.3 V LDOs Data Sheet](#) EC table, the high-side MOSFET driver and low-side MOSFET driver resistance are shown as [Figure 5](#), along with test conditions. Driver resistance indicates the driver capability.

MOSFET DRIVERS				
R <sub>DRVH</sub>	DRVH resistance	Source, I <sub>DRVH</sub> = -50 mA, (V <sub>VBST</sub> - V <sub>SW</sub> ) = 5 V	3	Ω
		Sink, I <sub>DRVH</sub> = 50 mA, (V <sub>VBST</sub> - V <sub>SW</sub> ) = 5 V	1.9	
R <sub>DRV L</sub>	DRV L resistance	Source, I <sub>DRV L</sub> = -50 mA, V <sub>VREGS</sub> = 5 V	3	Ω
		Sink, I <sub>DRV L</sub> = 50 mA, V <sub>VREGS</sub> = 5 V	0.9	

**Figure 5. Driver Resistance**

A crude estimate of the gate rising time can be calculated using simplified linear approximations of the gate drive current. The gate drive current can be determined using the below equation when MOSFET turns on. [Equation 4](#) shows the gate current in procedure 1. [Equation 5](#) is the gate current in procedure 2. [Equation 6](#) is the gate current in procedure 3, and [Equation 7](#) is the gate current in procedure 4. In the following equation, I<sub>G</sub> is the gate current. V<sub>DRV</sub> is drive voltage. R<sub>gate</sub> is total drive resistance. It includes IC drive resistance, MOSFET internal gate resistance and gate resistance of PCB board.

$$I_{G1} = \frac{V_{DRV} - 0.5 \times V_{TH}}{R_{gate}} \quad (4)$$

$$I_{G2} = \frac{V_{DRV} - 0.5 \times (V_{TH} + V_{GS,Miller})}{R_{gate}} \quad (5)$$

$$I_{G3} = \frac{V_{DRV} - V_{GS,Miller}}{R_{gate}} \quad (6)$$

$$I_{G4} = \frac{V_{DRV} - 0.5 \times (V_{DRV} + V_{GS,Miller})}{R_{gate}} \quad (7)$$

Assuming that I<sub>G1</sub> charges the input capacitor of the MOSFET from 0 to V<sub>TH</sub>, use [Equation 8](#) to calculate the charging time. I<sub>G2</sub> charges the input capacitor of MOSFET from V<sub>TH</sub> to V<sub>GS,Miller</sub>. [Equation 9](#) shows this period charging time. I<sub>G3</sub> is the discharge current of the C<sub>RSS</sub> capacitor while the drain voltage changes from V<sub>DS</sub> to 0. [Equation 10](#) shows the discharging time. I<sub>G4</sub> charges input capacitor of MOSFET from V<sub>GS,Miller</sub> to V<sub>DRV</sub>. [Equation 11](#) shows the charging time.

$$t_1 = C_{ISS} \times \frac{V_{TH}}{I_{G1}} \quad (8)$$

$$t_2 = C_{ISS} \times \frac{V_{GS,Miller} - V_{TH}}{I_{G2}} \quad (9)$$

$$t_3 = C_{RSS} \times \frac{V_{DS}}{I_{G3}} \quad (10)$$

$$t_4 = C_{ISS} \times \frac{V_{DRV} - V_{GS,Miller}}{I_{G4}} \quad (11)$$

From the previous equation, the gate rising time depends on drive voltage, total gate resistance, and many MOSFET parameters. If a faster gate rising time is requested, it is better to use the MOSFET of the smaller C<sub>ISS</sub>, C<sub>RSS</sub>, and smaller gate resistance. If you use it the same way, gate falling time also can be estimated.

Switching loss of MOSFET is produced during period 2 and 3. During  $t_2$ , the drain voltage is  $V_{DS}$  and the current is ramping from 0 to  $I_D$ . Again, using linear approximations of the waveforms, the power loss of MOSFET for this period can be estimated from Equation 12. In the below equation, T is the switching period. During the time  $t_3$ , the drain voltage is falling from  $V_{DS}$  to near 0 V. Equation 13 shows how to calculate the power loss.

$$P_2 = \frac{t_2}{T} \times V_{DS} \times \frac{I_D}{2} \quad (12)$$

$$P_3 = \frac{t_3}{T} \times \frac{V_{DS}}{2} \times I_D \quad (13)$$

Calculating the exact switching losses is almost impossible. The reason is the effect of the parasitic inductive components significantly alters the current and voltage waveforms, as well as the switching times during the switching procedures. Taking into account the effect of the different source and drain inductances of a real circuit results in second order differential equations to describe the actual waveforms of the circuit. Since the variables, including gate threshold voltage, MOSFET capacitor values, and driver output impedances, have a very wide tolerance, the above described linear approximation seems to be a reasonable enough compromise to estimate gate rising time and switching losses in the MOSFET.

### 3.2 Bootstrap Circuit

Figure 6 shows the bootstrap circuit of the IC. Normally, there is a 5 V LDO power supply to charge the external cap, so the BST PIN voltage is higher 5 V than SW PIN that also connects with high-side MOSFET source terminal. When the current goes through from bootstrap cap to high-side MOSFET gate, high-side MOSFET turns on. When the current goes through from high-side gate to SW, high-side MOSFET turns off. During the time of high-side MOSFET turning off, 5 V LDO can charge the bootstrap cap.

The Bootstrap resistor influences switching rising slew rate. If the resistor is larger, the current of charging high-side MOSFET gate is smaller, so the slew rate of switching rising is slower. At the same time, the switching loss is larger and efficiency is lower. The advantage is that SW overshoot voltage decreases and EMI noise is small.

The bootstrap cap is used to turn on high-side MOSFET and maintain it on. If the cap is too small, it cannot maintain enough time for high-side MOSFET on. It can happen to the BST under voltage protection. If the cap is too large, it needs a long time to charge the cap. Normally, a 0.1  $\mu$ F cap is enough for TPS512XX family parts.

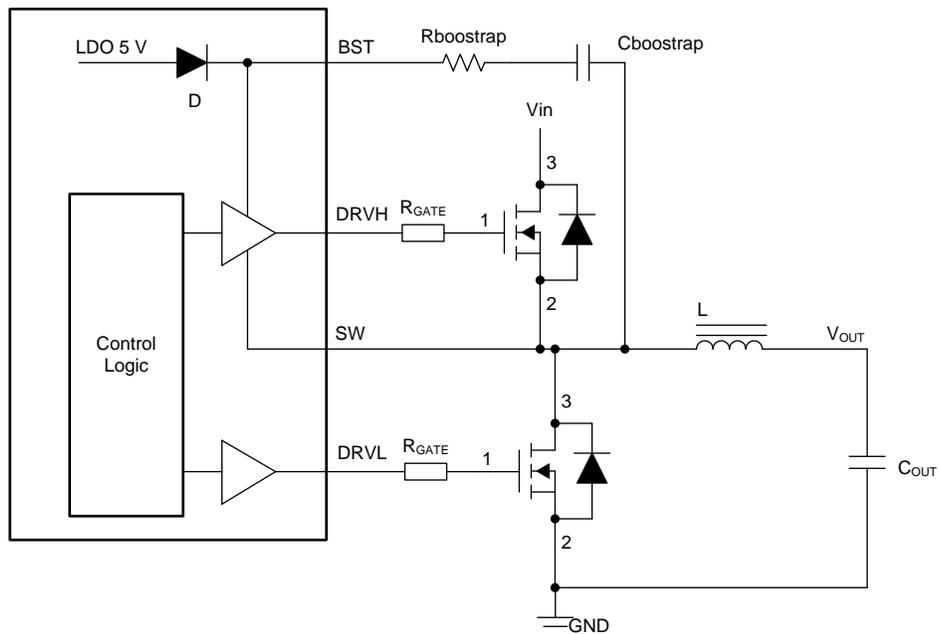


Figure 6. Bootstrap Circuit

#### 4 Adjust Driver Parameters

In theory, the quickest slew rate of switching is the best, because the switching loss is the lowest. It can cause larger switching over voltage and EMI noise. So the driver parameters must be adjusted to guarantee the safety of the MOSFET. The best solution, under the premise of ensuring safety, is that the slew rate of switching must be as fast as it can.

The following waveforms are tested based on TPS51285B with CSD87330Q3D. The information of other parts is available for reference of the [Dual Synchronous Step-Down Fixed Output Controller with 5-V and 3.3-V LDOs User's Guide](#). In the following waveforms, channel 1 is the high-side MOSFET gate to GND. Channel 2 is the low-side MOSFET gate to GND. Channel 3 is the SW waveform. Channel M is the high-side MOSFET gate to high-side MOSFET source voltage. The input voltage is 12 V, the output voltage is 3.3 V, and the output current is 5 A.

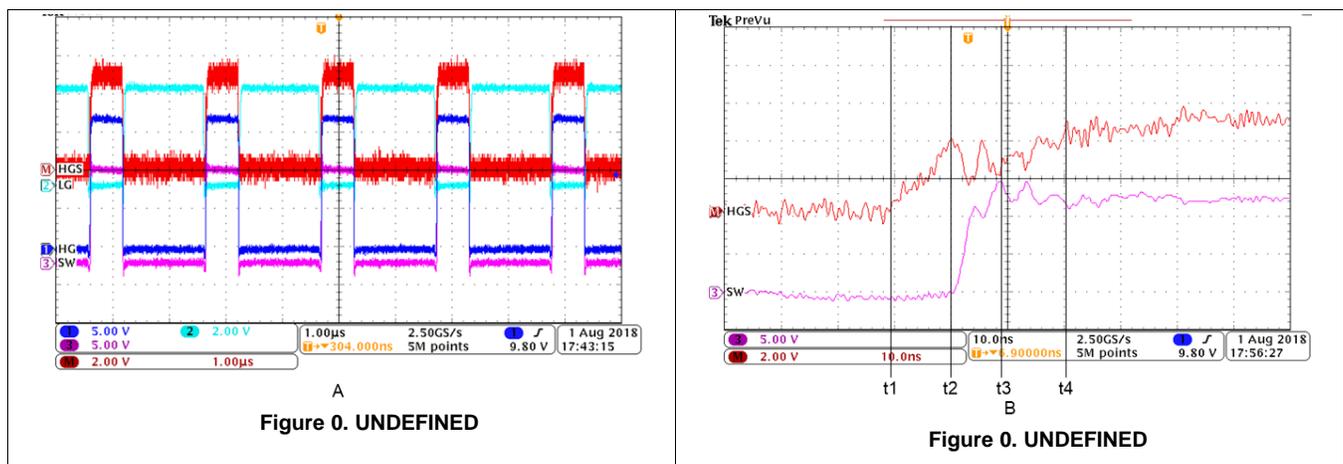
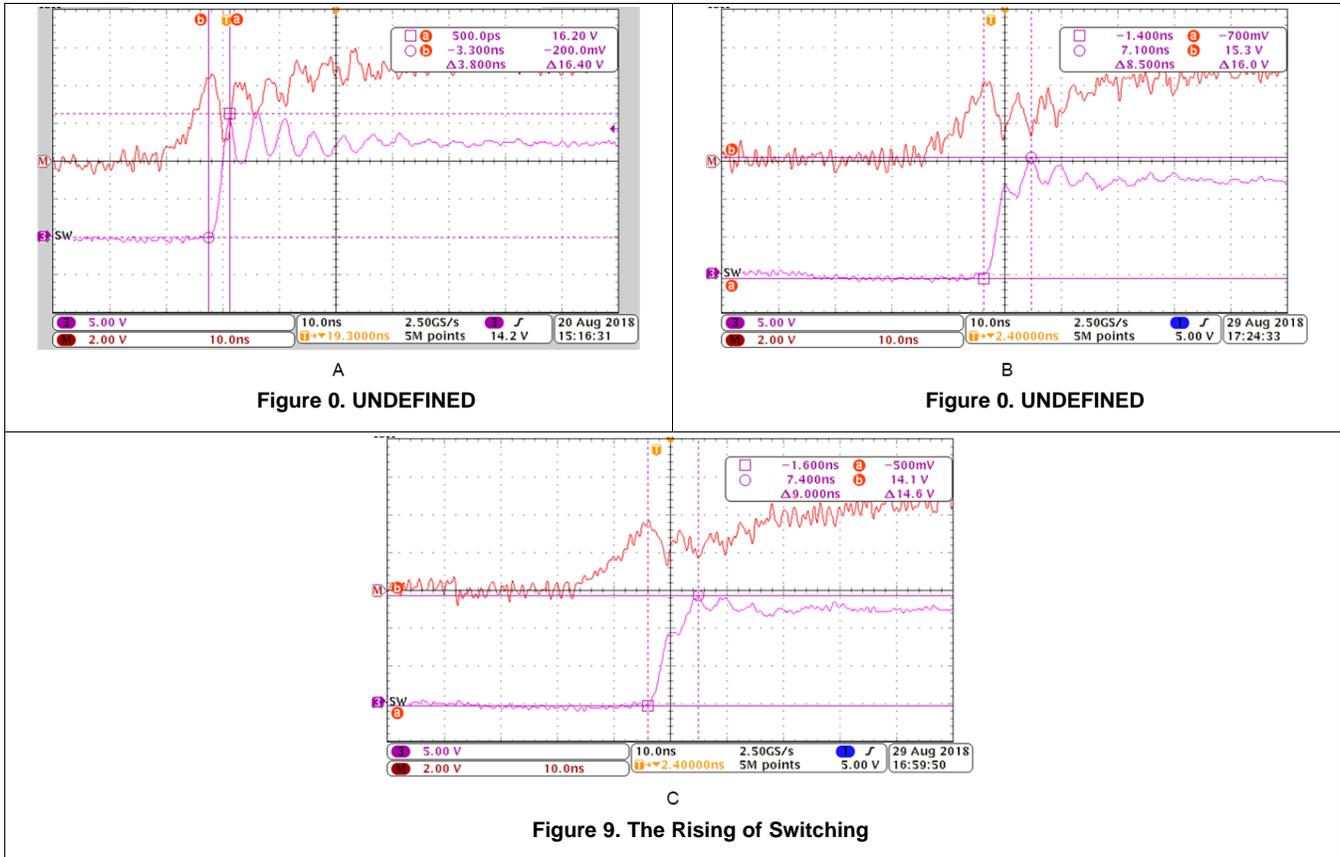


Figure 0. UNDEFINED

Figure 0. UNDEFINED





In [Figure 9](#), the gate resistor is always  $4.7\ \Omega$  and does not change. The bootstrap resistor is  $4.7\ \Omega$  in waveform (A),  $10\ \Omega$  in waveform (B), and  $15\ \Omega$  in waveform (C). In waveform (A), SW overshoot voltage is the biggest at 16.2 V. The slew rate of SW rising is about 4.31 V/ns. The efficiency is 93.7%. In waveform (B), SW overshoot voltage is about 15.3 V and slew rate is about 1.88 V/ns. The efficiency is about 93.6%. In waveform (C), the SW overshoot voltage is about 14.1 V and slew rate is about 1.6 V/ns. The efficiency is about 93.4%. Comparing the three waveforms, a  $10\ \Omega$  bootstrap resistor is better.

Use different types of MOSFET and a smaller  $Q_g$  MOSFET. The driver parameters must be adjusted depending on the MOSFET you use. The key factor is to adjust switching slew rate and SW overshoot to guarantee the safety of IC and MOSFET and efficiency as high as it can.

## 5 Summary

This application report mainly introduces how to adjust driver parameters depending on MOSFET about TPS512xx IC. It does not need a low-side gate resistor to get faster switching of the low-side MOSFET turning on or off. The gate resistor of high-side MOSFET is confirmed by the falling of switching, then the bootstrap resistor is confirmed by the rising of switching.

## 6 References

- Texas Instruments, [Ultra-Low Quiescent \(ULQ\) Dual Synchronous Step-Down Controller with 5 V and 3.3 V LDOs Data Sheet](#)
- Texas Instruments, [Dual Synchronous Step-Down Fixed Output Controller with 5-V and 3.3-V LDOs User's Guide](#)
- Texas Instruments, [Fundamentals of MOSFET and IGBT Gate Driver Circuits Seminar](#)
- Texas Instruments, [CSD87330Q3D Synchronous Buck NexFET Power Block Data Sheet](#)

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (January 2018) to A Revision</b>	<b>Page</b>
• Edited application report for clarity. ....	<b>1</b>

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