Application Report
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Improvements to the UCD90320 Device

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ABSTRACT

The UCD90320 is the highest channel density power sequencer and system monitor device with blackbox logging in the market to replace the UCD90240. This document details the improvements from the UCD90240 to the UCD90320 to give a jump start to migration.

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Trademarks

1 Introduction

The UCD90320 power-supply sequencer and monitor with Advanced Configuration and Power Interface (ACPI) support has the following capabilities:

- Control up to 32 voltage rails (24 analog and eight digital)
- Has built-in blackbox logging
- Ensures correct power sequences during both normal and fault conditions
- Includes a dedicated fault pin to easily cascade multiple devices

They are an upgrade to the UCD90240 (listed as not recommended for new designs [NRND]). This application report addresses some frequently asked questions to give you a jump start.

2 Improvements from the UCD90240 Device

Table 1 lists the improvements from the UCD90240 to the UCD90320 device.

Table 1. Feature Improvements

FEATURES	UCD90240	UCD90320
Package	u*JrBGA ZRB 9xmm	nFBGA ZWS 12-mm×12-mm
Pitch	0.65 mm	0.8 mm
Pin Count	157	169 (Additional 12 ground pins)
Channels	24 (Analog monitor only)	32 (24 analog monitor pins and 8 digital monitor pins
Rail Profile (Each profile includes 9 thresholds: UV_FAULT, OV_FAULT, UV_WARNING, OV_WARNING, POWER_GOOD, POWER_NOT_GOOD, VOUT, MARGIN_HIGH and MARGIN_LOW)	1	4
GPI debugging	No	Yes
Rail State	No	Yes
Flexible IO Remapping	No. EN, PWM, and LGPO pins are dedicated function pins	Yes. The same physical pin can be mux'ed as EN/Margin/LGPO for improved flexibility and increased number of GPI(24->32) and LGPO(12->16) pins
Logic General Purpose Output (LGPO) sequence on/off dependency	No	Yes
Resequencing Mask	No	Yes

3 Package Changes

Significant changes have been adapted on the UCD90320 over the UCD90240 to benefit various applications. Texas instruments produces a laminated-based family of chip select packages (CSPs) known as the New Fine Pitch Ball Grid Array (nFBGA) package. nFBGA packages use solder ally balls as the interconnect between the package substrate and the board on which the package is soldered. This change helps to contract and expand at the same rate as the underneath PCB board and it provides significant improvement on the Board-Level Reliability (BLR) compared to the u*JrBGA used on the UCD90240, especially for thick PCB boards. Moreover, the pitch is enlarged to 0.8 mm which is more much friendly to the PCB layout than the 0.65 mm pitch used on the UCD90240. Due to the large pitch, the footprint of the UCD90320 package is at 12-mm×12-mm, which is slight larger than 9-mm×9-mm of the UCD90240.

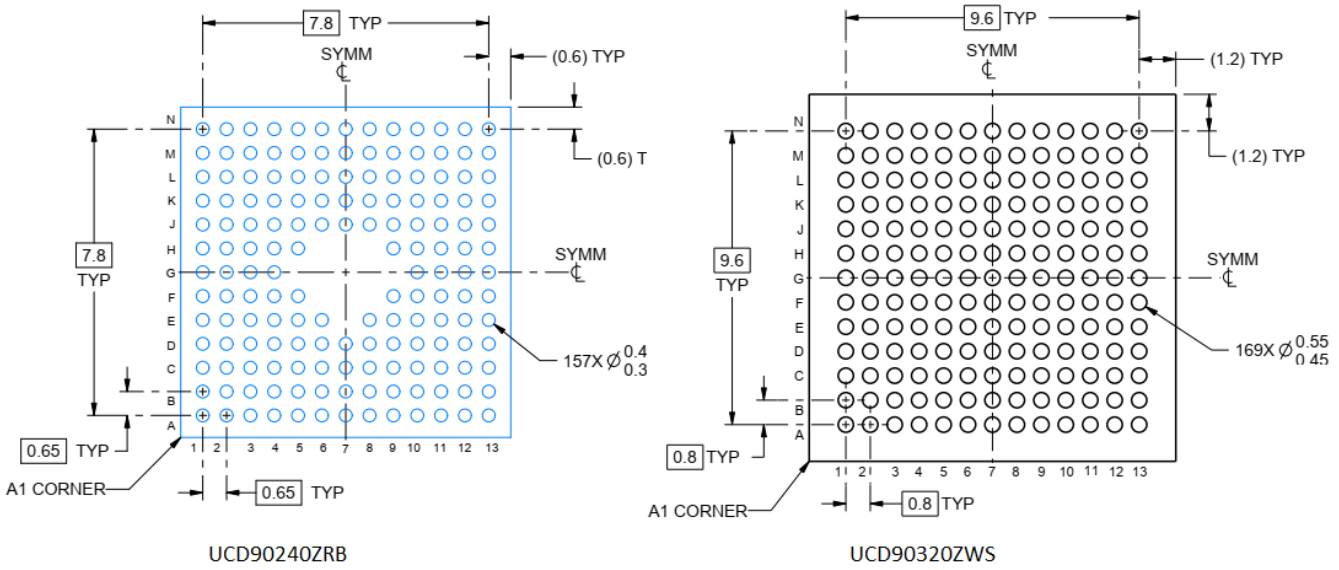

Figure 1. Package Changes

4 IO Remapping

The UCD90320 has flexible IO remapping among a total of 84 IO pins while the UCD90240 pre-allocated these 84 into different function groups. The unused EN/PWM/LGPO pins can be re-configured for the following:

- GPI and commanded GPIO
- System reset
- System watchdog
- Fault pin at the UCD90320

Due to the flexible IO remapping, the UCD90320 supports up to 32 GPI pins and 16 LGPO pins which is an increase of eight and four, respectively from the UCD90240. Applications can also read all of the 84 IO status via PMBus™ command while the UCD90240 only supports the reading status of 24 GPIO pins. Table 2 lists the complete IO mapping.

Table 2. UCD90320 IO Mapping

PIN INDEX	PIN NAME	PIN NUMBER	PURPOSES					
			MARGIN	EN	LGPO	GPI	GPIO	GPI RAIL
0	MAR01(GPIO)	J13	Y	N	N	Y	Y	N
1	MAR02(GPIO)	L5	Y	N	N	Y	Y	N
2	MAR03(GPIO)	D8	Y	N	N	Y	Y	N
3	MAR04(GPIO)	K6	Y	N	N	Y	Y	N
4	MAR05(GPIO)	D4	Y	N	N	Y	Y	N
5	MAR06(GPIO)	E4	Y	N	N	Y	Y	N
6	MAR07(GPIO)	F5	Y	N	N	Y	Y	N
7	MAR08(GPIO)	N5	Y	N	N	Y	Y	N
8	MAR09(GPIO)	N6	Y	N	N	Y	Y	N
9	MAR10(GPIO)	K5	Y	N	N	Y	Y	N
10	MAR11(GPIO)	M6	Y	N	N	Y	Y	N
11	MAR12(GPIO)	L6	Y	N	N	Y	Y	N
12	MAR13(GPIO)	D11	Y	N	N	Y	Y	N

Table 2. UCD90320 IO Mapping (continued)

PIN INDEX	PIN NAME	PIN NUMBER	PURPOSES					
			MARGIN	EN	LGPO	GPI	GPIO	GPI RAIL
13	MAR14(GPIO)	C12	Y	N	N	Y	Y	N
14	MAR15(GPIO)	A13	Y	N	N	Y	Y	N
15	MAR16(GPIO)	B13	Y	N	N	Y	Y	N
16	MAR17(GPIO)	D12	Y	N	N	Y	Y	N
17	MAR18(GPIO)	C13	Y	N	N	Y	Y	N
18	MAR19(GPIO)	E12	Y	N	N	Y	Y	N
19	MAR20(GPIO)	E13	Y	N	N	Y	Y	N
20	MAR21(GPIO)	M13	Y	N	N	Y	Y	N
21	MAR22(GPIO)	L12	Y	N	N	Y	Y	N
22	MAR23(GPIO)	M5	Y	N	N	Y	Y	N
23	MAR24(GPIO)	J12	Y	N	N	Y	Y	N
24	EN1(GPIO)	M9	N	Y	N	Y	Y	N
25	EN2(GPIO)	N9	N	Y	N	Y	Y	N
26	EN3(GPIO)	L10	N	Y	N	Y	Y	N
27	EN4(GPIO)	K10	N	Y	N	Y	Y	N
28	EN5(GPIO)	L9	N	Y	N	Y	Y	N
29	EN6(GPIO)	K9	N	Y	N	Y	Y	N
30	EN7(GPIO)	N8	N	Y	N	Y	Y	N
31	EN8(GPIO)	M8	N	Y	N	Y	Y	N
32	EN9(GPIO)	L8	N	Y	N	Y	Y	N
33	EN10(GPIO)	K8	N	Y	N	Y	Y	N
34	EN11(GPIO)	N7	N	Y	N	Y	Y	N
35	EN12(GPIO)	M7	N	Y	N	Y	Y	N
36	EN13(GPIO)	K7	N	Y	N	Y	Y	N
37	EN14(GPIO)	L7	N	Y	N	Y	Y	N
38	EN15(GPIO)	N4	N	Y	N	Y	Y	N
39	EN16(GPIO)	N3	N	Y	N	Y	Y	N
40	EN17(GPIO)	K3	N	Y	N	Y	Y	N
41	EN18(GPIO)	K4	N	Y	N	Y	Y	N
42	EN19(GPIO)	J4	N	Y	N	Y	Y	N
43	EN20(GPIO)	J2	N	Y	N	Y	Y	N
44	EN21(GPIO)	J3	N	Y	N	Y	Y	N
45	EN22(GPIO)	H4	N	Y	N	Y	Y	N
46	EN23(GPIO)	H3	N	Y	N	Y	Y	N
47	EN24(GPIO)	G4	N	Y	N	Y	Y	N
48	EN25(GPIO)	F13	N	Y	N	Y	Y	N
49	EN26(GPIO)	F12	N	Y	N	Y	Y	N
50	EN27(GPIO)	G11	N	Y	N	Y	Y	N
51	EN28(GPIO)	H10	N	Y	N	Y	Y	N
52	EN29(GPIO)	H13	N	Y	N	Y	Y	N
53	EN30(GPIO)	H12	N	Y	N	Y	Y	N
54	EN31(GPIO)	H11	N	Y	N	Y	Y	N
55	EN32(GPIO)	L13	N	Y	N	Y	Y	N
56	LGPO1(GPIO)	C9	N	N	Y	Y	Y	N
57	LGPO2(GPIO)	B9	N	N	Y	Y	Y	N
58	LGPO3(GPIO)	A9	N	N	Y	Y	Y	N

Table 2. UCD90320 IO Mapping (continued)

PIN INDEX	PIN NAME	PIN NUMBER	PURPOSES					
			MARGIN	EN	LGPO	GPI	GPIO	GPI RAIL
59	LGPO4(GPIO)	C8	N	N	Y	Y	Y	N
60	LGPO5(GPIO)	D5	N	N	Y	Y	Y	N
61	LGPO6(GPIO)	C5	N	N	Y	Y	Y	N
62	LGPO7(GPIO)	C6	N	N	Y	Y	Y	N
63	LGPO8(GPIO)	C4	N	N	Y	Y	Y	N
64	LGPO9(GPIO)	L3	N	N	Y	Y	Y	N
65	LGPO10(GPIO)	M1	N	N	Y	Y	Y	N
66	LGPO11(GPIO)	M2	N	N	Y	Y	Y	N
67	LGPO12(GPIO)	M3	N	N	Y	Y	Y	N
68	LGPO13(GPIO)	L4	N	N	Y	Y	Y	N
69	LGPO14(GPIO)	N1	N	N	Y	Y	Y	N
70	LGPO15(GPIO)	M4	N	N	Y	Y	Y	N
71	LGPO16(GPIO)	N2	N	N	Y	Y	Y	N
72	DMON1(GPIO)	F4	N	N	N	Y	Y	Y
73	DMON2(GPIO)	F3	N	N	N	Y	Y	Y
74	DMON3(GPIO)	G3	N	N	N	Y	Y	Y
75	DMON4(GPIO)	D10	N	N	N	Y	Y	Y
76	DMON5(GPIO)	L11	N	N	N	Y	Y	Y
77	DMON6(GPIO)	N12	N	N	N	Y	Y	Y
78	DMON7(GPIO)	N11	N	N	N	Y	Y	Y
79	DMON8(GPIO)	M11	N	N	N	Y	Y	Y
80	GPI01	B11	N	N	N	Y	Y	N
81	GPI02	B12	N	N	N	Y	Y	N
82	GPI03	C11	N	N	N	Y	Y	N
83	GPI04	A12	N	N	N	Y	Y	N

5 Digital Monitor Rail

The UCD90320 supports up to eight digital monitor rails in addition to the 24 analog rails. The GPI rails are defined as using a GPI pin to monitor the external digital signal, such as POWER_GOOD. The majority functions of the GPI rails are the same as analog voltage rails, such as dependency, timing, timeout, and fault responses. GPI rails do not have all thresholds defined by the rail profile; it is a level monitor. When the input is logical high (3V3), the rail is POWER_GOOD, otherwise the rail is not POWER_GOOD and treated as UNDERVOLTAGE(UV)_FAULT. When the GPI input is changed from logical high to logical low with enable signal asserted, it is treated as a UV fault and this event can shutdown, retry, and resequence rails which is up to how the UV fault response is configured. GPI rails do not support margin function, AVS, and other analog rail related functions. GPI rail cannot co-exist with analog voltage rail in a given rail.

6 Rail Profile

The rail profile is composed of group threshold values defined by the following PMBus commands:

- VOUT_COMMAND
- VOUT_OV_FAULT_LIMIT
- VOUT_OV_WARNING_LIMIT
- VOUT_MARGIN_HIGH
- POWER_GOOD_ON
- VOUT_MARGIN_LOW

- POWER_GOOD_OFF
- VOUT_UV_WARNING_LIMIT
- VOUT_UV_FAULT_LIMIT

In the UCD90240, each voltage monitor rail can only have one profile. This has been changed in the UCD90320. Each voltage monitor rail may have up to four profiles. Applications can switch among the profiles via two assigned GPIs. The advantage of multiple profiles for any given rail is that it allows applications to switch via GPI signals to achieve fast response in comparison with individual PMBus command. Also, a single configuration can support up to four different power requirements for any given system. The rail profile is not available for GPI rails or rails without voltage monitoring.

7 GPI Debugging

The UCD90320 supports GPI debug function, which can be enabled when the assigned GPI is asserted. Under GPI debug, the device does not activate the PMBus ALERT pin for any faults/warnings, respond to any fault responses, or log any faults. This function is mainly designed for the debug purpose and it is not recommended in the final production.

Table 3 lists the faults/warnings that are impacted by debug mode.

Table 3. List of Events Affected by GPI Debug Mode

VOUT_OV_FAULT	TON_MAX	IOUT_UC	SYSTEM_WATCHDOG_TIMEOUT
VOUT_OV_WARNING	TOFF_MAX Warning	OT_FAULT	VOUT_UV_WARNING
VOUT_UV_FAULT	IOUT_OC_FAULT	OT_WARNING	IOUT_OC_WARNING
SEQ_ON_TIMEOUT	SEQ_OFF_TIMEOUT	SLAVE_FAULT	RESEQUENCE_ERROR
All GPI de-asserted			

When the debug mode is on, the rail sequence on and off dependency conditions are ignored. As soon as the sequence on and off timeout is expired, the rails are sequenced on or off accordingly, regardless of the timeout action. If the sequence on and off timeout value is set to 0, the rails are sequenced on or off immediately. The LGPOs affected by these events are back to their original states. The fault pin affected by these events does not pull the fault bus low. It does not log any faults, suspend system watchdog, or ignore the sequencing dependencies for rails.

This feature gives applications options when performing board-level debug or programming to not trigger the PMBus Alert, response fault, or continue the system watchdog.

One GPI pin can be assigned to perform a GPI debugging function. When asserting the assigned GPI, the device is under the GPI debug mode.

8 LGPO Sequencing On and Off Dependency

The UCD90320 supports sequencing dependencies not only over rails and GPIs, but also on LGPOs, which is not available on the UCD90240. If sequencing on and off dependencies on the LGPO is required in the system, the LGPO signal is required to wire back to one of the GPIs under the UCD90240. This approach uses two extra pins which can be an issue for applications that have limited available pins. The LGPO sequencing dependency feature in the UCD90320 can save up to two extra pins for other functions.

9 Rail State

The UCD90320 queries the state of each rail to help customers easily determine the power status of the system. Table 4 lists the nine rail states of the device.

Table 4. Rail State Value Descriptions

RAIL STATE	VALUE	CONDITION FOR ENTERING RAIL STAT
INIT	0	Device out of reset
IDLE	1	When a ON_OFF_CONFIG condition is not met, a rail is shut down due to a fault, or the rail is waiting for the TURNON period to re-sequence
SEQ_ON	2	Wait for the dependency to be met to assert the enable signal.
START_DELAY	3	Wait TON_DELAY to assert the enable signal.
RAMP_UP	4	Enable signal is asserted and rail is approaching the power good threshold. If the power good threshold is set to 0 V, the rail stays at this state even if the monitored voltage is higher than 0 V.
REGULATION	5	The monitoring voltage is higher than the power good threshold when the enable signal is asserted, rails stay at this state even if the voltage is below the power good threshold and continues as long as there is no fault action taken.
SEQ_OFF	6	Wait for the dependency to be met to de-assert the enable signal.
STOP_DELAY	7	Wait for the TOFF_DELAY to de-assert the enable signal.
RAMP_DOWN	8	The enable signal is de-asserted and the rail is ramping down. This state is available only if TOFF_MAX_WARN_LIMIT is not set to unlimited, or if the turn-off sequence is triggered by a fault action. The rail must not be under fault retry sequence to show this RAMP_DOWN state. Otherwise, the IDLE state is present.

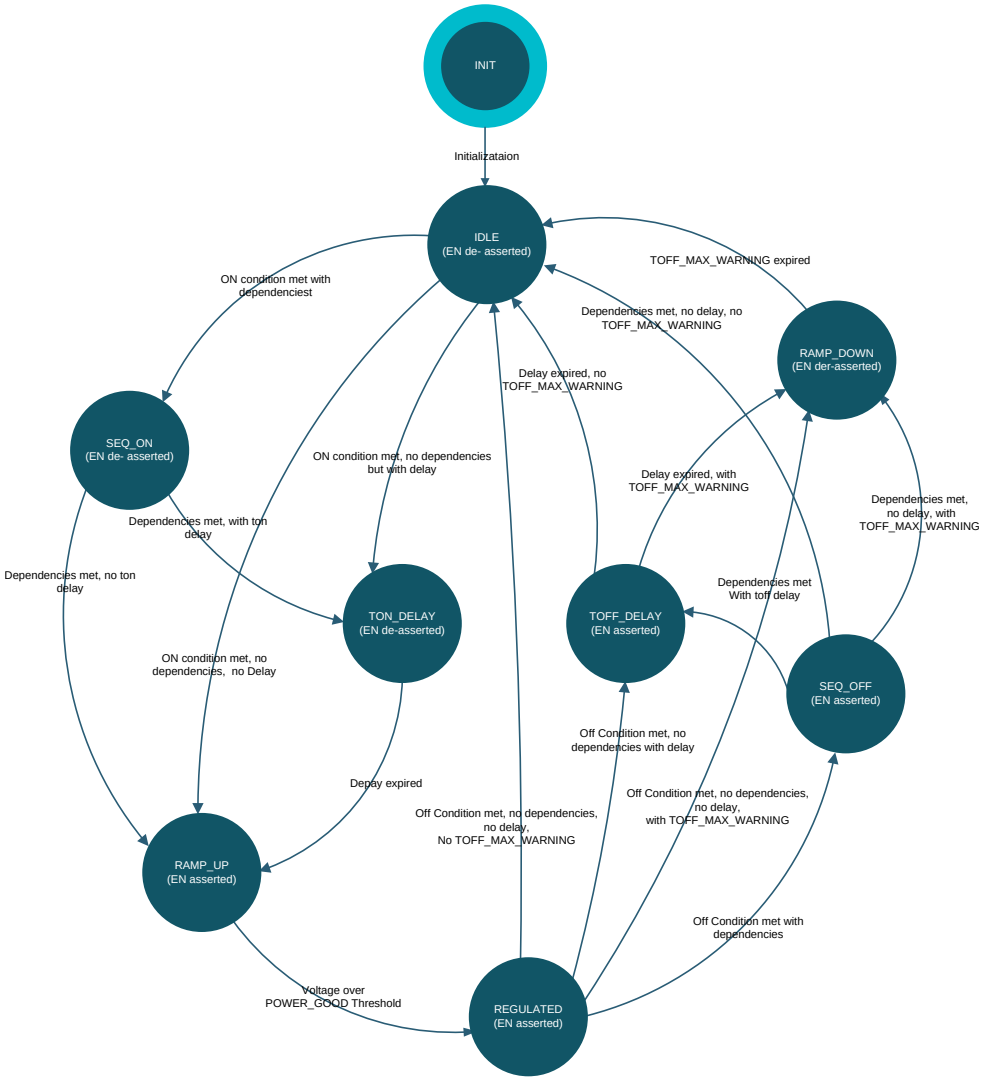

Figure 2. Rail State Machine Diagram

Figure 2 shows how the rail states are changed.

10 Resequencing Rail Mask

The UCD90320 supports resequencing the rail mask which allows devices to ignore the POWER_GOOD_OFF and TOFF_MAX_WARN statuses when performing resequencing. This is a useful feature if the resequencing event is triggered by the rail which is not controlled by the UCD90320. When the corresponding bits are set in the mask, the associated rails are ignored for checking during the resequencing.

11 Migrating from the UCD90240 Device to the UCD90320 Device

As explained in the Section 3, the UCD90320 has a different package footprint from the UCD90240, therefore, schematic changes are required. Moreover, because of the new features introduced for the UCD90320, all files generated based on the UCD90240, such as the project file (.xml), system file (.tisfs), data flash file (.hex), and script file (.csv) are not compatible with the UCD90320. Applications have to re-generate these files. The migration generates new schematics and configuration file.

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