Application Note

How the Switching Frequency Affects the Performance of Buck Converter

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ABSTRACT

The buck converter uses an inherent switching action to regulate voltage. This switching frequency can affect the performance of a buck converter, and is thus very important. This application report analyzes the influence of switching frequency on buck converter performance in terms of efficiency, thermals, ripple, and transient response. It also shows bench test results at both 600-kHz and 1000-kHz using the TPS568230[1].

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1 Introduction

The system under consideration is a typical buck SMPS circuit with D-CAP3™ control mode. There are many specific requirements in application. To realize a better performance, it is important to know the role of switching frequency in the power system. This application report analyzes the major power loss, output voltage ripple, and transient response and shows the solution size of different frequency at the end.

2 Power Loss

Switching frequency can be an important factor on power loss for a buck converter. Three dominant power losses are identified as: switching loss, conduction loss, and driver loss. This section provides the brief formula based on buck converter.

2.1 Switching Loss

Switching losses are associated with the transition of the switch from its on-state to off-state, and back. Figure 2-1 is a complete switching process with regards to inductive load. It shows drain current and drain voltage with respect to time. T_{cross} by definition is the time for both the voltage and the current to complete their transients[2].

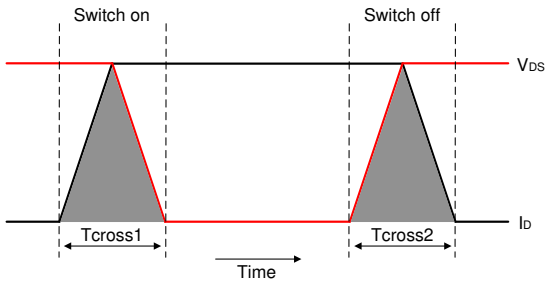

Figure 2-1. The Voltage and Current Waveform When Switching an Inductive Load

As shown in Figure 2-1, the area enclosed by the voltage, current, and time axis is the power loss of MOSFET during the transition. The power loss in single cycle is derived in Equation 1.

$$E = 2 \times \int_0^{t_{cross}} V\left(t\right) I\left(t\right) dt = V_{DSmax} \times I_{Dmax} \times t_{cross} \quad (1)$$

where

- V_{DSmax} is the voltage across the switch (when it is OFF)
- I_{Dmax} is the current through it (when it is ON)
- t_{cross} is the crossover time during turn-on and turn-off, respectively

The buck converter has a filter inductor in the output side, so it meets the switching loss equation above. Equation 2 shows the inductive switching loss when switching repetitively. The higher the switching frequency, the greater the number of times the switch changes state per second, therefore, these losses are proportional to the switching frequency.

$$P = V_{in} \times I_{Dmax} \times t_{cross} \times f_{sw} \quad (2)$$

where

- V_{in} is the input voltage
- f_{sw} is the switching frequency

2.2 Conduction Loss

In modern power conversion, though the V × I losses are much closer to the ideal or the value of zero when the switch is off, there are considerable losses when the switch is on, and that is due to the presence of on-resistance of MOSFET. This particular loss term is clearly the conduction loss.

The conduction loss coincides with the interval in which power is being processed in the converter. Unlike the switching loss, the conduction loss is not frequency-dependent. It does depend on duty-cycle. Equation 3 shows the conduction loss of a MOSFET.

$$P = I_{RMS}^2 \times R_{DS} \quad (3)$$

where

- I_{RMS} is the RMS of the switching current
- R_{DS} is the on-resistance of the MOSFET

The diode conduction loss is the other major conduction loss term in the buck converter. It is equal to $V_D \times I_{D\_AVG}$, where V_D is the diode forward-drop. I_{D_AVG} is the average current through the diode which is equal to $I_O \times (1\text{-}D)$ for the buck converter. It is also frequency-independent.

2.3 Driver Loss

The switching process of MOSFET is always accompanied by the charge and discharge of the interelectrode capacitances. By controlling the gate voltage of the driving terminal and then controlling the switching of the MOSFET, driver loss occurs during this process, as follows:

$$P = V_{drive} \times Q_g \times f_{sw} \quad (4)$$

where

- V_{drive} is the gate drive voltage
- Q_g is the gate charge factor

Q_g is related to the effective input capacitance and gate drive voltage. Equation 4 shows the driver loss is also proportional to the switching frequency.

2.4 Test Results

The efficiency and thermal performance are two important features in real applications. As can be seen from the above analysis, the switching loss and driver loss are directly affected by switching frequency. Table 2-1 lists the test parameters using the *TPS568230* device. The TPS568230 has a MODE pin which can set up three different modes of operation for light load running and 600 kHz/800 kHz/1 MHz switching frequency at heavy load. The light load operation in this paper are all select Eco-mode™.

Table 2-1. TPS568230 Test Parameters

Fsw/kHz	Vin/V	Vout/V	L/µH	DCR/mΩ	Cin/µF	Cout/µF
600	12	1	0.68	4.7	44	88
1000	12	1	0.47	3.8	22	44

Based on the test condition in Table 2-1, Figure 2-2 shows the efficiency comparison with loading range from 1 mA to 8 A. Figure 2-3 and Figure 2-4 show the thermal comparison results with 8 A loading. It can be concluded that due to the difference of switching loss and driver loss, there is different efficiency and thermal performance in the two frequency conditions. It has higher efficiency and a better thermal result when set to 600 kHz switching frequency.

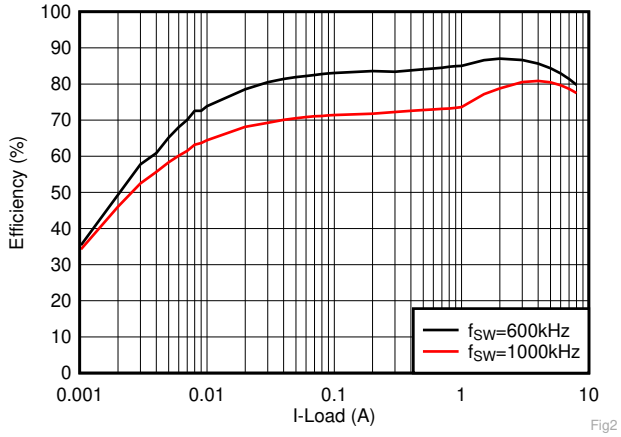

Figure 2-2. Efficiency Comparison Data

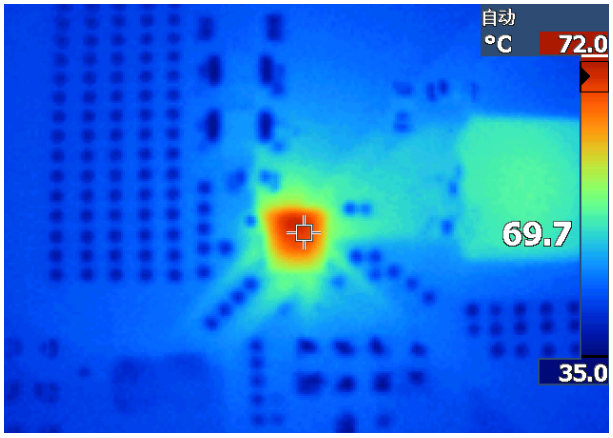

Figure 2-3. Thermal, F_{SW} = 600 kHz

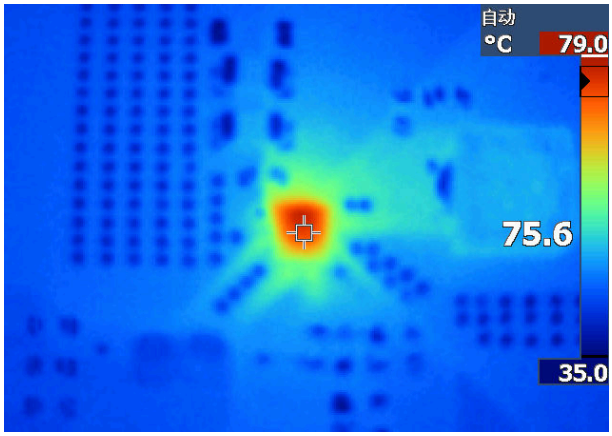

Figure 2-4. Thermal, F_{SW} = 1000 kHz

3 Output Ripple

The buck converter has an inherent switching action, which causes the currents and voltages in the circuit to fluctuate. The output voltage also has ripple on top of the regulated steady-state DC value. Designers of power systems consider the output voltage ripple to be a key parameter for design considerations. This section presents a brief formula for the output voltage ripple and an analysis the relationship with switching frequency.

The switching action of the synchronized MOSFET causes the current in the inductor to have a triangular waveform. The DC component of the inductor current flows through the output load, and the AC portion of the inductor flow through the output capacitor, as shown in Figure 3-1. The time-varying current through the capacitor causes the voltage across the capacitor to be perturbed[3].

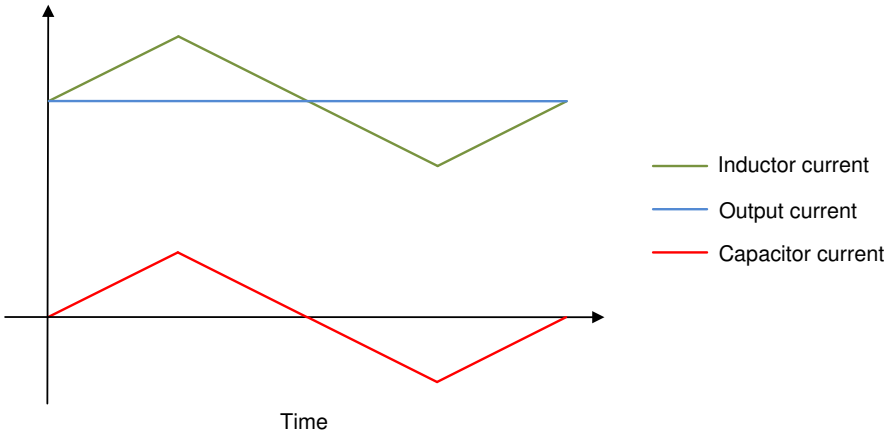

Figure 3-1. Current in the Buck Converter

The D-CAP3 mode control technology allows the use of ceramic output capacitors with low ESR. The *Output Ripple Voltage for Buck Switching Regulator Application Report* (SLVA630) presents an accurate, yet easy-to-implement, formula for the output voltage ripple under low ESR condition. At light load condition, the converter operates in power skip mode (PSM) and the output voltage ripple is dependent on the output capacitor and inductor value. A larger output capacitor and inductor values minimize the voltage ripple in PSM mode. At heavy load conditions, the device operates in PWM mode. Since ceramic capacitors have extremely low ESR and relatively little capacitance, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$V_{ripple} = \frac{I_{ripple}}{8Cf_{sw}} + \frac{I_{ripple}R^2C}{2} \times \frac{f_{sw}}{D(1-D)} \quad (5)$$

Noting that:

$$I_{ripple} = V_{out} \times \frac{1-D}{L \times f_{sw}} \quad (6)$$

where

- I_{ripple} is the inductor current ripple
- C is the capacitance of the output capacitor
- R is the equivalent series resistance (ESR) of the output capacitor
- D is the duty cycle of switching
- V_{out} is the output voltage

For quick calculation, a simpler model of output voltage ripple is assumed. The total output ripple is the linear sum of the voltage ripple due to the capacitor alone and the voltage ripple due to resistor alone:

$$V_{ripple} = \frac{I_{ripple}}{8Cf_{sw}} + I_{ripple}R \quad (7)$$

Equation 6 and Equation 7 reveal that the total output ripple is mainly affected by duty cycle, output capacitor, and inductor. Another important factor is switching frequency. Higher frequency is of great benefit for reducing output voltage ripple. Based on the parameters in Table 2-1, Figure 3-2, and Figure 3-3 show the ripple test results with 8 A loading. The ripple is 11 mV under 600 kHz and 10 mV under 1000 kHz. The ripple becomes smaller even though using the output power stage (LC) with smaller inductance and capacitance increases the switching frequency.

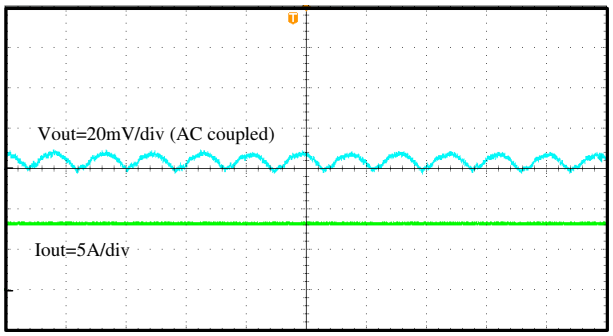

Figure 3-2. Output Voltage Ripple, F_{SW} = 600 kHz

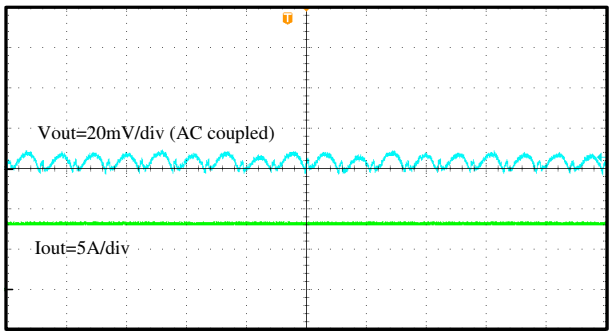

Figure 3-3. Output Voltage Ripple, F_{SW} = 1000 kHz

4 Transient Response

The load transient is stringent in some high-end. The D-CAP3 transient response is very quick and output transients are usually small. There are two key elements that may influence load transient. One element is the load step size and the transient slew rate. The other elements are output capacitor/inductor and switching frequency. The output LC should be designed to meet the transient requirement. Figure 4-1 shows how D-CAP3 topology works in a load transient case[4].

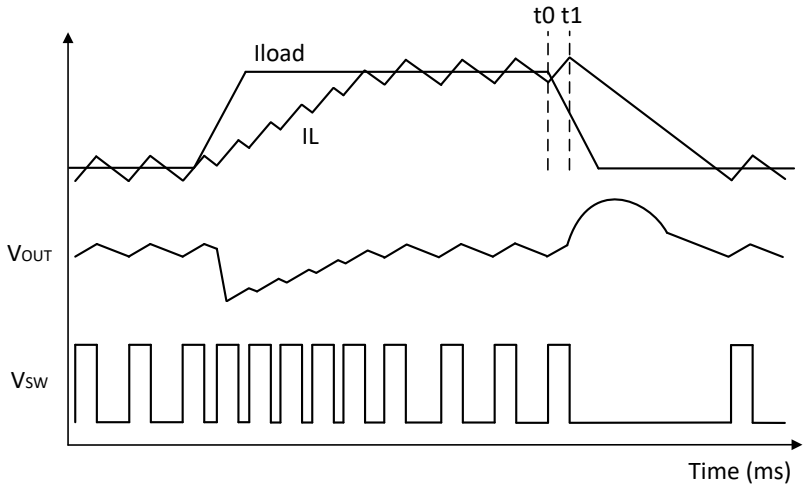

Figure 4-1. Load Transient Response of D-CAP3 Converter

During load step-up: The D-CAP3-based converter reacts with reducing off-time response until the minimum off time is reached while maintaining the constant on time as shown in Figure 4-1. It takes a relatively shorter time for the inductor to catch up the load step due to the absence of the error amplifier. The output undershoot is mainly impacted by loop response time, output inductance, capacitance, and minimum off time.

During load step-down: The converter stops switching when the output voltage becomes bigger than the reference voltage. There could be some delay from load release to non-switching due to the onset of the on-time timer. t0–t1 in Figure 4-1 shows the delay period. Two delays are commonly found in D-CAP3 control: one is the comparator delay and the other is on time delay. In any D-CAP3 control, the on time is always constant. If the load release occurs during the very beginning of the on time, the on time must complete its pre-programmed duration before being turned off. The worst-case delay could be expected to be 1 × Ton as Ton = D × 1 / fsw. The delay time directly affects the energy delivered to the output capacitor so the output overshoot is mainly dominated by output inductor/capacitor and constant on time. The higher the frequency, the shorter the Ton, which is good for overshoot.

Figure 4-2 and Figure 4-3 show the load transient test results under the condition in Table 2-1. Load transient from 0.8 A to 7.2 A with a 2.5 A/µs slew rate. The overshoot/undershoot are 35 mV/-27 mV under 600 kHz and 25 mV/-15 mV under 1000 kHz. The undershoot of 1000 kHz is better even through using a smaller output

capacitor. Because the loop response speed of 1000 kHz mode is faster than 600 kHz mode since the smaller output inductor and capacitor can be used in higher frequency. Besides, the overshoot under 1 MHz is better than 600 kHz as the Ton is relatively shorter when 1000 kHz mode is selected.

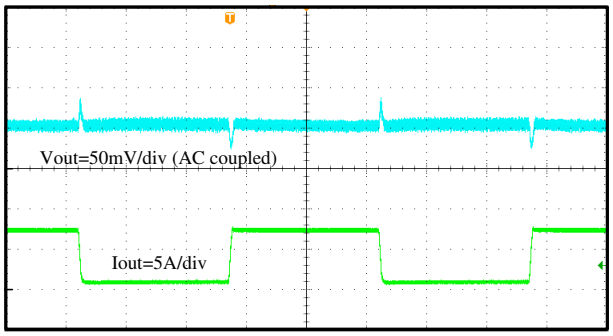

Figure 4-2. Load Transient, F_{SW} = 600 kHz

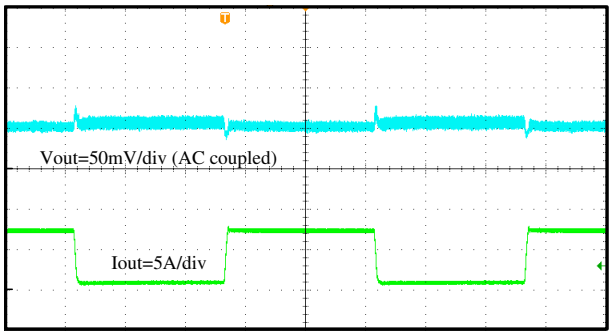

Figure 4-3. Load Transient, F_{SW} = 1000 kHz

5 PCB Layout

With the higher switching frequency set, the engineer can choose a smaller filter inductor and less output capacitor. Besides, a higher switching frequency is helpful for the voltage ripple of input side, so the input capacitor can also be reduced. The PCB solution size becomes smaller to achieve more flexible applications. Based on the parameters in Table 2-1, Figure 5-1 shows the PCB solution under 600 kHz. Figure 5-2 shows the PCB solution under 1000 kHz. The solution size shrinks by about 30% of 1000 kHz application compared to 600 kHz application.

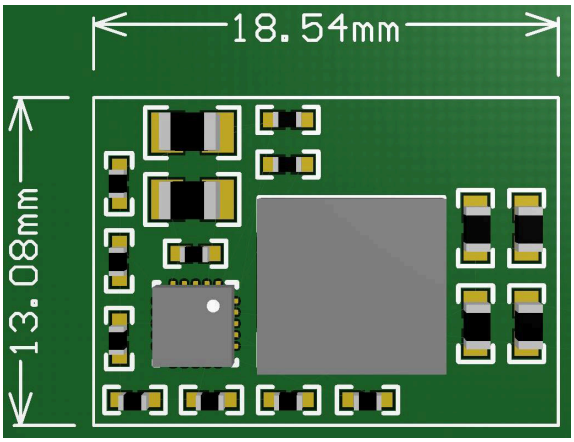

Figure 5-1. PCB Solution, F_{SW} = 600 kHz

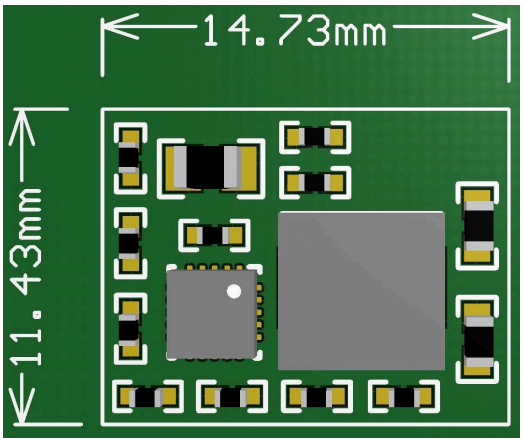

Figure 5-2. PCB Solution, F_{SW} = 1000 kHz

6 Conclusion

This application note analyzes the effect of switching frequency on the performance of buck converter. The higher the switching frequency, the smaller inductor and capacitor are needed, and a better dynamic performance can be achieved while it decreases the efficiency with the increase of switching frequency.

Table 6-1 summarizes the bench test results at both 600-kHz and 1000-kHz using the TPS568230. The device under 1000kHz mode can be paired with a smaller filter inductor and output capacitor. It can improve the ripple and load transient performance in this condition. With the increase of power loss under 1000kHz mode, the efficiency becomes lower then 600kHz mode. There is a trade-off between dynamic performance and efficiency. The engineer can choose 600kHz mode if they care more about efficiency, otherwise, 1000kHz mode is a better choice to achieve better dynamic performance.

Table 6-1. TPS568230 Bench Test Results under 600kHz and 1000kHz

Fsw/kHz	Efficiency AT 8 A	Thermal/°C AT 8 A	Ripple/mV	Overshoot/Undershoot/mV	Design Size/mm²
600	80.01%	72	11	35 / -27	242
1000	77.48%	79	10	25 / -15	168

7 References

1. Texas Instruments, *TPS568230 4.5-V to 18-V Input, 8-A Synchronous Step-Down Voltage Regulator*, data sheet.
2. Sanjaya Maniktala, *Switching Power Supplies A-Z, 2E*
3. Texas Instruments, *Output Ripple Voltage for Buck Switching Regulator*, application note.
4. Texas Instruments, *Calculating Output Capacitance to Meet Transient and Ripple Requirements of an Integrated POL Converter Design Based on D-CAPx™ Modulators*, application note.

8 Revision History

Changes from Revision * (July 2019) to Revision A (April 2014)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated table design size	8

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