Application Report
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Power Switch Fault Glitch Solution During Power Up

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ABSTRACT

The Fault open-drain output of power switch is usually connected to MCU as an indicator when an over-current or over temperature condition is encountered. However, in some cases, as input of power switch powers up fast, momentary false fault asserts that may lead to the MCU operating incorrectly.

It is suggested to use the software method such as controlling the MCU to avoid the fault glitch. This application report also displays one work around to avoid this false fault signal transferring to MCU. The document is applicable for TPS25221, TPS2065C/D, and TPS2059C/D.

Contents

1 Introduction 2
2 Root cause of False Fault Glitch 3
3 Solution for the Fault Glitch 3
4 Summary 5

List of Figures

1 Bench Set-Up 2
2 Fault Glitch as Ramp V_{IN} at 6 V/ms 2
3 Simplified Internal Circuit Between IN Pin and Fault Pin 3
4 Solution for Fault Glitch 3
5 Without RC Filter Waveform, 5 V/ms 4
6 With RC Filter Waveform, 5 V/ms 4
7 Fault Signal Behavior as V_{in} Power up in Current Limit Condition 4
8 Fault Signal Behavior as Current Limit 4

List of Tables

1 Recommended Operating Condition of Input Voltage in TPS2065C/D and TPS2069C/D Data Sheet 2

Trademarks

1 Introduction

The power-distribution switch family is intended for applications such as USB where heavy capacitive loads and short circuits are likely to be encountered. Device features include enable, reverse blocking when disabled, output discharge pulling down, over-current protection, over temperature protection, and de-glitch fault reporting.

The open-drain output fault signal asserts as over current and over temperature conditions encountered with about 9 ms de-glitch time.

However, as the device is powered up in a fast slew rate, the fault signal falsely asserts that lead to the incorrect operation of the System-on-Chip (SoC). Figure 1 shows the set-up of the bench and ramp V_{IN} at 6 V/ms slew rate. Figure 2 shows the fault will have a glitch as V_{IN} ramp to about 1 V, which is far from the recommended operation range from 4.5 V to 5.5 V. Table 1 is the recommended operating condition of V_{IN}.

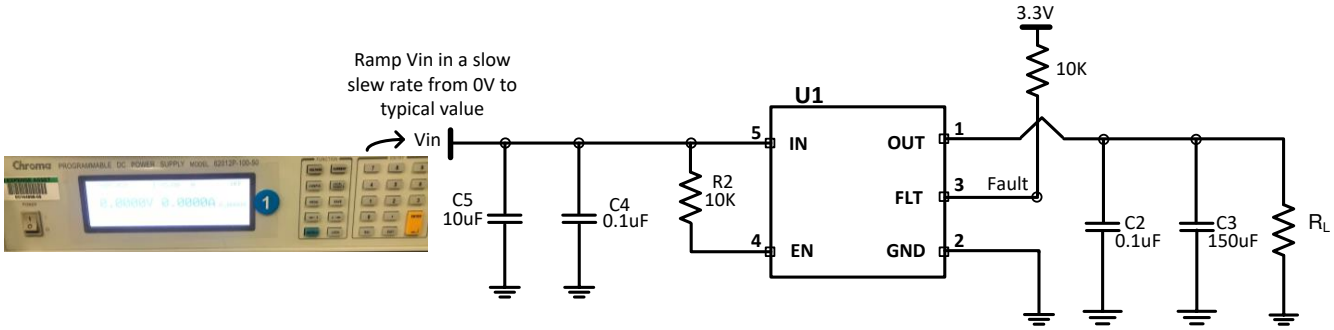

Figure 1. Bench Set-Up

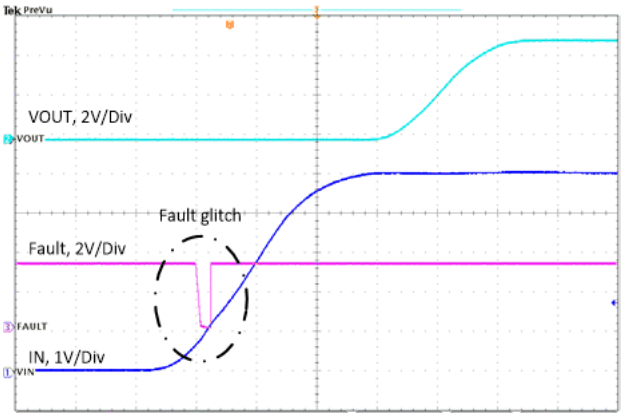

Figure 2. Fault Glitch as Ramp V_{IN} at 6 V/ms

Table 1. Recommended Operating Condition of Input Voltage in TPS2065C/D and TPS2069C/D Data Sheet

	MIN	MAX	UNIT
VIN Input voltage, IN	4.5	5.5	V

The following section discusses the root cause of this phenomenon and the solve method of this concern.

2 Root cause of False Fault Glitch

The following process occurs as V_{IN} ramps fast from 0 V to the recommended operation range:

- Before V_{IN} reach to UVLO threshold to start reset, the internal circuit status is unknown.
- If V_{IN} ramps pretty fast, the voltage on point B maybe coupled through C1.
- If the voltage on point B is larger than the threshold voltage V_{th}, T3 may pull down the FAULT pin.
- The whole circuit resumes to normal after the internal reset.

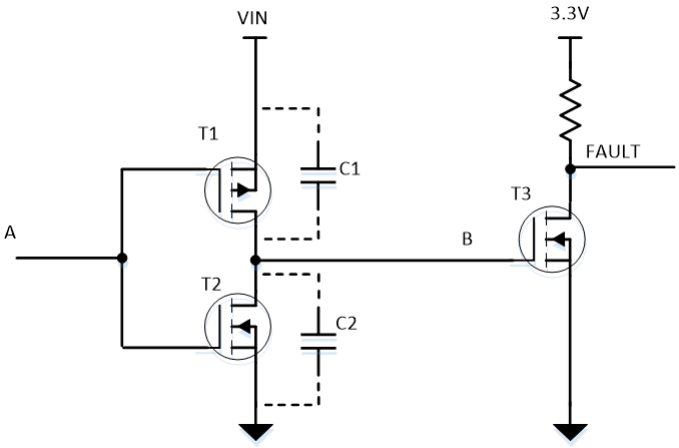

Figure 3. Simplified Internal Circuit Between IN Pin and Fault Pin

Due to the unknown status of the gate of T3, the Fault pin has the chance to be pulled down to 0 V.

3 Solution for the Fault Glitch

3.1 With RC Filter to Eliminate Fault Glitch as Start-Up

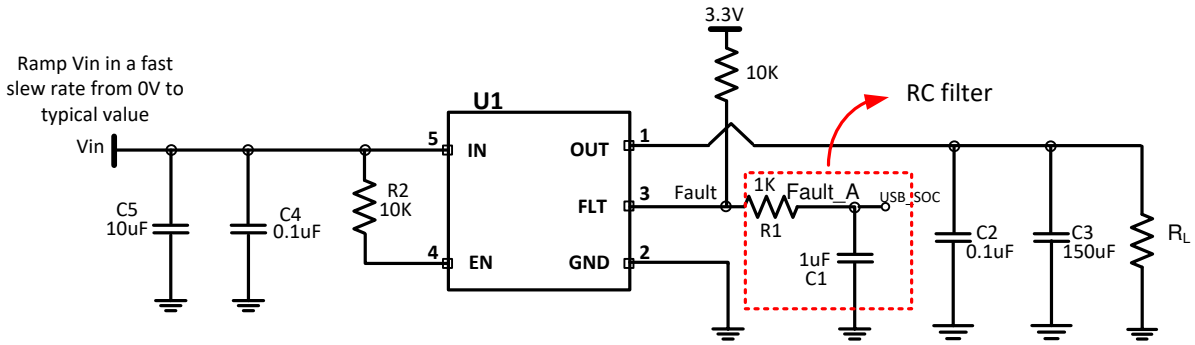

Figure 4. Solution for Fault Glitch

Adding the RC filter between the Fault and MCU to eliminate the glitch.

Since point B from Figure 3 is in unknown status until V_{IN} reaches UVLO (4 V, the worst case in TPS2065D or TPS2069D). The worst case for Fault low is from V_{in} = V_{th} to V_{in} reach UVLO.

If V_{in} = 5 V, and V_{IN} ramp = V_{ramp} V/ms, the worst Fault low period T_{FAULT_L} = (UVLO - V_{th}) / V_{ramp}. You need Fault_A to be > V_{FAULT_H} (1.7 V) during T_{FAULT_L}. V_{FAULTd_H} according to the customer's definition. Before power on, the initial voltage on C1 is 3.3 V. Before V_{in} reaches the UVLO voltage threshold, the voltage on C1 discharges through the FLT pin to GND.

Select RC value to make sure:

$$V_{Fault\_A} = 3.3\,V \times e^{\frac{-T_{FAULT\_L}}{RC}} > 1.7\,V \quad (1)$$

If V_{ramp} = 5 V/ms, then T_{FAULT_L} = 0.6 ms, select R = 1kΩ, C=1 µF.

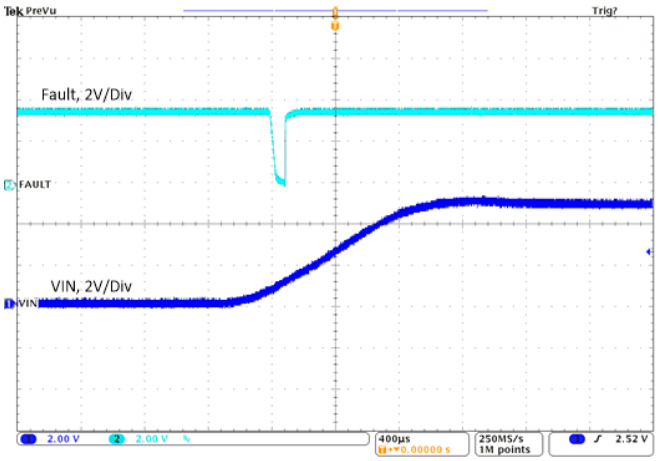

Figure 5. Without RC Filter Waveform, 5 V/ms

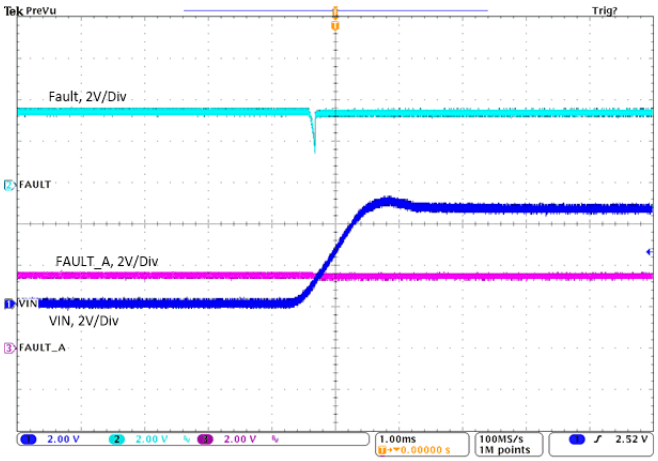

Figure 6. With RC Filter Waveform, 5 V/ms

As seen in Figure 5, without the RC filter added, the Fault pin is pulled down to 0 V. The duration time depends on the slew rate of input. Figure 6 displays that with the RC filter added, although the Fault pin has a glitch, the terminal Fault_A that is connected to MCU almost has no glitches, always high level. The method proposed can eliminate the fault glitch concern.

3.2 Validate the Influence of RC Filter to Normal Operation

In order to validate whether the method proposed has some impact on the IC's normal operation, the delay time of added RC filter is verified. The following bench has been set up.

V_{in} = 5 V, slew rate is 5V/ms. With RC filter added, the parameters are R1 =1kΩ and C1 = 1 µF. RLoad = 2.5 Ω, current limit = 1.55A in TPS2065D. In theory, Fault_A from 3.3 V to 0.7 V, the time is 1.55 ms. In general, 0.7 V is regarded as low level of fault signal.

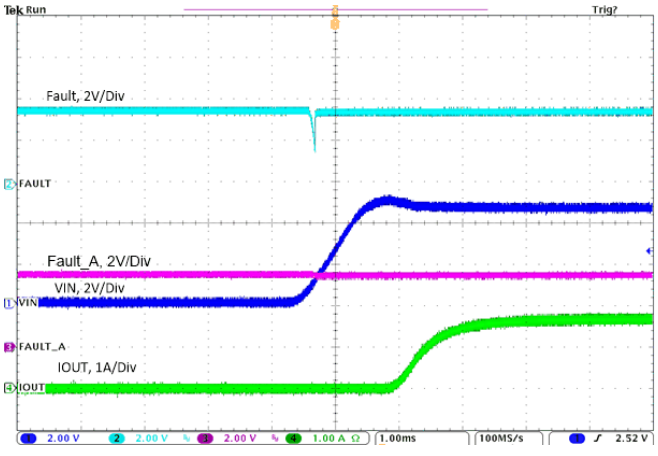

Figure 7. Fault Signal Behavior as V_{in} Power up in Current Limit Condition

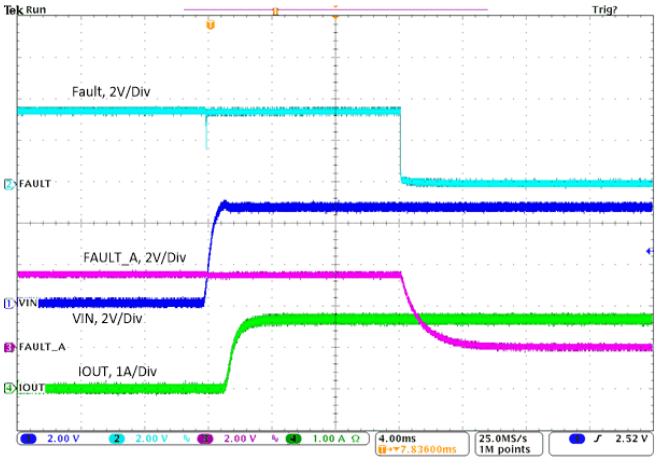

Figure 8. Fault Signal Behavior as Current Limit

In Figure 7, as V_{in} ramps fast in the current limit condition, the Fault pin will glitch from 3.3 V to 1.4 V. However, the Fault_A that is connected to MCU almost has no glitch. Figure 8 indicates that in current limit condition, the Fault_A can also assert normally, but with a delay time about 1.55 ms. The results are in coincidence with theoretical calculation.

4 Summary

The RC filter workaround can help solve the power switch fault glitch issue during V_{in} startup. The workaround will cause a delay on normal fault condition. The delay duration depends on the RC value. Comparing with internal fault glitch time, 8-9 ms, the 1.55 ms delay time is relatively less impact and can be compromised.

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