Application Report
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Generating Negative and Positive Voltage Rail With Boost Converter TLV61048

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ABSTRACT

Many applications require negative and positive voltage rails to power the amplifiers from a 3.3-V or 5-V power supply. Taking the TLV61048 device as an example, this document demonstrates a simple, cost-effective boost converter and discrete charge pump circuit to generate ±12-V voltage rails.

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Trademarks

1 Introduction

The application report first introduces the operating principle of the discrete charge pump circuit to generate negative voltage based on boost converter. Then the report derives formulas to calculate the external component values of the charge pump circuit. Finally, the TLV61048 device is used as example to verify the circuit designed in the lab.

2 Operating Principle

A typical boost circuit for 3.3-V input, 12-V output based on the TLV61048 device is shown in Figure 1. The TLV61048 device is a peak-current-control boost converter IC which integrates a power switch with current limit up to 3.7 A. The switching frequency can be configured through the FRE pin. If the FRE pin is connected to GND, the switching frequency of the device is 1 MHz.

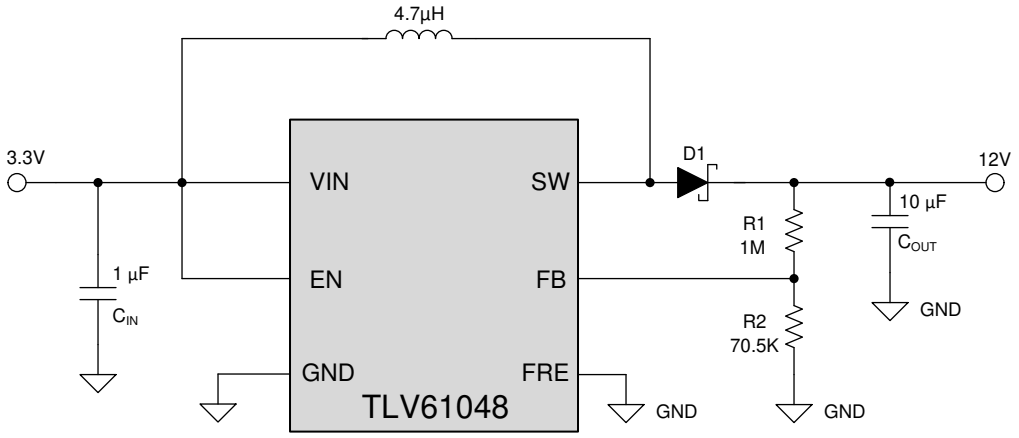

Figure 1. TLV61048 Boost Converter Schematic

Figure 2 shows the operating waveform at 100-mA loading. The integrated power N-MOSFET switches on and off to regulate the output voltage, which is set by R1 and R2.

- During T_{ON}, the internal low-side FET is on. The SW pin voltage is zero and inductor current lineally increases. The output voltage is sustained by the output capacitor.
- During T_{OFF}, the internal N-MOSFET is off. The inductor flows through the Schottky diode D1 to charge the output capacitor.

The sum of T_{ON} and T_{OFF} is the switching cycle T_{SW}, approximately 1 µs. The device operates at Continue Conductive Mode (CCM) in Figure 2, as the inductor current is always higher than zero.

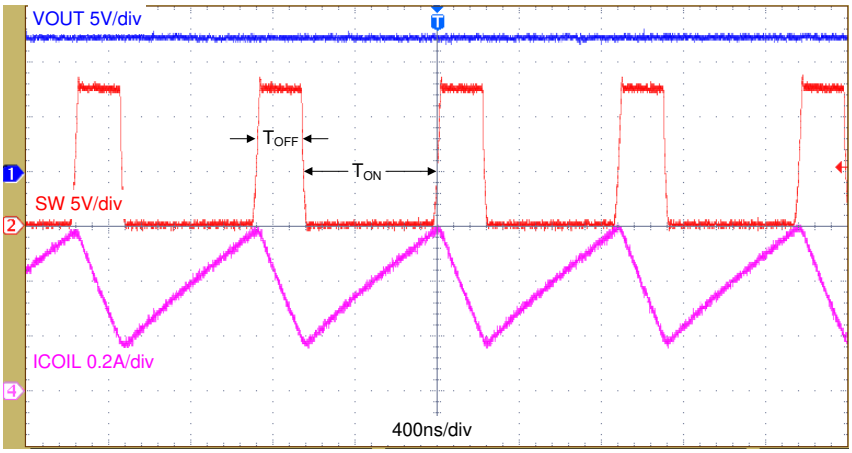

Figure 2. Operating Waveform at 100-mA Loading

At CCM, the duty cycle can be calculated using Equation 1:

$$D = 1 - \frac{\eta \times V_{IN}}{V_{OUT}} \quad (1)$$

where:

- η is the efficiency
- V_{IN} is the input voltage of the boost converter
- V_{OUT} is the output voltage of the boost

The power components of the typical boost converter with discrete circuit to generate a negative voltage is shown in Figure 3. The positive rail is V_{OUT1}, while the negative voltage rail is V_{OUT2}. The external components for negative voltage rail comprise of a resistor R_{CHG}, and a capacitor C_{CHG} and two diodes, D2 and D3.

- During T_{OFF}, the fly capacitor C_{CHG} is charged to SW pin voltage through the R_{CHG} and D2.
- During T_{ON}, the energy of the C_{CHG} flows into the C_{OUT2} through R_{CHG} and D3.

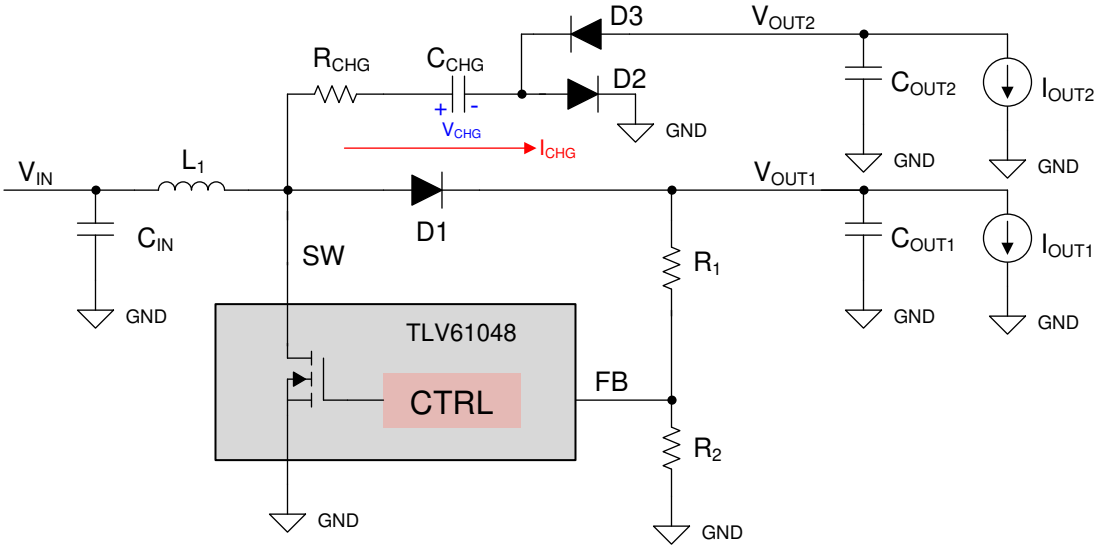

Figure 3. Boost With Discrete Charge Pump Circuit

Figure 4 shows the simplified operating waveform of the circuit, where:

- V_{SW} is the SW pin voltage waveform at CCM
- I_{COIL} is the inductor current
- I_{CHG} is the current through the C_{CHG}
- V_{CHG} is the voltage across the C_{CHG}

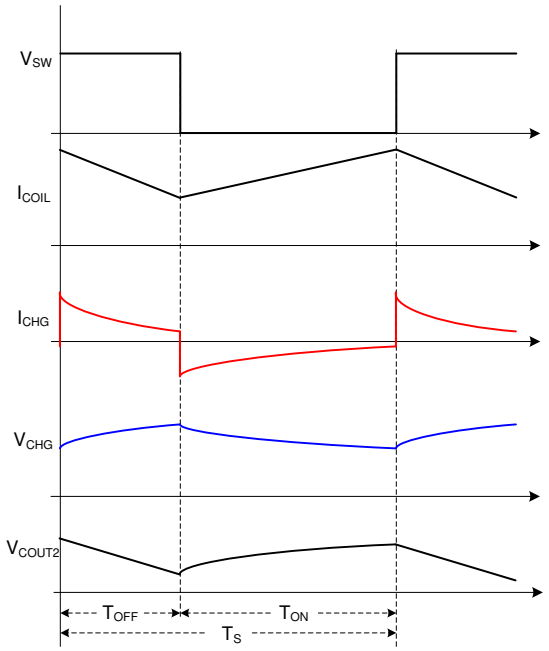

Figure 4. Simplified Operating Waveform

3 External Components Calculation

At stable condition, the average current through the C_{CHG} and C_{OUT2} within one switching cycle must be zero. Thus the average current of I_{CHG} during T_{ON} is defined by Equation 2.

$$I_{CHG1} = \frac{T_S}{T_{ON}} \times I_{OUT2} = \frac{1}{D} \times I_{OUT2} \tag{2}$$

The average current through C_{CHG} during T_{OFF} can be calculated by Equation 3 .

$$I_{CHG2} = \frac{T_{ON}}{T_{OFF}} \times I_{CHG1} = \frac{1}{1-D} \times I_{OUT2} \tag{3}$$

From Equation 2 and Equation 3, the voltage ripple of the C_{CHG} can be calculated with Equation 4.

$$\Delta V_{CHG} = I_{CHG1} \times \frac{1}{C_{CHG}} \times T_{ON} = \frac{I_{OUT2}}{C_{CHG}} \times T_{SW} \tag{4}$$

As all the energy of the C_{OUT2} is provided by during C_{CHG} during T_{ON}, the C_{CHG} voltage reaches valley and V_{OUT2} reaches peak at the end of T_{ON}. The waveform in Figure 4 demonstrates this behavior. This means that the voltage ripple of the C_{CHG} would impact the voltage level of the V_{OUT2}. So C_{CHG} voltage ripple should be set to typical 1% of its DC voltage.

The DC voltage of the C_{CHG} can be calculated with Equation 5. Ignoring the voltage drops of the R_{CHG}, the V_{CHG} is equal to V_{OUT1}.

$$V_{CHG} = (V_{OUT1} + V_{D1}) - I_{CHG2} \times R_{CHG} - V_{D2}$$

where:

- V_{OUT1} is positive rail voltage set by the feedback resistor
- V_{D1} is forward voltage of D1.
- I_{CHG1} is the average current during T_{OFF}
- V_{D2} is the forward voltage of D2

(5)

The voltage ripple of the C_{OUT2} is defined by Equation 6. The output voltage ripple can also be set to 1% of its DC voltage.

$$\Delta V_{COUT2} = I_{OUT2} \times \frac{1}{C_{OUT2}} \times (1-D) \times T_{SW} \tag{6}$$

The DC voltage of C_{OUT2} can be estimated through Equation 7, closed to (V_{OUT1} – 0.3) if ignoring the R_{CHG} voltage drop.

$$-V_{COUT2} = V_{CHG} - I_{CHG1} \times R_{CHG} - V_{D3} = (V_{OUT1} + V_{D1}) - (V_{CHG1} + I_{CHG2}) \times R_{CHG} - 2 \times V_{D2}$$

where:

- V_{CHG} is DC voltage of the C_{CHG}
- V_{D3} is the forward voltage of the D3, equal to VD2

(7)

The R_{CHG} is to limit the peak current through the capacitor, internal MOSFET, and D2 and D3. From Equation 7, high R_{CHG} will result in low C_{OUT2} voltage. Thus the R_{CHG} cannot be too large. It is suggested to select R_{CHG} as Equation 8, which means the time constant of the R_{CHG} and C_{CHG} is equal to the switching cycle.

$$R_{CHG} \times C_{CHG} = T_S \tag{8}$$

The power loss of the resistor can be estimated through Equation 9, assuming that the RMS current through the R_{CHG} is closed to the average current.

$$P_{RCHG} = R_{CHG} \times \left(D \times {I_{CHG1}}^2 + (1-D) \times {I_{CHG2}}^2\right) \tag{9}$$

4 Circuit Design With TLV61048

This section uses the TLV61048 device as an example to demonstrate the design process introduced in this application report.

The input and output electrical requirements follow:

- Input voltage V_{IN}: 3.3 V
- Positive rail voltage V_{OUT1}: 12 V
- Negative rail voltage V_{OUT2}: –12 V
- Maximum output current of V_{OUT1} and V_{OUT2}: 100 mA
- Voltage ripple of V_{OUT2}: 120 mV

Based on this requirement, the design process is as shown in the following list when setting the switching frequency to 1 MHz:

- Duty cycle D: 75% by Equation 1
- Average current during T_{ON}, I_{CHG1}= 133 mA by Equation 2
- Average current during T_{ON}, I_{CHG2}= 400 mA by Equation 3
- DC voltage of the C_{CHG} at zero loading, V_{CHG} ≈ 12 V by Equation 5
- Voltage ripple of V_{CHG} is 1% of its DC voltage, ΔV_{CHG} ≈ 120 mV
- Effective capacitance of C_{CHG}, 0.83 µF by Equation 4
- Current limit resistor, R_{CHG} = 1.2 Ω by Equation 8
- Power loss of R_{CHG}, 60 mW by Equation 9
- Effective capacitance of C_{OUT2}, 0.6 µF by Equation 6
- DC voltage of C_{CHG} at 100 mA, V_{CHG}= 11.5 V by Equation 5
- DC voltage of C_{OUT2} at 100 mA, V_{OUT2}= –11 V by Equation 7

Using the external components value closed to the previous calculation result , the final circuit is shown in Figure 5. The effective capacitance of the 2.2-µF capacitor at 12-V bias condition is around 0.8 µF.

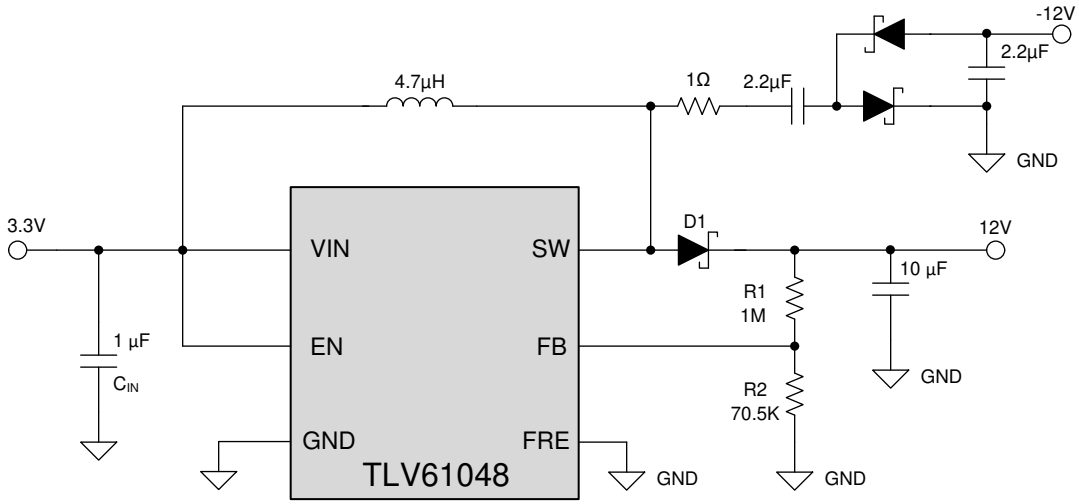

Figure 5. Designed Circuit With TLV61048

The startup waveform through the EN pin at a 100-mA condition is shown in Figure 6. After the EN pin becomes logic high, the voltage of V_{OUT1} and V_{OUT2} ramp up to the setting value smoothly.

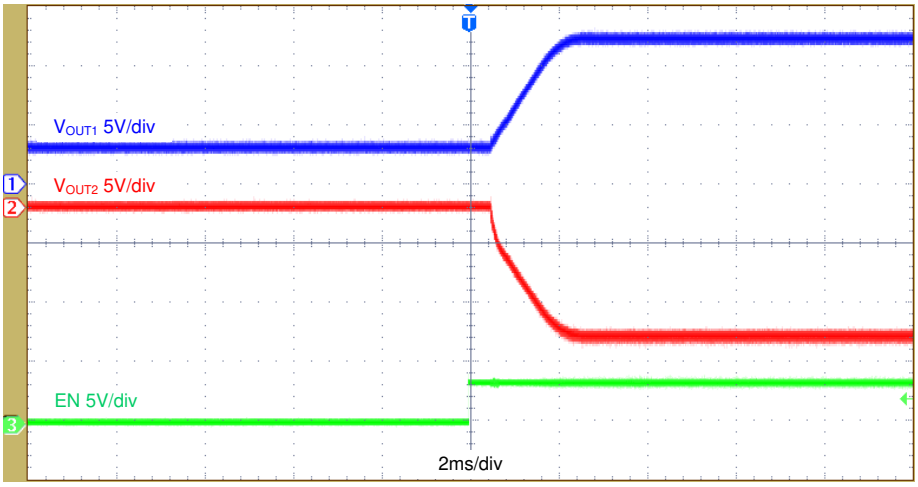

Figure 6. Startup Waveform by EN Pin

The absolute value of V_{OUT2} from 20 mA to 100 mA is shown in Figure 7. The voltage gap between the calculation result by Equation 7 and the bench test result is approximately 100 mV. Because of the voltage drop of the resistor and the Schottky diode, the V_{OUT2} absolute value is 11.6 V at 20-mA loading and is 11 V at 100-mA loading.

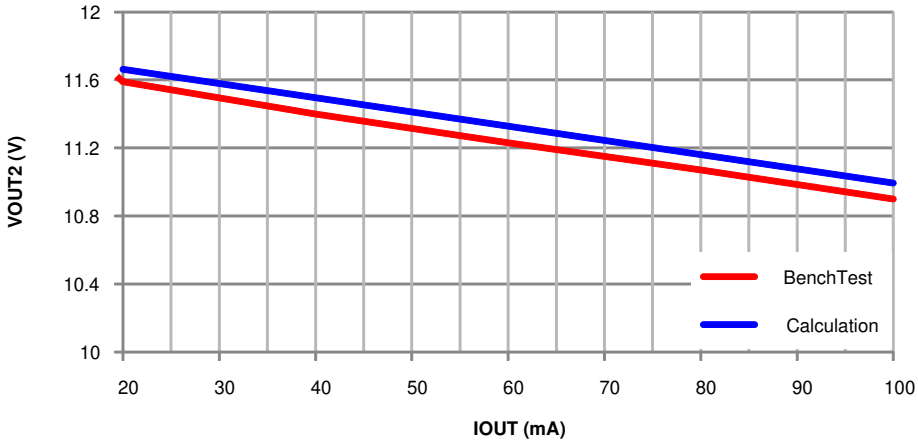

Figure 7. Load Regulation of the Negative Rail

5 References

1. Texas Instruments, *Design for a Discrete Charge Pump*

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