

Powering the AM64xx with the LP8733xx PMIC



Overview

The AM64x processor is able to service a broad number of applications and has multiple power solutions. For some applications, system complexity or user needs will require additional rails, while other users have a higher consideration for physical size or cost. By offering both single and dual-PMIC power solutions, TI has multiple options for powering the AM64x. The purpose of this tech note is to highlight the single PMIC solution recommended for the AM64x Processor and outline its benefits. There is also a secondary, dual-PMIC solution for those users who desire power for additional ICs connected to AM64x.

How Does the LP873364 PMIC Power the AM64?

The LP873364 device has an input range from 2.8 V to 5.5 V, making this solution appropriate for applications powered from a 3.3 V or 5 V DC supply. It has four rails and two GPOs that are used for sequencing. The LP873364 device has two step-down converters that provide the 0.75-V power rail required for the VDD_CORE Arm® core and a 3.3-V rail for DVDD3V3, which can also power peripherals and I/O. Isolating the AM64x analog and digital 1.8 V domains is possible with the two 1.8 V 300-mA LDOs, reducing the opportunity for crosstalk. These LDOs provide additional power for peripherals as well.

This PMIC includes two General Purpose Outputs (GPOs) programmed to sequence additional regulators, if required, such as the TPS745 (LDO) and TPS62822 (buck regulator). For an easier design solution, one can swap the TPS62822 with the TPSM82822 module, which integrates the step-down converter with a pre-selected inductor. The TPS745 powers the 0.85-V rail necessary to supply VDDR_CORE and comes with integrated power good and active discharge. Using a discrete LDO or regulator with no active discharge could cause the VDDR_CORE power rail to take an indeterminate amount of time to fully discharge, in which case VDDR_CORE would be an unknown voltage after the power-down sequence starts, and potentially violate the VDDR_CORE/VDD_CORE power down requirement for the AM64x. However, this is not a problem with the proposed design. Both the TPS745 and TPS62822 (TPSM82822) are robust discrete power options with PG's that can be tied back to

GPO and therefore MCU_PORz, thus protecting the processor and shutting down the rails in a controlled power down sequence in case of a power fault. The PGOOD of LP873364 is wired in a gated mode of operation, which eliminates the need for additional components to generate processor PORz upon start-up and to monitor voltage levels of key voltage domains.

- For applications using DDR4 memory, TPS62822 (TPSM82822) powers VDDS_DDR of the AM64x and VDD of the DDR4. A second TPS745 discrete LDO is enabled by LP873364 LDO0 to supply the DDR4 VPP rail.

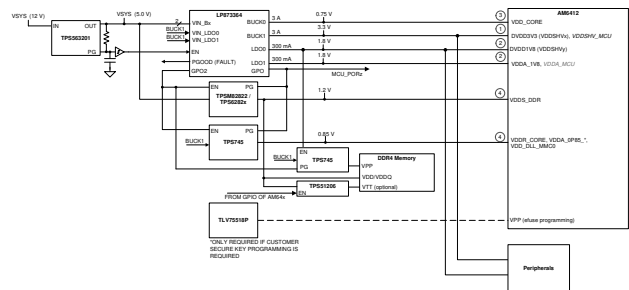


Figure 1. Powering AM64x With LP8733xx | DDR4 Memory

- For LPDDR4 applications, TPS62822 (TPSM82822) powers VDDS_DDR of the AM64x and VDD2 of the LPDDR4. The memory's VDD1 is powered by LDO0 of the LP873364. A second TPS745 discrete LDO is not needed.

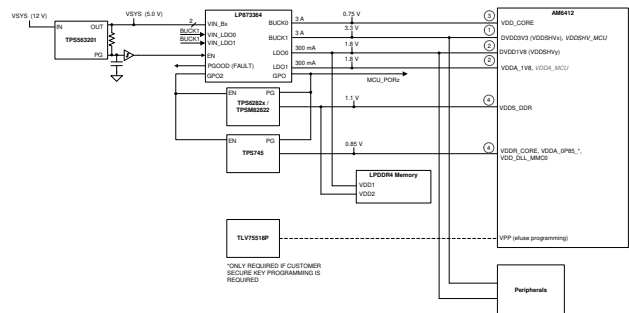


Figure 2. Powering AM64x With LP8733xx | LPDDR4 Memory

A single PMIC approach is both cost and size optimized. It can occupy up to 42% less board space than the [AM64x SK EVM](#) and takes up considerably less board space than the [AM64x GP EVM](#). It has been tested extensively in the lab for power, sequencing, brownout, and fault conditions. The single PMIC power design can be implemented for either DDR4 or LPDDR4 and is encouraged for new designs.

Can the LP873364 be Used in a Dual PMIC Configuration?

The LP873364 can also be used in conjunction with the TPS6521855, a PMIC from the TPS65218xx family pre-programmed specifically to meet the needs of the AM64x. In this configuration, the TPS6521855 GPIO1 can be used to enable LP873364, initiating the proper power up sequence. Similar to the single PMIC solution, a discrete such as the TPS745 is necessary to supply the VDDR_CORE rail. The TPS6521855 device has four step-down converters that generate the 1.1-V (or 1.2-V) rail required for LPDDR4 (or DDR4) memory, the 1.1-V rail required for multiple Ethernet PHYs, a 3.3-V rail required for I/Os, and an additional 2.5-V rail for the Ethernet PHYs. TPS6521855 comes pre-programmed for interface with LPDDR4 memory, but maintains the [programmable DIY functionality](#) of the TPS65218xx family, and can be reprogrammed for DDR4 memory use. If DDR4 is used, the VPP rail of the DDR memory will be supplied 2.5 V by DCDC4 of the TPS6521855. In the case of LPDDR4, the TPS6521855 supplies the necessary 1.8 V. The TPS6521855 output voltages and sequencing order are determined by an EEPROM-backed register map, which can be programmed to work with the LP8733xx to power the AM64x processor.

By utilizing two PMIC devices, there are more rails available for functionality and interface with additional ICs like TI's [DP83867 Gigabit PHYs](#). The pre-programmed TPS6521855 interfaces with the LP873364 to provide a user-friendly power design by means of its ready hardware solution available with the AM64 SK EVM, which can be leveraged for design as a reference.

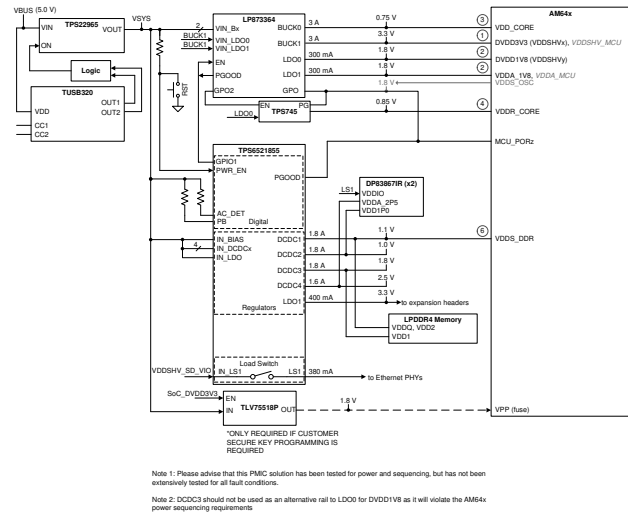


Figure 3. Two PMIC Solution: LP873364 w/ TPS745 (LDO) and TPS6521855 Power Block Diagram

Pre-production samples of the LP873364 (P873364RHDR) are now available, and the device will be released in 4Q'21.

To create a design based on this technical brief, visit the [LP8733 product folder](#) and the [TPS6521815 product folder](#).

Related Documentation

- Texas Instruments: [AM335x PMIC Selection Guide](#)
- Texas Instruments: [Powering the AM335x, AM437x, and AM438x with TPS65218D0](#)
- Texas Instruments: [TPS6521815 User-Programmable Power Management IC \(PMIC\) With 6 DC/DC Converters, 1 LDO, and 3 Load Switches Data Sheet](#)
- Texas Instruments: [LP8733xx Dual High-Current Buck Converter and Dual Linear Regulator Data Sheet](#)
- [AM64x Sitara™ Processors Landing Page](#)

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