Application Report
SLVAES2–April 2020

Six System Architectures With Robust Reverse Battery Protection Using an Ideal Diode Controller

Dilip Jain

ABSTRACT

With the emergence of new trends in automotive electronics such as autonomous driving, advanced car infotainment systems, system designers are facing new challenges, particularly in designing automotive front-end power systems. The front-end reverse battery protection system directly impacts the reliability of overall system design. The rise in processing power levels and miniaturized electronic system sizes increases the demand for high efficiency and high power density designs. Electronic Control Unit (ECU) designs such as Sensor Fusion, USB Type-C™ hubs, and Premium Audio amplifiers typically range from 100 W–1000 W. Discrete reverse battery protection solutions like Schottky diodes and P-FETs no longer become a viable solution at these system power levels due to poor efficiency, need of thermal management, and an increase in PCB space. Redundancy requirements especially in autonomous driving are driving a need for newer system architectures like input supply ORing, and power MUXing in dual battery-based systems. Robust protection during stringent automotive Electromagnetic Compatibility (EMC) testing adds an another layer of complexity while designing these front-end power systems.

This application report highlights how the new LM74800-Q1 back-to-back power N-channel FET-based ideal diode controller with load dump protection simplifies the reverse battery protection system design and how it enables various front-end protection circuit design architectures based on common drain, common source topology of the back-to-back FETs, ORing and Power MUXing.

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1 LM74800-Q1 Ideal Diode Controller Overview

The LM74800-Q1 ideal diode controller drives and controls external back-to-back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control, inrush current limiting, and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V and 24-V automotive battery-powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V.

The device has separate GATE control and outputs (DGATE and HGATE) for back-to-back FET driving. An integrated ideal diode controller (DGATE) drives the first MOSFET (Q_1) to replace a Schottky diode for reverse input protection and reverse current blocking for output voltage holdup. An integrated charge-pump with 600-µA (3-mA in LM74810-Q1) capacity and 20-mA peak DGATE source current driver stage along with short turn ON and turn OFF delay times ensures fast transient response. This ensures robust performance during automotive testing such as with the ISO16750 or LV124 where an ECU is subjected to AC superimposed input signals. With a second MOSFET (Q_2) in the power path, the device allows a load disconnect (ON/OFF control) and overvoltage protection using HGATE control. The device features an adjustable overvoltage cutoff protection feature using a programming resistor across the SW and OVP terminal.

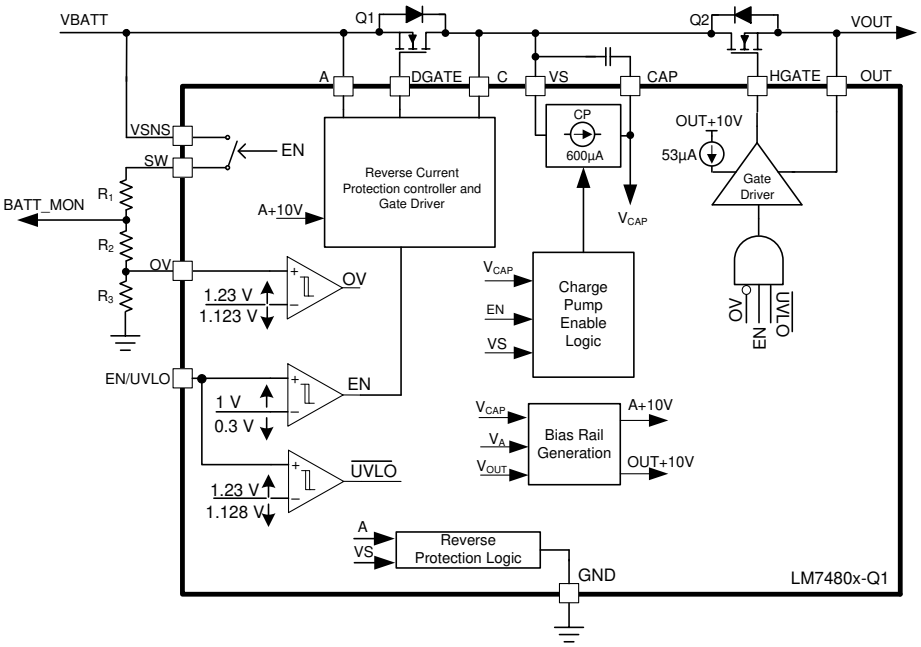

Figure 1. Functional Block Diagram

Figure 1 shows the LM74800-Q1 functional block diagram. The ideal diode stage controls the DGATE drive and operates based on the A (anode), C (cathode) and EN/UVLO (EN) inputs. With the closed loop feedback control, this stage regulates the forward voltage drop across A and C terminals at 10.5-mV (typical). The load switch stage controls the HGATE drive and operates based on the EN/UVLO and OVP input signals. The separate GATE control enables robust system performance and functional class A status during automotive testing.

The device has a separate supply input pin (Vs). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM74800-Q1 device offers flexibility in system design architectures and enables circuit design with various power path control topologies like common drain, common source, ORing and Power MUXing. With these various topologies, the system designers can design the front-end power system to meet various system design requirements.

Some system design architectures based on the LM74800-Q1 device and the associated end-application goals are outlined in the following sections.

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2 Design # 1: Common Drain Topology of the Back-to-Back FETs

Back-to-back FETs based front-end protection is required in the systems where inrush current limiting and load disconnection control along with reverse battery protection is desired. Load disconnection during an overvoltage fault such as load-dump allows use of low voltage downstream components such as capacitors and DC/DC converters enabling dense ECU designs such as ADAS camera, USB Hubs, LIDAR, and TCU. Common Drain topology of the back-to-back FETs provides access to an always ON path and load disconnect control path saving system IQ during sleep mode with always ON loads connected. The Common Drain topology also enables ORing designs with load disconnect control.

Figure 2 shows a typical application circuit with common drain topology of the back-to-back N-channel FETs using the LM74800-Q1 device. TVS, D_1 is required for ISO7637 transient pulse suppression.

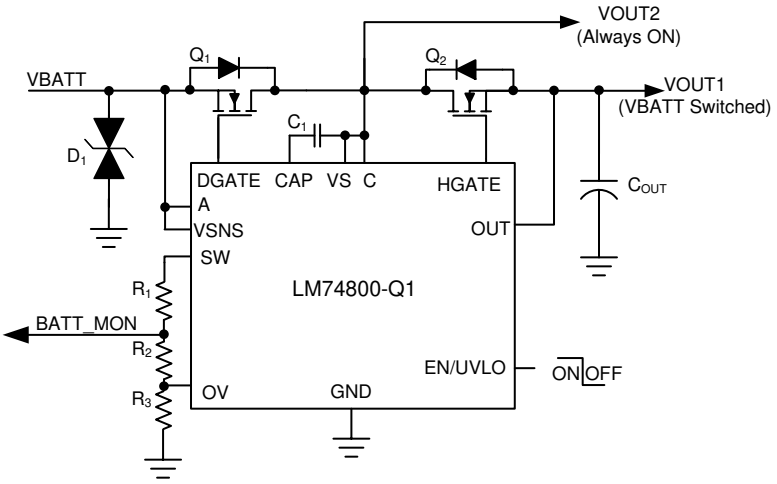

Figure 2. Typical Application Circuit With Always ON Power Path and ON/OFF Control

The GATE of FET Q_1 is driven by DGATE and controlled by the LM74800-Q1 device to protect the downstream loads from reverse voltages due to mis-wiring of the battery terminals to the ECU as well as during ISO7637 transient testing. Performance during ISO7637 Pulse 1 testing is shown in Figure 3. This FET Q_1 is also controlled to act as an ideal diode rectifier

- To block reverse current flow from the output capacitors, C_{OUT}, back to input supply during system tests such as input microshorts or short supply interruptions (LV124-E10) thereby holding output capacitor charge and enabling functional status A system performance during this test. Performance during input microshort testing (LV214-E10) is shown in Figure 4 and Figure 5. Notice that the HGATE remains un-disturbed during this testing ensuring robust performance.
- During AC superimpose tests (LV124-E06), to block reverse current flow from the load back to battery and turn ON quickly minimizing body diode conduction. This operation ensures thermally efficient operation and provides output voltage filtering. Figure 6 illustrates the performance during AC superimpose testing (LV124-E06).

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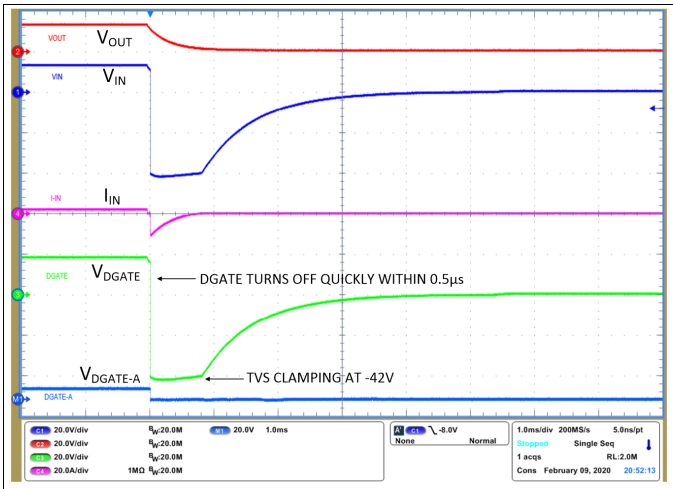

Figure 3. Performance During ISO7637-Pulse 1 Testing

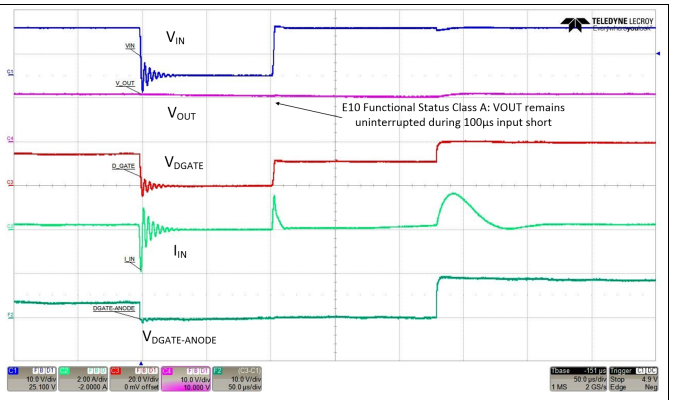

Figure 4. Performance During Input Microshort Testing – HGATE Remains Undisturbed

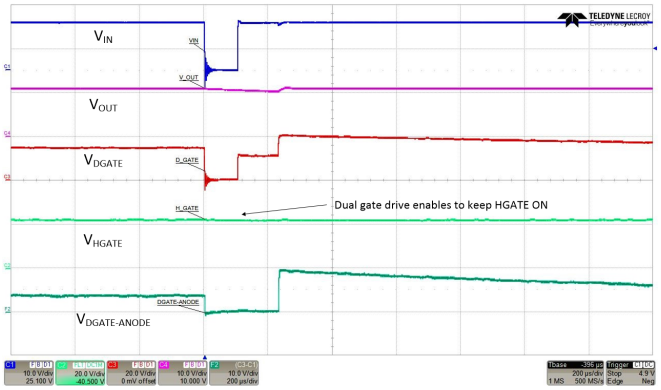

Figure 5. Performance During Input Microshort Testing – HGATE Remains Undisturbed

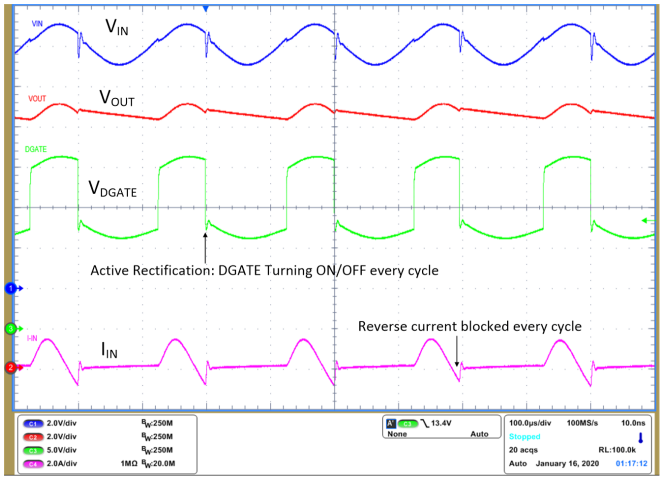

Figure 6. Performance During AC Superimpose Testing - Active Rectification, Low V_{OUT} Ripple

The GATE of FET Q_2 is driven by HGATE and it is controlled for load switching. This FET protects the downstream loads from system faults such as overvoltages during automotive load dump input undervoltage conditions and overload conditions. Inrush current limiting can also be achieved by the slew rate control of HGATE. This switch can be used to disconnect the downstream loads to save the system quiescent current during the sleep mode or ignition off state of a car by pulling the EN/UVLO of LM74800-Q1 low to meet the total ECU current budget of < 100 µA.

With the common drain configuration of the external back-to-back FETs, one can access the always ON path (VOUT2) that is protected from reverse polarity faults and reverse current flow. This terminal can be used to power loads such as CAN and LIN transceivers that are expected to be active even during the ignition off state of a car. When the EN/UVLO input of the LM74800-Q1 device is pulled low below the low I_Q shutdown threshold voltage $V_{(ENF)}$, both the DGATE and HGATE turn OFF, disconnecting the system loads connected on VOUT1 path. This reduces the system I_Q due to the downstream DC/DC converters and electrolytic capacitors. The VOUT2 path still continues to provide power to the always-on loads through the body diode conduction of Q_1. With EN/UVLO pulled low, the LM74800-Q1 device consumes a very low I_Q of 3 µA.

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3 Design # 2: Ideal Diode Configuration Only

For the ideal diode configuration without back-to-back FET driving, refer to the LM74700-Q1 solution. The LM74700-Q1 is an optimum ideal diode solution for the system designs requiring < 300-µA charge pump capacity. The LM74800-Q1 offers 600-µA and LM74810-Q1 offers 3-mA charge pump capacities, respectively. Figure 7 shows the LM748x0-Q1 configuration for ideal diode-only designs.

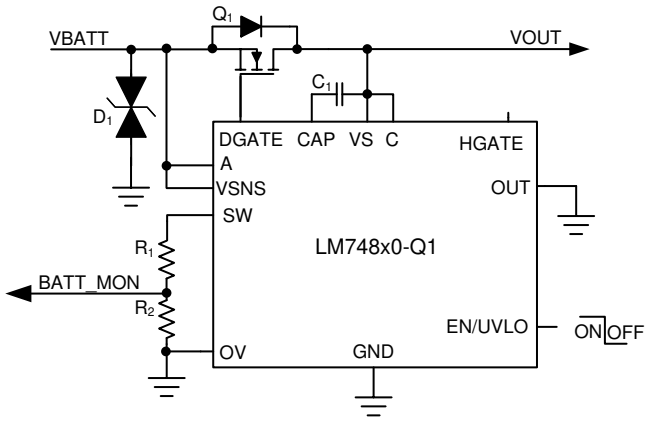

Figure 7. Typical Application Circuit for Ideal Diode-Only Designs

Compute the required charge pump capacity, $I_{(CAP\_MIN)}$ for your design by multiplying the maximum AC superimpose frequency and and gate charge of Q_1 , that is, Q_G at 6-V V_{GS}. See Figure 8 for Q_G calculation from the FET gate charge characteristic curves. Active rectification operation of Q_1 is assured during every AC superimpose cycle with a controller having charge pump capacity, $I_{(CAP)} > I_{(CAP\_MIN)}$. Figure 9 illustrates the performance of the LM74810-Q1 under 200-kHz AC superimpose testing.

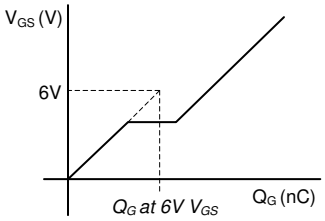

Figure 8. Typical Gate Charge Characteristics of a MOSFET

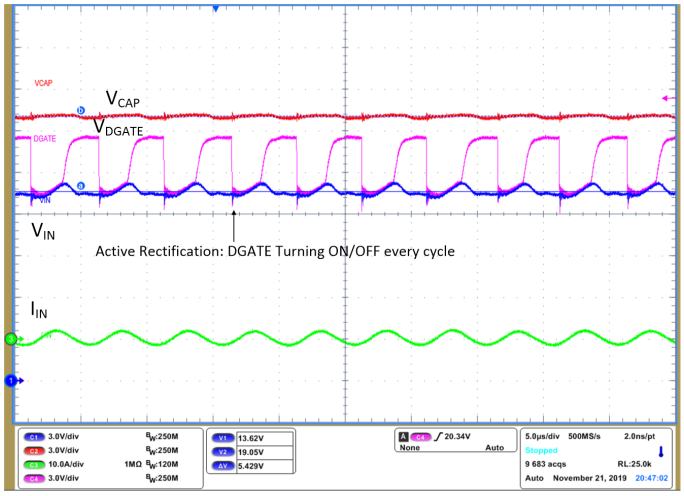

Figure 9. LM74810-Q1 Performance During 200-kHz AC Superimpose Testing

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4 Design # 3: Common Source Topology of the Back-to-Back FETs

Automotive ECU designs powered from a vehicle battery need to be load dump tolerant. For the 12-V car battery based designs, the suppressed load dump peak specification is 35-V. These systems are with centralized load dump suppression inside the alternator. For the system designs without the centralized load dump suppression, the surge voltage due to unsuppressed load dump can peak up to 101 V in 12-V systems and 202 V in 24-V battery based systems as per the ISO-16750-2:2010 standard. The surge voltage during load dump ranges for a duration of 40-ms to 400-ms, depending on the test levels. This results in a huge amount of energy content and the ECUs need to be protected from these surge voltages. Several high-power TVS stacks (SMD sized) are required to clamp to a safe level (below the downstream absolute maximum voltages) during the unsuppressed load dump resulting in an increase in overall solution size and BoM cost of the front-end protection circuit.

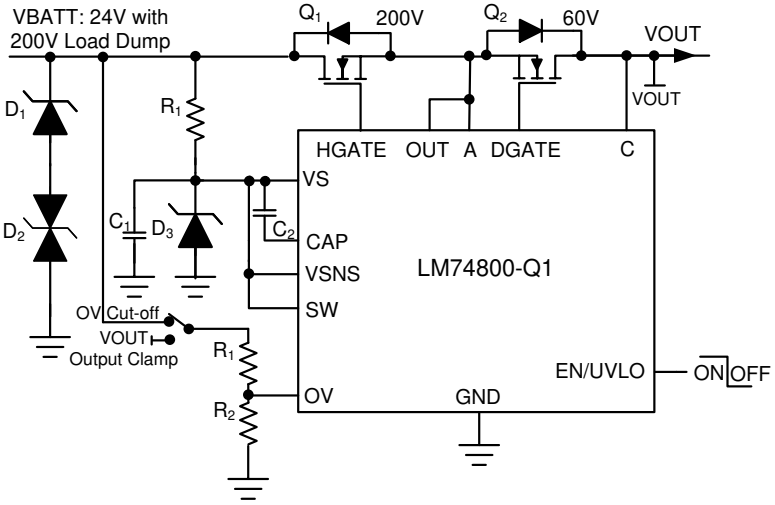

Figure 10. Typical Application Circuit for Unsuppressed Load Dump Protection

The LM74800-Q1 solution with the external MOSFETs configured in common source topology provides unsuppressed load dump protection using the series power path protection technique. Figure 10 shows the unsuppressed load dump protection circuit using the LM74800-Q1 device. The VDS rating of Q_1 should be > peak load dump voltage. TVS diodes D_1 and D_2 are designed for ISO7637 Pulse 1, negative voltage suppression and are SMB sized. The combined positive clamping voltage of this TVS setup is at a level close to the peak surge voltage of the load dump profile. This ensures that the TVS does not conduct during the load dump. The negative clamping voltage of the TVS D_2 during ISO7637 Pulse 1 should be set above the absolute maximum voltage rating of –65 V of the LM74800-Q1 device. For a 24-V vehicle-based design with ISO7637 Pulse 1 level of –600 V with 50Ω surge impedance, TVSs SMBJ150A and SMBJ36CA are recommendations for D_1 and D_2, respectively for LM74800-Q1 design. Set the overvoltage threshold using the resistors R_1 and R_2. With the resistor ladder connected from the input supply side, the circuit operates in overvoltage cutoff mode and with the connection from the V_{OUT} side, it operates in V_{OUT} clamp mode. Figure 11 and Figure 12 illustrate the unsuppressed load dump protection with OV-cutoff and V_{OUT}-clamp operation, respectively.

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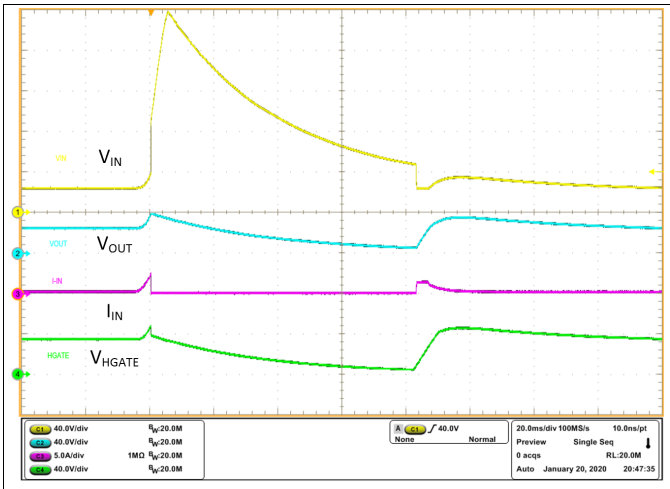

Figure 11. Performance During 200-V Unsuppressed Load Dump – OVP Cutoff at 38 V

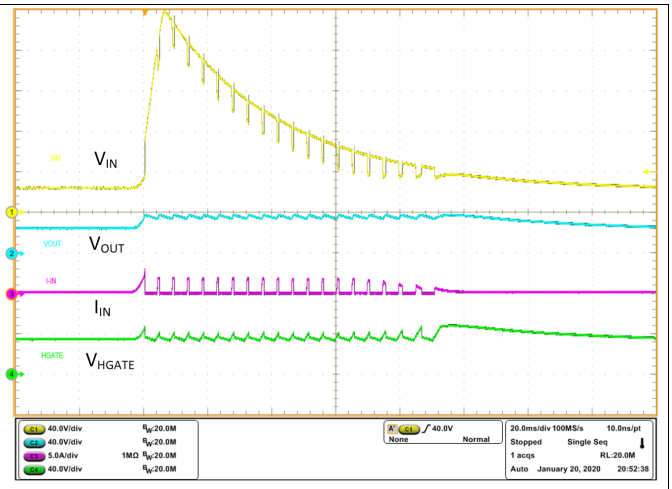

Figure 12. Performance During 200-V Unsuppressed Load Dump – V_{OUT} Clamp at 38 V

5 Design # 4: Reverse Battery Protection With Overcurrent Protection

Load current monitoring and overcurrent protection are required in functional safety designs as well as ADAS and Infotainment ECU designs such as LIDAR and Audio amplifiers.

Figure 13 shows front-end protection design based on LM74800-Q1 ideal diode controller and INA302-Q1 current sense amplifier.

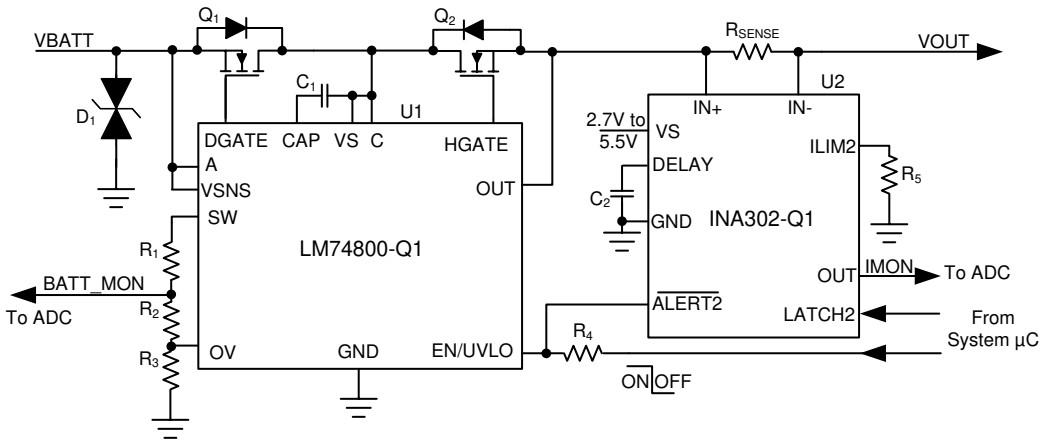

Figure 13. Typical Application Circuit for Reverse Battery Protection With Overcurrent Protection

The INA302-Q1 current-sense amplifier has integrated dual comparators with adjustable fault assertion ($\overline{\text{ALERT2}}$) delay. Overcurrent protection threshold can be set using R_5. For latch-off operation after fault detection, drive LATCH2 of the INA302-Q1 device high.

The overload fault response time can be set using C_2. During an overload fault event, $\overline{\text{ALERT2}}$ asserts after the set delay and pulls EN/UVLO of the LM74800-Q1 device low, turning OFF Q_2 within 6-µs.

6 Design # 5: Dual Supply Input ORing With Load Disconnect Control

System designs with redundancy are common architecture in safety-critical designs such as ADAS systems. In these designs, the ECU input power can be from more than one supply connection.

Figure 14 shows the application circuit for a dual-supply input ORing with load disconnect control using the LM74800-Q1 and LM74700-Q1 devices.

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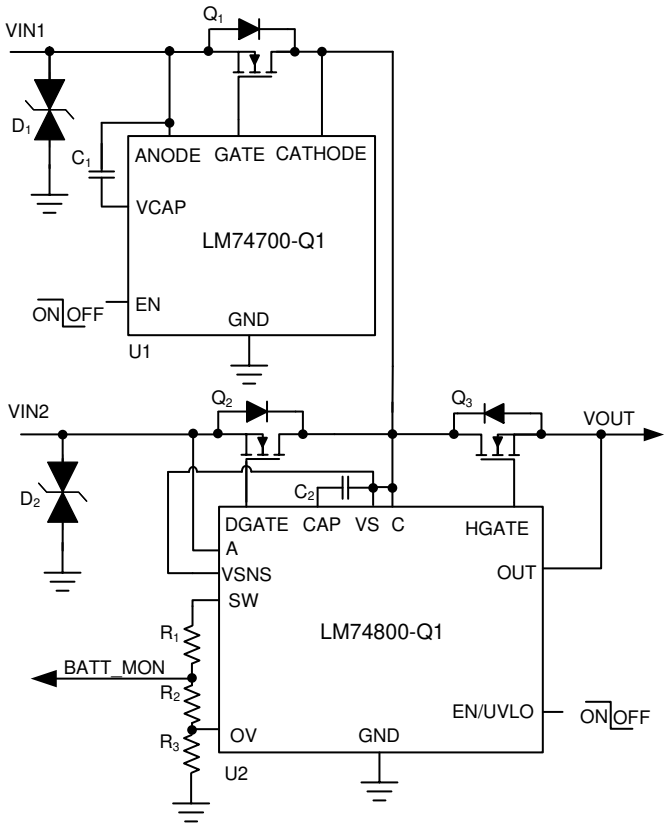

Figure 14. Typical Application Circuit for Supply ORing With Load Disconnect Control Designs

Based on the system redundancy architecture VIN1 and VIN2 can either be powered from two separate battery sources or can be connected to a common battery source through separate cables running through the fuse box. The downstream supply comes from ORed inputs and the load protection and operation is similar to as in Section 2.

7 Design # 6: Reverse Battery Protection With Priority Power MUXing

Another architecture of power-supply redundancy is based on a system with one primary source like a vehicle battery and an auxiliary supply source like a DC/DC converter or a large storage capacitor. When both the supplies are present, then the priority should be given to the primary source and the system should be powered from the primary source path independent of the supply voltage levels. In the absence of the primary supply or when the primary supply drops to a specified undervoltage level, then the downstream should switch over to the auxiliary power path. The transition should be fast enough ensuring that the output voltage does not drop below the undervoltage lock out level of the downstream circuit.

Figure 15 shows LM74800-Q1 application circuit for Priority Power MUXing design.

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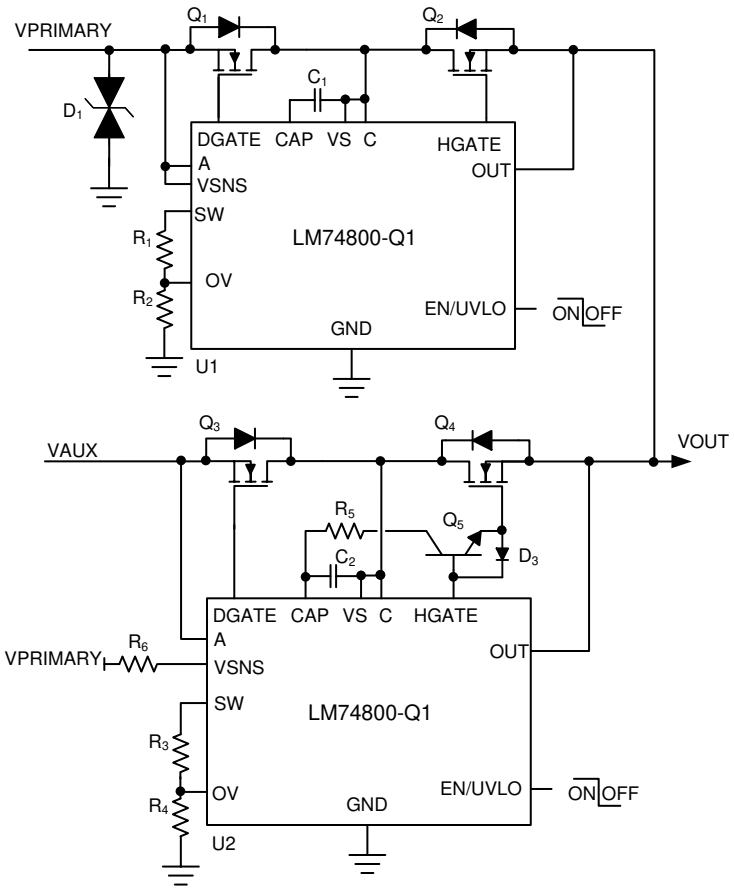

Figure 15. Typical Application Circuit for Priority Power MUXing Designs

The OV connection of the AUX channel is from the primary supply path. The OV falling threshold of U2 is set at the undervoltage level of primary supply. During normal operation, primary path is ON. OV of U2 is high and this keeps GATE of Q_4 OFF, disconnecting the auxiliary supply path to the load. When the primary supply is dropped or when it reaches a set undervoltage level, then Q_2 turns OFF, disconnecting the primary path. At the same time, OV threshold of U2 goes low and HGATE starts rising after a delay of 6-µs (typical). HGATE has gate drive strength, $I_{(HGATE)}$ of 53 µA. Q_5 enables higher GATE drive levels up to 600-µA for fast turn ON of Q_4. U1 on the primary path remains active keeping Q_2 ON, as its Vs supply is powered from the auxiliary path. When the primary supply is connected back, then the system output immediately gets connected to the primary path. OV of U2 goes high and Q_4 turns OFF within 3 µs (typical).

8 Summary

With the separate supply input provision and separate GATE control architecture for back-to-back FET driving, the LM74800-Q1 device offers flexibility in system design architectures and enables circuit design with various power path control topologies like common drain, common source, ORing, and Power MUXing. With these various topologies, the system designers can design the front-end power system to meet various system design requirements. A summary of the system design architectures follows.

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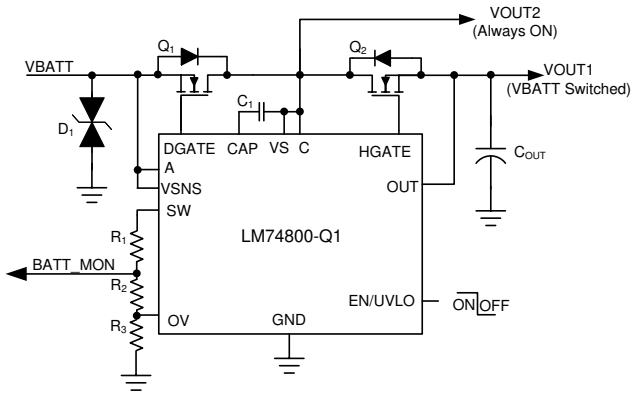

Figure 16. Design # 1

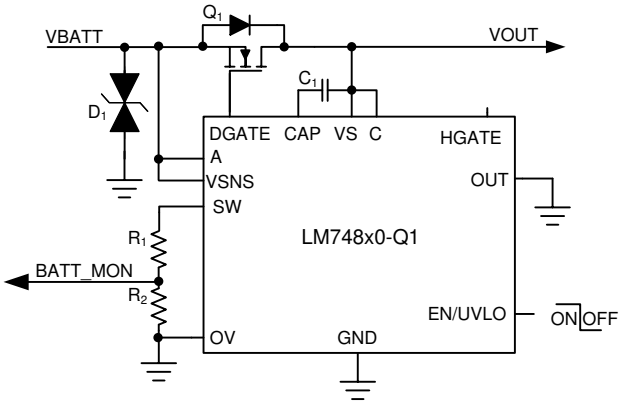

Figure 17. Design # 2

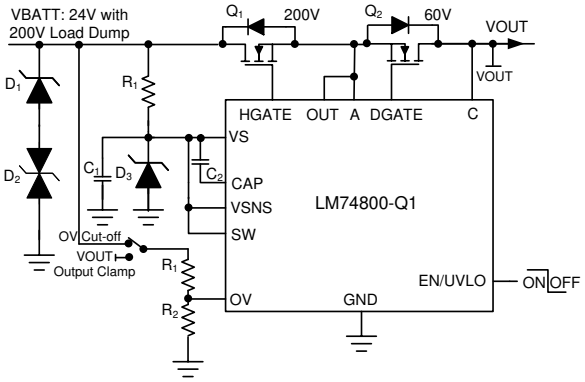

Figure 18. Design # 3

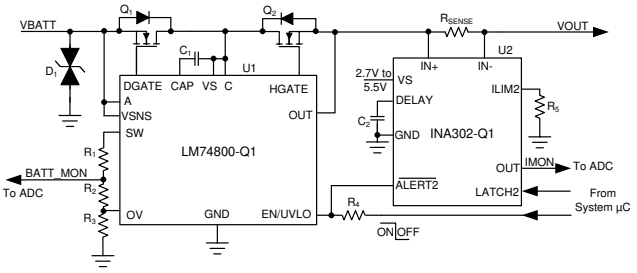

Figure 19. Design # 4

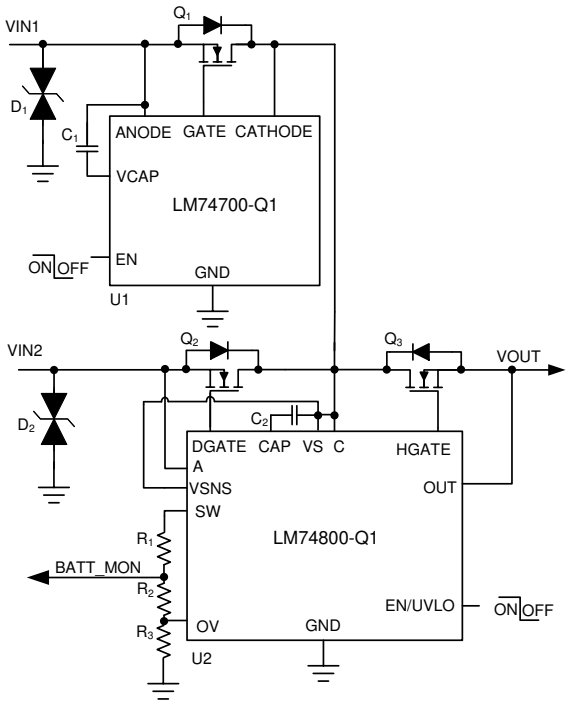

Figure 20. Design # 5

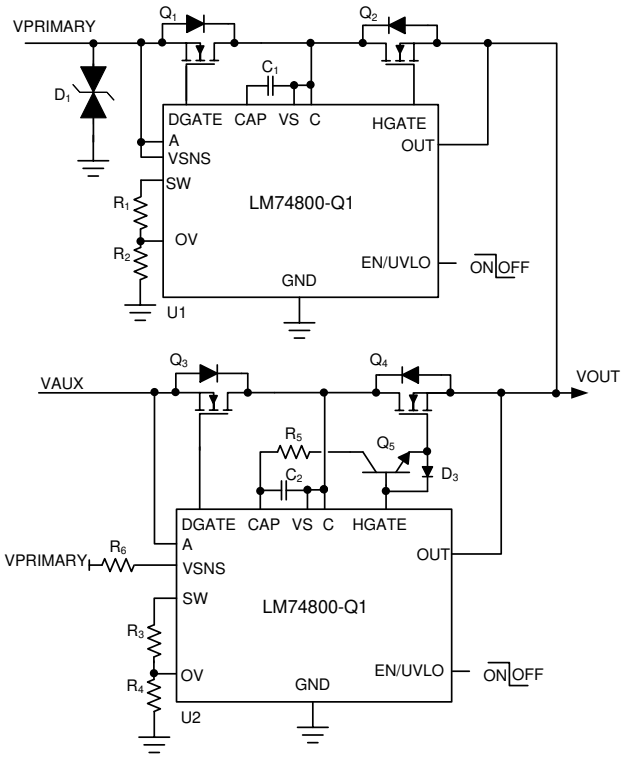

Figure 21. Design # 6

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