Application Report

Designing for Loss of Ground and Loss of Battery on Texas Instruments High-Side Switches

Timothy Logan

ABSTRACT

A loss of ground fault is an erroneous condition on the power design of a system where the reference to ground is disconnected and lost from the system. This can be caused by several different events such as a physical severing of the ground connection or a faulty external wiring being introduced to the power rail. If not properly addressed during the design phase, a loss of ground fault can not only cause damage to the attached power components of a system but also to valuable upstream components such as microcontrollers or logic arrays. A loss of battery condition is when the connection from the high side switch to the upstream power supply is lost. In this fault condition proper design precautions must be taken in order to protect against special loading conditions such as inductive turnoff. In this application note a few key design insights are examined to protect against both loss of ground and loss of battery faults when using Texas Instruments smart high-side switch products.

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1 Loss of Ground Conditions

1.1 Loss of Device Ground

The first classification of loss of ground when using a Texas Instruments high-side switch is the loss of the local device ground. In this condition, other components of the overall system may have maintained a valid ground reference; however the ground that is referenced by the TI high-side switch has been lost. Figure 1-1 illustrates this condition.

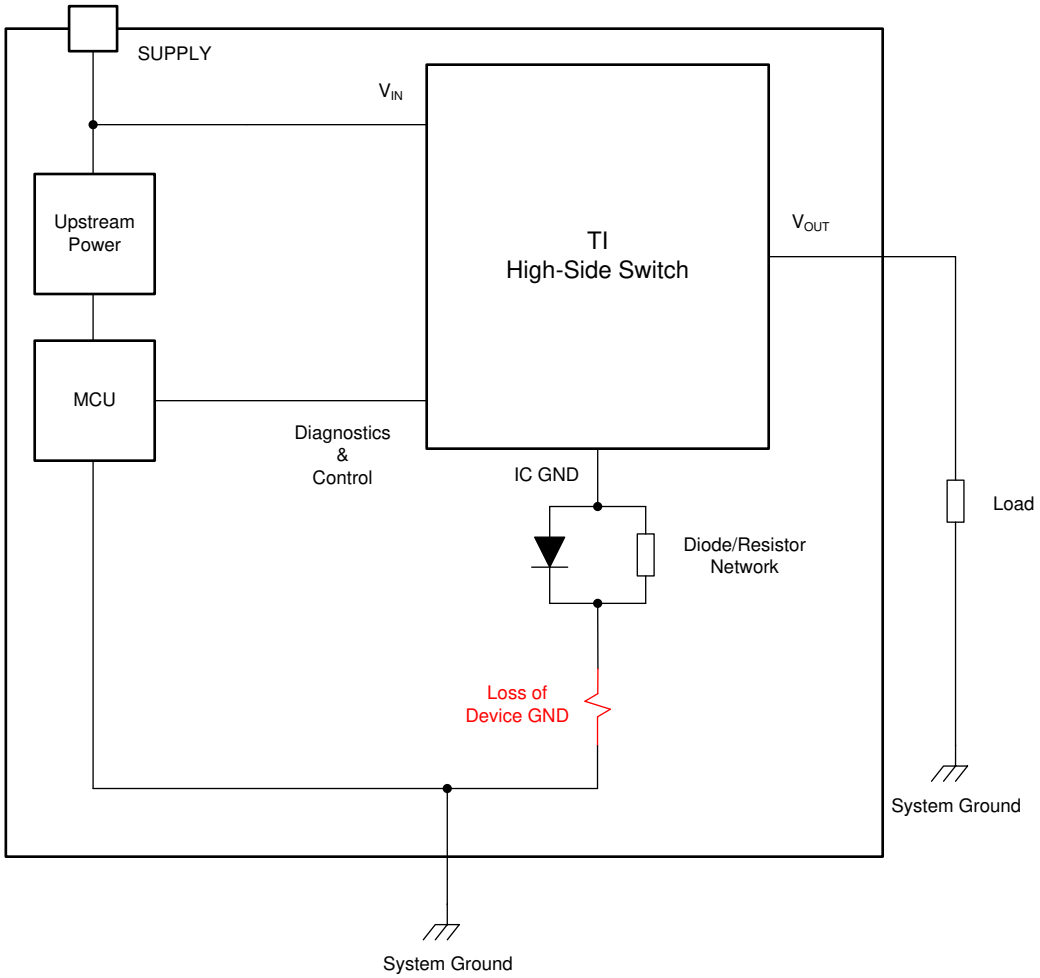

Figure 1-1. Loss of Device Ground

1.2 Loss of Module Ground

The second classification of a loss of ground fault when designing with a TI high-side switch is the loss of ground of the entire module. As high-side switches generally power off board loads, this can be a loss of ground of the entire module or board such as an electronic control unit (ECU). Figure 1-2 illustrates this condition.

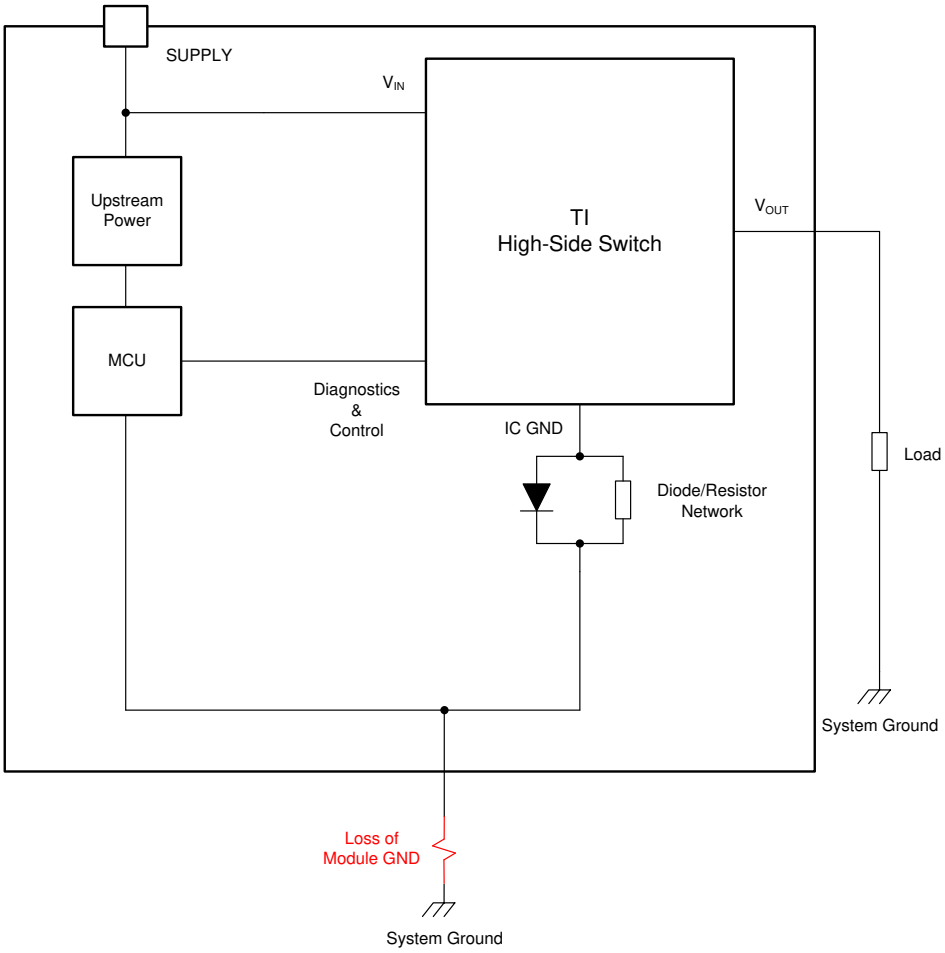

Figure 1-2. Loss of Module Ground

For both loss of local device ground and loss of global module ground, TI high-side switches will have built-in protection mechanisms to disable output and prevent damage. In this automatic shutoff condition, the device turns off the output to protect the downstream load. Once the ground reference is reestablished, the device returns to normal operation and the output follows the relevant signal on the IN pin.

1.3 Output Protection on TPSxHxx Devices

One corner case that needs to be considered on TPSxHxx smart high-side switch devices is a special condition where a loss of module ground occurs while there is a low-impedance path from the supply line to module ground. Figure 1-3 illustrates this condition.

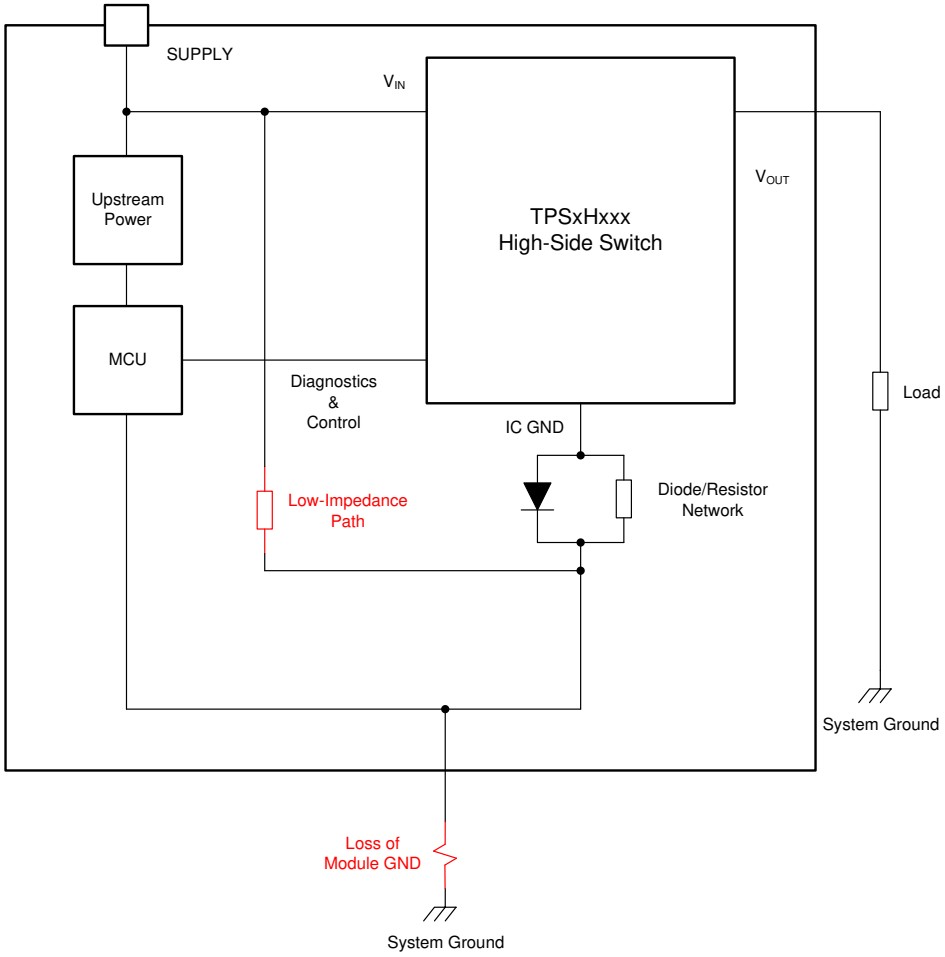

Figure 1-3. Low-Impedance Path

In the TPSxHxx device family there exists an approximately 200-kΩ internal parasitic path from the ground pin to the output pin of the switch itself. Without proper protection when a loss of device ground occurs a current path can exist through the TPSxHxx device. This current path starts from the supply voltage line, passes through the external low-impedance element, continues through the ground network resistor, continues through the internal parasitic path, and outputs to the attached load of the device. Figure 1-4 illustrates this current path.

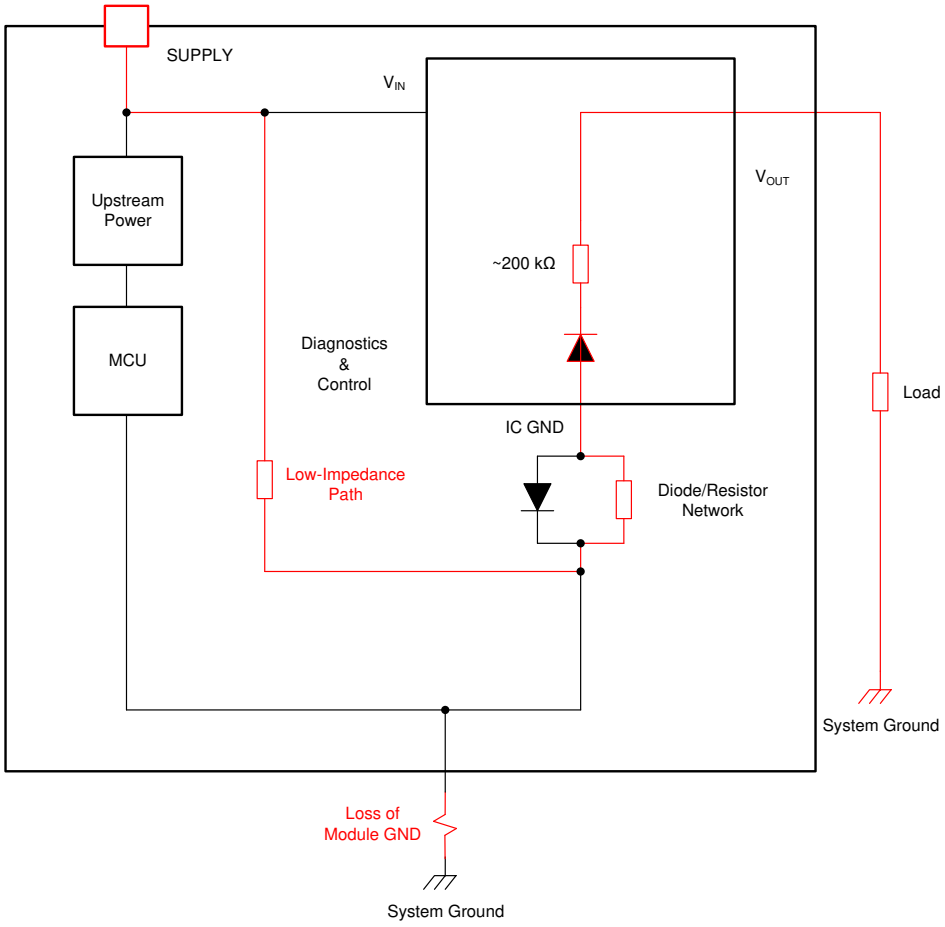

Figure 1-4. Parasitic Path

This parasitic current path can cause the internal FET of the TPSxHxx to partially and potentially fully bias and in effect output a voltage on the load regardless of whether the device is enabled or not. It is important to note that this fault condition will only occur when the following conditions hold true:

1. A low-impedance path exists between the input supply line and the module ground of the high-side switch
2. A module loss of ground exists as described in Section 1.2

It is also important to note that this phenomenon is only observed on the TPSxHxx device family. In the newer generation high-side switches, such as the TPSxHBxx or TPSxHAxx devices, this 200-kΩ parasitic path between the device ground pin and output does not exist and this fault condition is non-existent. Table 1-1 lists the devices affected by this issue.

Table 1-1. Devices With Parasitic Path

Device
TPS1H000-Q1
TPS2H000-Q1
TPS1H200-Q1
TPS1H100-Q1
TPS2H160-Q1
TPS27S100
TPS4H000-Q1
TPS4H160-Q1

Note that in every device listed in Table 1-1, all versions of the specified device are affected. For example. for the TPS1H100-Q1 device, both the TPS1H100A-Q1 and TPS1H100B-Q1 are affected.

A key metric here is what is considered a “low” enough impedance between supply input and module ground to cause this fault. This fault will occur when the voltage at the ground pin is within approximately 500 mV to 1 V of the supply line voltage. Figure 1-5 illustrates the equivalent circuit and current path.

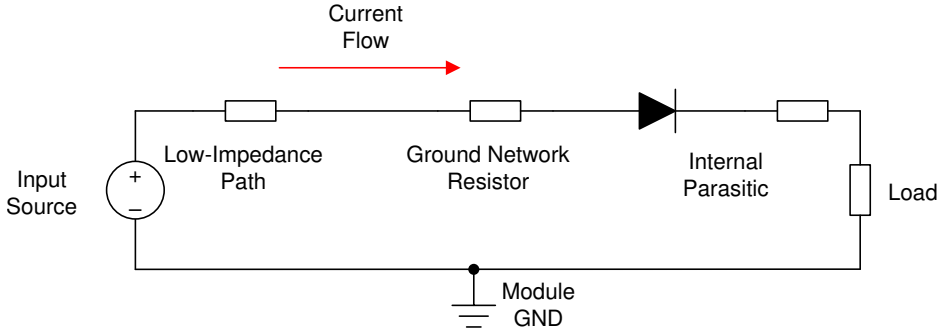

Figure 1-5. Equivalent Current Path

This fault condition occurs when the combined voltage drop across the low-impedance path and the resistor diode network results in a voltage potential before the internal parasitic that is approximately within 500 mV to 1 V of the original input source voltage. In regular operating conditions where the module ground connection is not lost, this is not an issue as a valid ground connection exists after the low-impedance path.

To protect against this double fault condition, appropriate design considerations have to be made to the resistor/diode network connected between the ground pin of the high-side switch and the local device ground. The data sheet of each device may vary; however, the general recommendation is to place a 1-kΩ resistor in parallel with a diode that has a forward current greater than 100 mA. To protect against the described about parasitic fault condition, it is recommended to increase the value of the resistor on the ground network to around 2 kΩ and to change the unidirectional diode to steering diode configuration such as the BAV199. Figure 1-6 illustrates this solution.

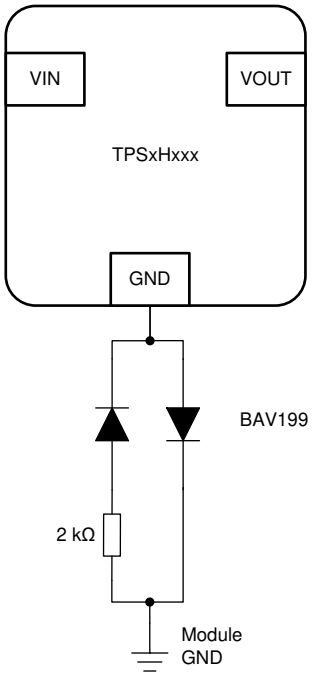

Figure 1-6. Solution

The key parameter with the increased resistance is to introduce a voltage drop across the resistor so that the voltage seen at the GND pin of the TPSxHxxx is not within 500 mV to 1 V of the supply voltage seen at the input. An increased resistor value; however, will cause protection challenges during inductive clamping events where a negative voltage spike occurs on module ground. For this reason, the BAV199 steering diode is introduced allowing for the voltage drop to not be an issue when handling inductive loads.

2 Loss of Battery Conditions

2.1 Loss of Battery

A loss of battery condition is a fault condition where the potential connected to the supply rail of the high-side switch is suddenly lost. This creates a scenario where an undefined potential sits between the input supply of the high-side switch and the output load attached. This can be caused by conditions such as a faulty upstream regulator or physically severed power connection. All of TI's smart high-side switches have built-in protection mechanisms that will immediately shut off the output of the high-side switch in a loss of battery condition. While the output of the high-side switch will be shut off to protect the switch and load itself, precautions must be taken to protect the upstream and downstream power path when driving inductive loads.

2.2 Inductive Loading and Loss of Battery

One concern when dealing with loss of battery faults is how to handle the negative voltage spike that is associated with driving an inductive load. During this turnoff, an unwanted voltage spike occurs on the output of the high-side switch due to the sudden turn off of the inductive load. In cases where a loss of battery condition is possible, having an inductive discharge clamp from V_{OUT} to VS is not possible as the potential on VS will be undefined. Instead the designer has two options:

- Connecting a flyback diode in parallel with the load
- Use of a resistor/diode network on GND pin and serial protection resistors

The first option of connecting a flyback diode in parallel with the inductive load is a safe way of decoupling the voltage spike from the upstream high-side switch. In this approach the energy is dissipated across the circular path in parallel with the load as Figure 2-1 shows:

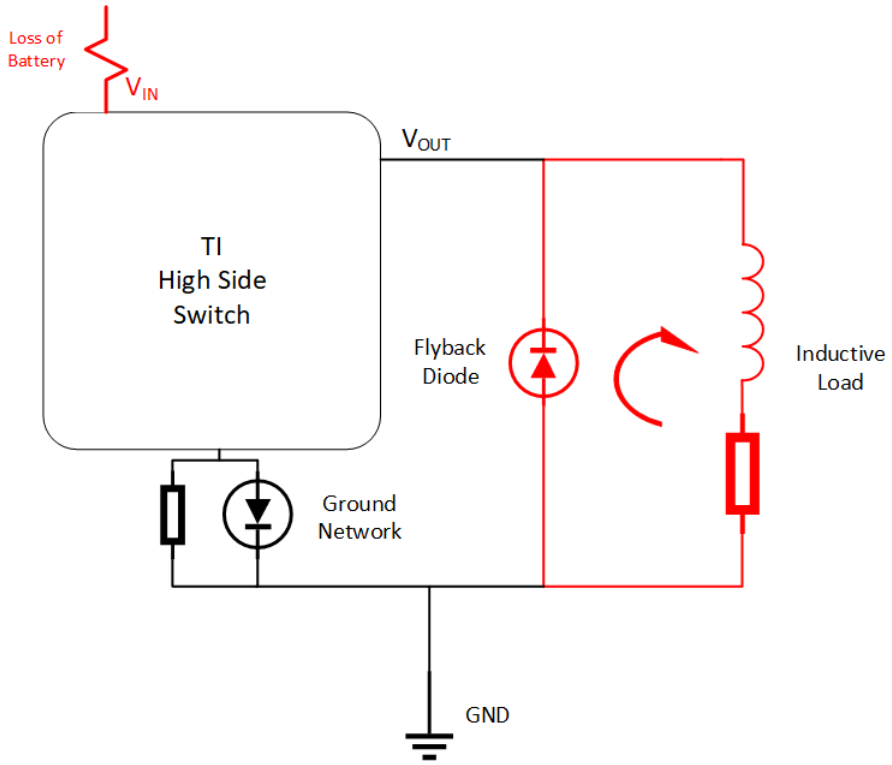

Figure 2-1. Current Path for Flyback Diode

As the current path is dissipated across the diode, the negative voltage seen at the output of the high-side switch will be approximately equal to the negative forward voltage of the diode (typically –0.7 V). While this method has the advantage of decoupling the high-side switch completely from the inductive discharge process it is considerably slower versus dissipating the inductive load across the switch. Specifically, you can use the following *current decay formula for flyback diode* to model how long it would take for an inductive load to decay:

$$t_{decay} = \frac{-L_{load}}{R_{load}} * \ln\left(\frac{V_F}{V_F + (I_0 * R_{load})}\right) \quad (1)$$

For example, suppose there was a 100-mH inductive load that had an initial current of 1 A and a series load resistance of 10 Ω. Also presume that the design is using a standard diode with a forward voltage drop of 0.7 V. Plugging this into the previous formula yields the example flyback current decay as follows:

$$t_{decay} = \frac{-0.100}{10} * \ln\left(\frac{0.7}{0.7 + (1 * 10)}\right) \quad (2)$$

This calculates out to a total decay time of 27.3 ms. As a comparison, looking at the same loading conditions being discharged over the integrated VDS clamp of the TPS1H100, this would equate to a discharge time of approximately 1.76 ms with a 18-V supply rail and 70-V integrated VDS clamp (see the *How To Drive Resistive, Inductive, Capacitive, and Lighting Loads With Smart High Side Switches Application Report* for details on this calculation). One common mitigation to this problem is to replace the standard flyback diode with a Zener diode and regular diode in parallel with the load as Figure 2-2 shows:

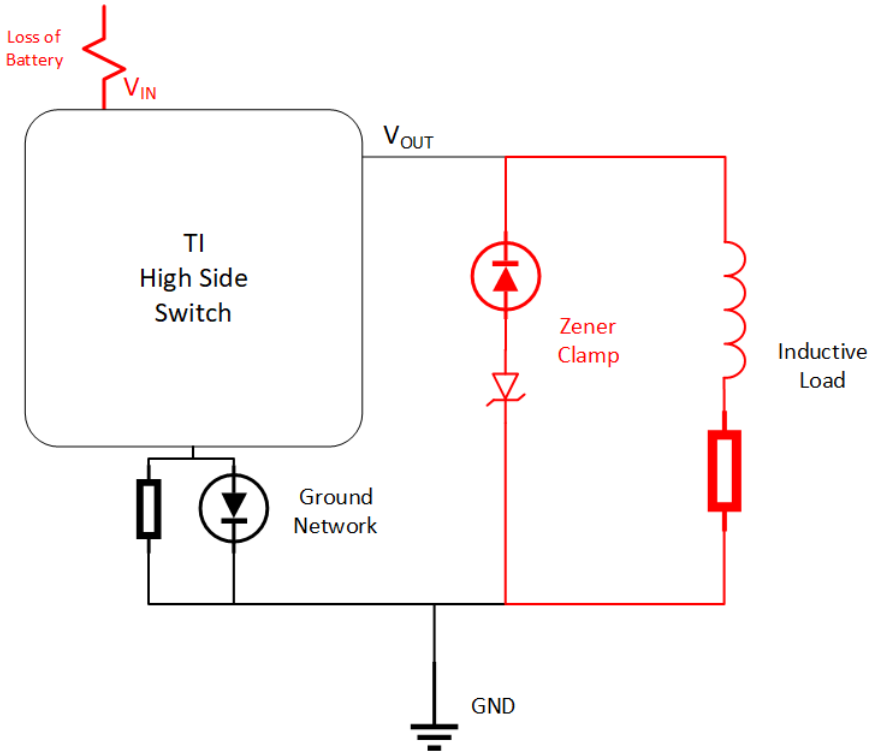

Figure 2-2. Zener Diode for Inductive Loading

In this scenario, the Zener diode allows the voltage spike being caused by the discharging inductor to be clamped at a higher voltage level versus the normal diode. This essentially leads to an output potential on the load of the negative Zener voltage of the Zener diode. The normal diode is placed in series with the Zener diode to prevent any forward biasing of the Zener diode. Using the same loading conditions as previously stated in Equation 2 and using a Zener voltage of something like 10 V, the following Zener calculation is attained:

$$t_{decay} = \frac{-0.100}{10} * \ln(\frac{10}{10 + (1 * 10)}) \quad (3)$$

This leads to a total current decay time of the inductor of 6.9 ms. Increasing the Zener voltage of the diode results in a quicker discharge time; however, it also results in a high potential present on the output pin. Care must be taken to ensure downstream power components can handle the Zener voltage chosen.

It is also important to note that when a loss of battery condition occurs, a sudden and sharp decrease of the input voltage will be seen. If there is not sufficient capacitance on the input of the high-side switch, this can cause a fault condition where the negative voltage of the Zener clamp will be seen on the input of the switch itself. In this fault condition, the negative voltage on the supply pin will cause current to be drawn in through both the GND pin as well as the control and sense pins of the high-side switch. For TPSxHxx devices, if there is no diode on the GND pin of the high-side switch and there is sufficient current being injected into the GND pin, the parasitic latch on described in Section 1.3 might occur.

CAUTION

With a negative voltage on the input the ESD cells of the device can potentially break down and cause damage to the device. To mitigate the risk of this fault condition from happening the following design considerations are recommended:

- A diode on the GND pin of the high-side switch to block any negative current (follow the guidance in the device data sheet)
- A resistor on the GND pin of the high-side switch to pull the device ground to 0 V during a normal (no loss of battery) inductive turnoff
- Sufficient capacitance on the VS pin of the high-side switch to allow the internal FET to discharge and prevent the VS pin from going negative
- A unidirectional TVS diode from system ground to the VS pin to prevent the VS pin from going excessively negative (where possible)

Alternatively, if the flyback diode configuration is not possible due to size constraints or timing requirements it is possible to discharge small inductive load via the ground protection network on the TI high-side switch and serial protection resistors connected to the microcontroller. With this method the majority of the current is dissipated by both the protection resistors connected in series with the microcontroller pins and the ground resistor connected to the high-side switch. Figure 2-3 provides an illustration of this:

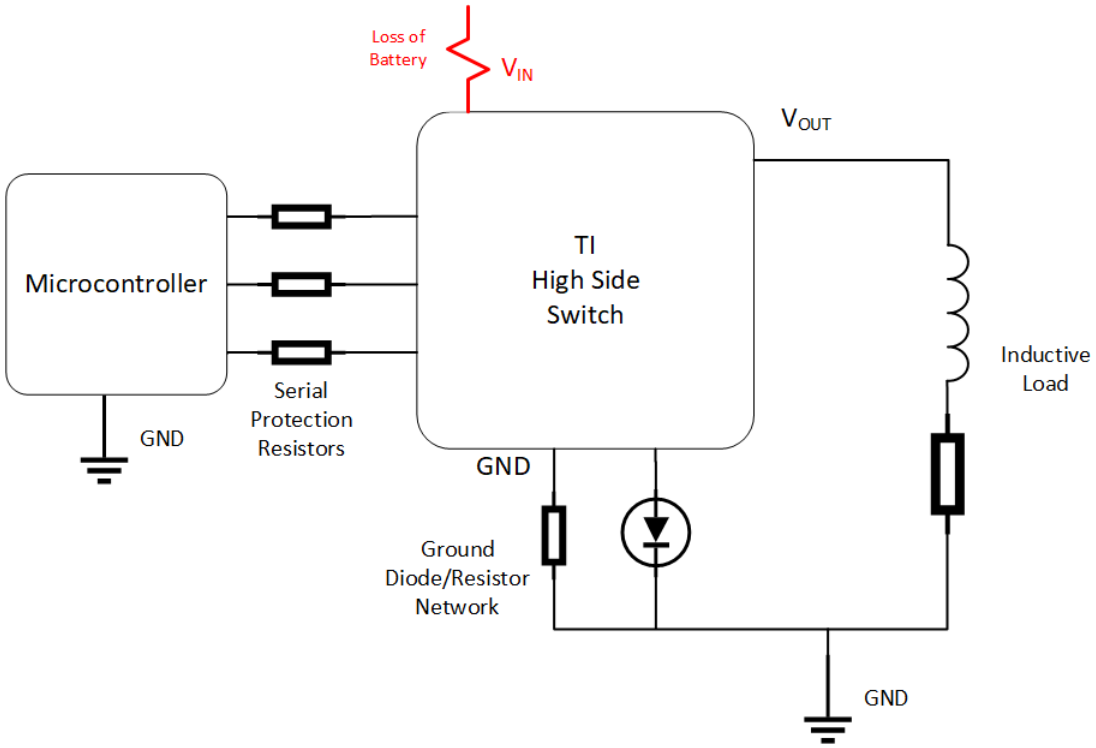

Figure 2-3. Series Resistor Protection

Note that this only works for very small inductances on the load that can mainly be attributed to cable lengths and parasitic values that typically equate to a few µH. In this setup, there are protections to prevent an overvoltage and this solution relies exclusively on the current-limiting capabilities of the protection/ground resistors as well as the robustness of the input/output pins of the high-side switch.

Trademarks

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 21, 2020 to July 16, 2020 (from Revision * (June 2020) to Revision A (July 2020)) **Page**

- Updated title of document to include *Loss of Battery*..... 2
- Added *Loss of Battery Conditions* section..... 8

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265