Application Report

Comparison of TPS6290x vs. TPS621x0

Nicole Lemieux, Tahar Allag

ABSTRACT

The TPS6290x family (TPS62903, TPS62902, TPS62901) is the next generation to the TPS621x0 (TPS62130, TPS62140, TPS62150) family. This application note goes through in detail the improvements that were made from the previous version to the new and how those changes benefit the designer. Key concepts discussed further:

- Feature sets contribute to the smaller solution size
- Less power loss achieved by reduced quiescent current and improvements to the overall efficiency
- Increased flexibility enabling the applicability to a wide range of applications

Table of Contents

List of Figures

List of Tables

Trademarks

AEE™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

Technology is constantly improving – sometimes by leaps and bounds, sometimes by microscopic steps. What is overlooked most of the time, is how those small changes lead to the ground-breaking changes. Each improvement is an improvement on the previous platform – all the way back to the cave men. Today's achievements stand on the shoulders of those who came before. The same goes for buck converters. The TPS6290x family is the next generation of 17V, low Iq, high efficiency, buck converters that improved upon the previous family TPS621x0. Table 1-1 shows the key features of each product and the improvements on the latest generation family. Each improved feature contributes to the leaps forward in the family. In turn, the improved device, a small part of a design, contributes to ground-breaking advancements in technology. But what does *improved* really mean? To understand how technology has improved, this application report provides a comparison of the previous version to the new version, as well as an explanation of how the changes benefit the user more than the previous version.

Table 1-1. Feature comparison of TPS621x0 and TPS6290x

Features	TPS621x0	TPS6290x	Improvements
VOUT	0.9 V to 6 V	0.4 V to 5.5 V	Supports lower Vout down to 0.4 V
Typical quiescent current	17uA	4uA	76% lower Iq
FB accuracy (-40$^{\circ C}$< T_J <125$^{\circ C}$)	1.8%	<1%	44% tighter Vref accuracy
Package size	3.0mmx3.0mm QFN	1.5mmx2.0mm QFN	67% smaller package
Smart configuration	No	Yes	Fewer external components needed to configure device
Junction Temperature	-40C to 125C	-40C to 150C	Supports higher Tj up to 150C
Switching Performance	2.5MHz	2.5MHz and 1MHz	Provides Adj Fsw
$R_{DS(ON)}$	120mΩ/50mΩ	62mΩ/22mΩ	Less power loss
Efficiency (12Vin, 1.2Vo, 2.2uH, 1MHz, 3 A)	78.8%	84%	Improved efficiency
Automatic Efficiency Enhancement	No	Yes	High efficiency for varying duty cycles
Capacitive discharge	Using PG	Using Smart Config	Achieved internally when selected
VSET	No	Yes	This allows for internal divider that has lower BOM count and better overs systems accuracy

2 Power Density

Power density is a term created to describe the power output of a device compared to its size. This is especially important in space constrained applications, or high functionality applications. These applications are mainly concerned with the space on the XY board area when talking about power density, but the Z (height) dimension can also be taken into consideration for total volume if desired. By shrinking the solution area, increasing the power output under similar conditions, or a combination of the two, the power density is positively impacted. As an example, comparing the 3-A rated parts in a case with 12 V on the input, 1.2 V on the output and in an ambient temperature of 65C, the TPS6290x is able to give the full 3-A load for a power density of 120mA/mm^2. The TPS621x0 provides 2.7 A for a power density of 68mA/mm^2 due to more power losses in the device. Section 3 provides additional detail of how the total solution size went from 40mm^2 for TPS62130 to a solution size of 25mm^2 in TPS62903. Section 4 describes how efficiency and thermals impact how much power is able to get out of a part.

$$PD = \frac{Current\ (mA)}{Area\ (mm^2)} \tag{1}$$

3 Achieving a Smaller Solution

3.1 Smaller Package and Fewer External Components

The QFN package of TPS6290x is one third the size of the previous generation, however the size of the package is not the only thing that has shrunk. The total solution size is reduced by more than 30% as well. To achieve both of these reductions, TPS6290x has decreased the number of pins on the package from 16 to 9, allowing the package to shrink and decreasing the passives needed to configure the device. The result saves precious board space, BOM costs and design time.

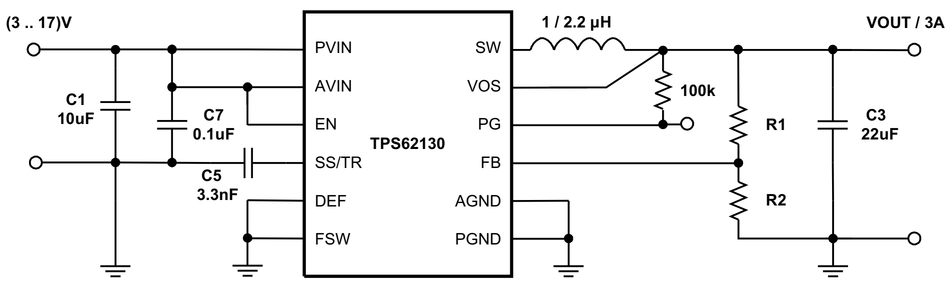

Figure 3-1. Typical application schematic of the TPS621x0

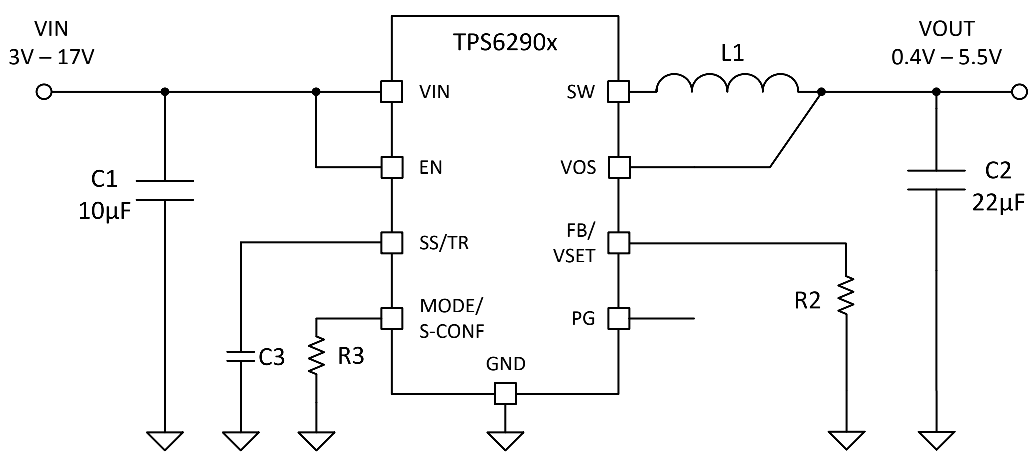

Figure 3-2. Typical application schematic of the TPS6290x

3.2 Smart Configuration Pin

The smart configuration pin is one of the primary contributors to the space savings and a key differentiator between the next generation devices and their predecessors. The SCONFIG pin allows the user the flexibility to select the settings of four features (feedback/voltage set, switching frequency, FPWM/PFM, and output discharge) with only one resistor. In the previous generation, each of these features would have to be configured individually. There are several advantages associated with this pin, too many to discuss in this document. To learn more about smart config pins and all of their design benefits, reference the document *Multi-Function Pins for Easy Designing*.

3.3 VSET

Using the SCONFIG pin in conjunction with the FB/VSET pin, can be used to save an additional one or two resistors when setting the output voltage. Typically, to set an output voltage, a resistor divider is used on the feedback pin. The advantage to using the resistor divider is you are able to choose any output value in the output voltage range. Both the TPS621x0 and TPS6290x have the ability to use a resistor divider to configure the Vout. Several applications use common voltages at point of load, so TPS6290x has added the ability to select an output value from one of 16 common voltages preset options through the VSET function. These values vary from 0.4 V to 5.5 V. If one of those preset output voltages is desired for a design, the VSET function can be used to save one or even both resistors (if left floating) when configuring the output voltage, as shown in Figure 3-3. The resulting total solution size is 25mm^2.

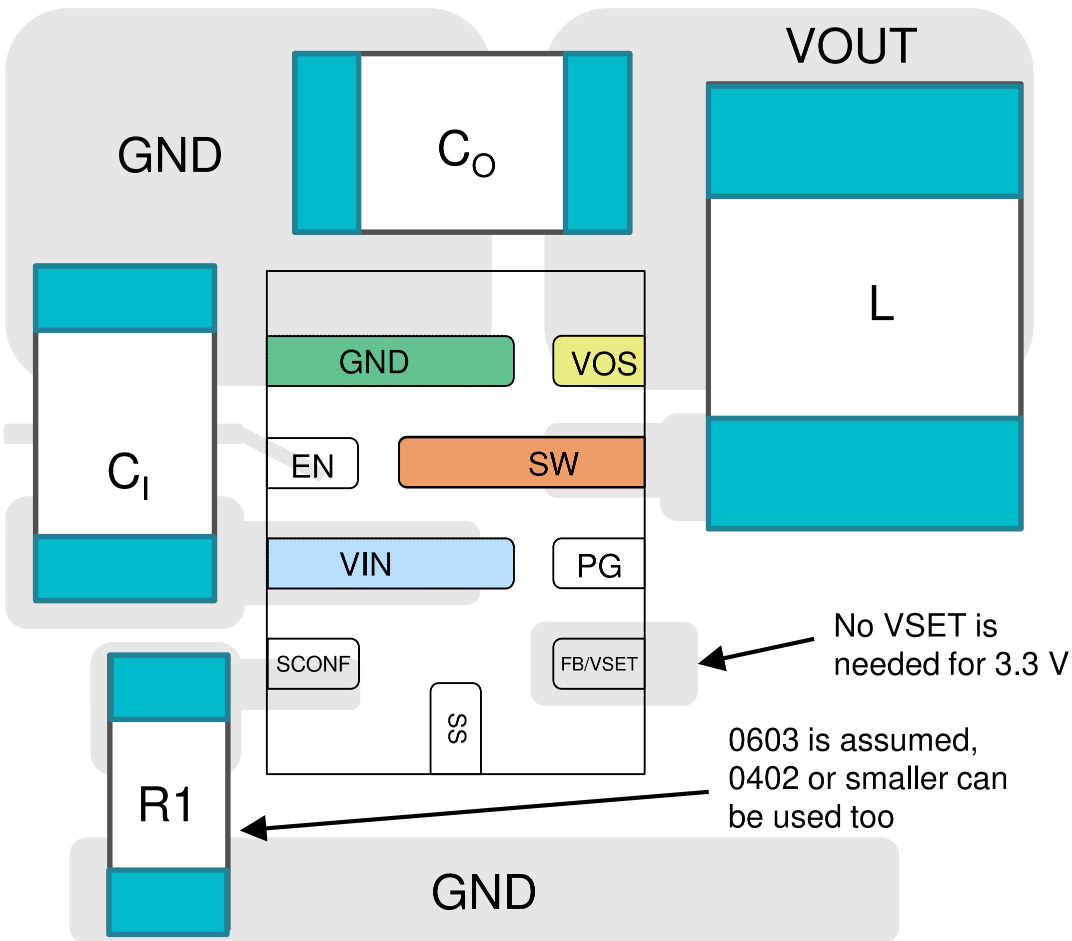

Figure 3-3. Configuration for the Smallest Solution Size Using TPS6290x

4 Reducing Power Loss

4.1 Junction Temperature

The TPS6290x has extended the junction temperature to 150C vs. the 125C of the TPS621x0. This allows the device to be used at higher ambient temperatures with higher loads. With the 45C/W $R_{\Theta JA}$ of the TPS621x0, and with an ambient temperature of 100C, the device is allowed to dissipate only 550mW of power to reach the max junction temperature of 125C. Whereas, the TPS6290x, has more than 700mW of allowable power to dissipate before the max junction temperature of 150C is reached. This translates to how much load the device can deliver under the same ambient temperature, VIN, and VOUT condition.

For example, if we compare the two devices under 1MH switching frequency, 17-V input, 1.2-V output, and 100C ambient. The TPS62130 can deliver only approximately 2 A whereas the TPS6290X can deliver 3 A before the max junction temperature is reached. For the TPS621X0 to deliver full load of 3 A, the ambient temperature has to be reduced to 80C.

4.2 Automatic Efficiency Enhancement (AEE™)

The AEE™ feature in the TPS6290x provides highest efficiency over the entire input voltage and output voltage range by automatically adjusting the converter's switching frequency when 2.5MHz is selected. This is achieved by setting the predictive off-time of the converter. The efficiency of a switched mode converter is determined by the power losses during the conversion. The efficiency decreases when VOUT decreases and or VIN increases. In order to keep the efficiency high over the entire duty cycle range (VOUT/VIN ratio), the switching frequency is adjusted while maintaining the ripple current. Equation 2 shows the relationship between the inductor ripple current, switching frequency and duty cycle.

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{sw}} \right) \tag{2}$$

Efficiency increases by decreasing switching losses and by preserving high efficiency for varying duty cycles while the ripple current amplitude remains low enough to deliver the full output current without reaching current limit. The AEE™ feature provides an efficiency enhancement for various duty cycles, especially for lower Vout values, where fixed frequency converters suffer from a significant efficiency drop. Furthermore, this feature compensates for the very small duty cycles of high VIN to low VOUT conversion, which limits the control range in other topologies.

4.3 1MHz and 2.5MHz Switching Frequencies

The TPS6290x switching frequency can be set to 1MHz or 2.5MHz using the smart configuration pin. This is useful to provide the user the flexibly to set the switching frequency that fits the applications. To improve the efficiency and reduce switching losses of the converter, 1MHz can be selected, with the trade-off of using a larger inductor. This selection is ideal for applications that may not have huge space constrains, but efficiency or thermals are the main concern. For applications needing the smaller inductor, optimized overall solution size, and can afford a slight drop in efficiency, 2.5MHz is the ideal choice.

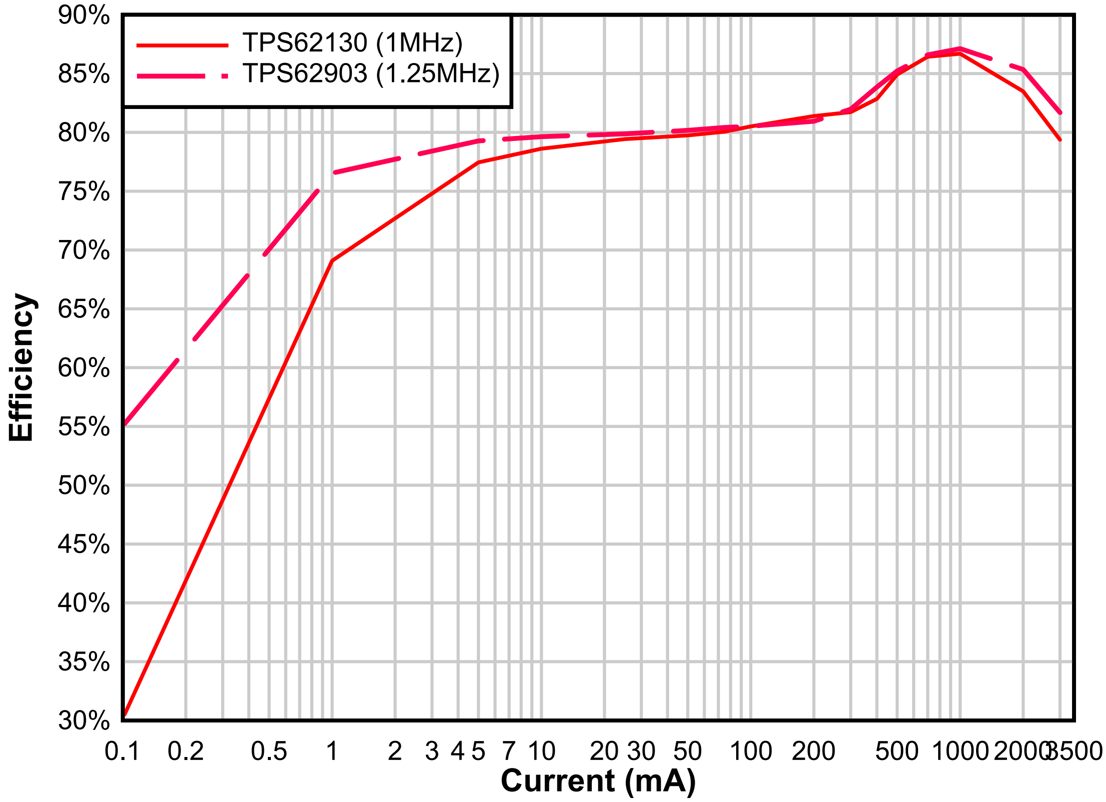

Figure 4-1. Efficiency Curves of TPS6290x vs. TPS621x0, VIN=12V, VO=1.2V, L=2.2uH (XGL4020-222ME)

4.4 Auto PFM/PWM vs. Forced PWM

To receive the best efficiency possible at light loads, the user can select the Auto Pulse Frequency Modulation, also called Pulse Width Modulation, mode. Auto PFM/PWM increases the efficiency by skipping switching pulses and reducing the device's current consumption. Alternately, Forced PWM forces the device to operate at fixed frequency across load, this has some efficiency impact at light load but the user can easily predict the operating frequency and set filters as needed. The user can choose between these modes using the SCONFIG pin discussed previously.

5 Application Flexibility

5.1 Quiescent Current

Low Iq is a key spec for the applications where the device is operated in standby or shutdown mode for the majority of the time, so they are not drawing unnecessary power while not in use. For battery powered applications, the quiescent current is critical to extending the life of the battery and improves light load efficiency. The TPS621x0 has low quiescent current of 17uA. The TPS6290x quiescent current is reduced even further to 4uA. The battery in these applications are meant to last an extended amount of time without having to be replaced. The reduction of the Iq by 76% will reduce the amount of current being drawn from the battery, therefore extending the battery life significantly.

5.2 Lower and More Accurate Output Voltages

TPS621x0 supports 0.9V as minimum output with a 1.8% Vout accuracy combined with the accuracy of the two feedback resistors used. This covers a lot of use cases, however not all. There are applications that require lower than 0.9 Vout, or a tighter spec for Vout accuracy and have previously been unable to use the TPS621x0 because of these requirements. TPS6290x opens up the opportunity for these applications to take advantage of its high-performance feature set by supporting as low as 0.4 V output voltage when using VSET and as low as 0.6 V using the feedback resistor option with a <1% Vout accuracy across full temperature range. If VSET option is selected, the external resistors are not needed and thus the total system accuracy is improved for the fact that the external feedback resistor accuracy is no longer added to the feedback loop.

5.3 Capacitive Discharge

In some applications, the output voltage needs to get to zero as soon as the device is disabled. For that, an internal discharge circuit is implemented inside the device to bleed off the remaining charge of the output capacitor as soon as the device is disabled. The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once TPS6290x has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is deactivated, in thermal shutdown or in undervoltage lockout. The user can turn this feature on or off using the smart configuration pin.

In the TPS621x0, this feature is implemented using the PG pin. The TPS621x0A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to VOUT through a resistor can be used to discharge VOUT in those cases. The discharge rate can be adjusted by the pull up resistor, which is also used to pull up the PG pin in normal operation.

6 Summary

The comparison between the TPS621x0 family and the TPS6290x family have exemplified the improvements in the new generation and how those improvements benefit the design the device is in. Decreased solution size, increased efficiency, implementation of the SCONFIG pin, and more all combine together to make significant advancements in the buck converter world and the technology of tomorrow.

7 References

- Texas Instruments, Understanding the Trade-offs and Technologies to Increase Power Density marketing white paper.
- Texas Instruments, Multi-Function Pins for Easy Designing application brief.
- Texas Instruments, Which Pinout is Best? article.