Application Note

Powering the AM62x with the TPS65219 PMIC

ABSTRACT

This application note discusses the TPS65219 power management IC (PMIC) full feature-set powering the AM62 Sitara™ processor and principal peripherals. The power delivery network (PDN) described in this document can be used as a guide for integrating the TPS65219 Power Management IC (PMIC) into industrial or automotive applications powering the Texas Instruments AM62x Sitara Processor. An orderable part number comparison table details the configurations of several factory programmed TPS65219 variants that can support different AM62x use cases. Example power maps are provided to assist the design process. For any questions or technical support, use the Power Management E2E forum.

Table of Contents

List of Figures

List of Tables

Trademarks

Sitara™ is a trademark of Texas Instruments.
Arm® is a registered trademark of Arm Ltd.
All trademarks are the property of their respective owners.

1 Introduction

The TPS65219 PMIC is a cost and space optimized solution developed to power the AM62x processor and its principal peripherals. TPS65219 has flexible mapping and comes in several factory programmed orderable part numbers to support different AM62x use cases. A hardware solution is readily available with the AM62x SK EVM. The AM62x is the latest in the Sitara™ family of Arm® processors, built with features to support embedded 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options. To be used in applications from Human Machine Interfaces (HMI) to 3D Point Cloud, this processor provides powerful computing while supporting power management features designed for portable or power-sensitive systems. The AM62x processor requires at minimum power for seven main rails. These include the core supply (VDD_CORE), RAM supply (VDDR_CORE), DDR PHY IO supply (VDDS_DDR), 1.8 V VDDA analog supply and the 1.8V/3.3 V IO supplies and analog IO rails (VDDSHV). Powering a processor such as the AM62x family demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 TPS65219 Overview

The TPS65219 PMIC contains seven regulators; 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) can be configured as load switch and bypass mode to support dynamic SD card voltages, while LDO3 and LDO4 (2×300 mA) can be configured as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. Table 2-1 shows a summary of the voltage and current capabilities for each of the analog resources. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65219 PMIC provides the full power package to supply the AM62x SoC, as well as many other SoCs.

This PMIC has two versions, TPS65219 supports industrial applications with a temperature range of -40°C to +105°C ambient and TPS65219-Q1 supports automotive applications that requires an extended temperature range of -40°C to +125°C ambient. Table 2-2 shows the differences between the industrial and automotive PMIC variants.

Table 2-1. TPS65219 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5 V - 5.5 V	0.6 V - 3.4 V	3.5 A	• 2.3 MHz switching frequency • Dynamic voltage scaling • Programmable power sequencing and default voltages. • Integrated voltage supervisor for undervoltage.
BUCK2	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
BUCK3	2.5 V - 5.5 V	0.6 V - 3.4 V	2 A	
LDO1	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	• Programmable power sequencing and default voltages. • Configurable as load switch and bypass-mode. • Integrated voltage supervisor for undervoltage
LDO2	1.5 V - 5.5 V (LDO, Load-Switch) 1.5 V - 3.4 V (Bypass)	0.6 V - 3.4 V (LDO) 1.5 V - 3.4 V (Bypass)	400 mA	
LDO3	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	• Programmable power sequencing and default voltages. • Configurable as load switch • Integrated voltage supervisor for undervoltage
LDO4	2.2 V - 5.5 V	1.2 V - 3.3 V	300 mA	

Table 2-2. TPS65219 vs TPS65219-Q1

Feature	TPS65219 (Industrial)	TPS65219-Q1 (Automotive)
Target Processor	AM62x 13 mm x 13 mm, 0.5-mm pitch, 425-pin FCCSP BGA (ALW)	AM62x-Q1 17.2 mm x 17.2 mm, 0.8-mm pitch, 441-pin FCBGA (AMC)
Switching Frequency	Up to 2.3 MHz Quasi-fixed frequency • Auto-PFM • Forced-PWM	Up to 2.3MHz . Capable of either quasi-fixed frequency or fixed-frequency depending on device configuration Quasi-fixed frequency • Auto-PFM • Forced-PWM Fixed-frequency • Spread spectrum available
Operating Free-Air Temp TA	40C to 105C	40C to 125C
Operating Junction Temp TJ	-40C to 125C	-40C to 150C
Functional Safety Capable	No	Functional Safety Capable (TI Quality managed process, Functional safety FIT rate calculation, and Failure Mode Distribution is available)
Package	Two package options • 4 mm × 4 mm, 0.4 mm pitch VQFN • 5 mm × 5 mm, 0.5 mm pitch VQFN	One package option • 5 mm × 5 mm, 0.5 mm pitch VQFN • (Wettable-Flank)

2.1 TPS65219 Functional Block Diagram

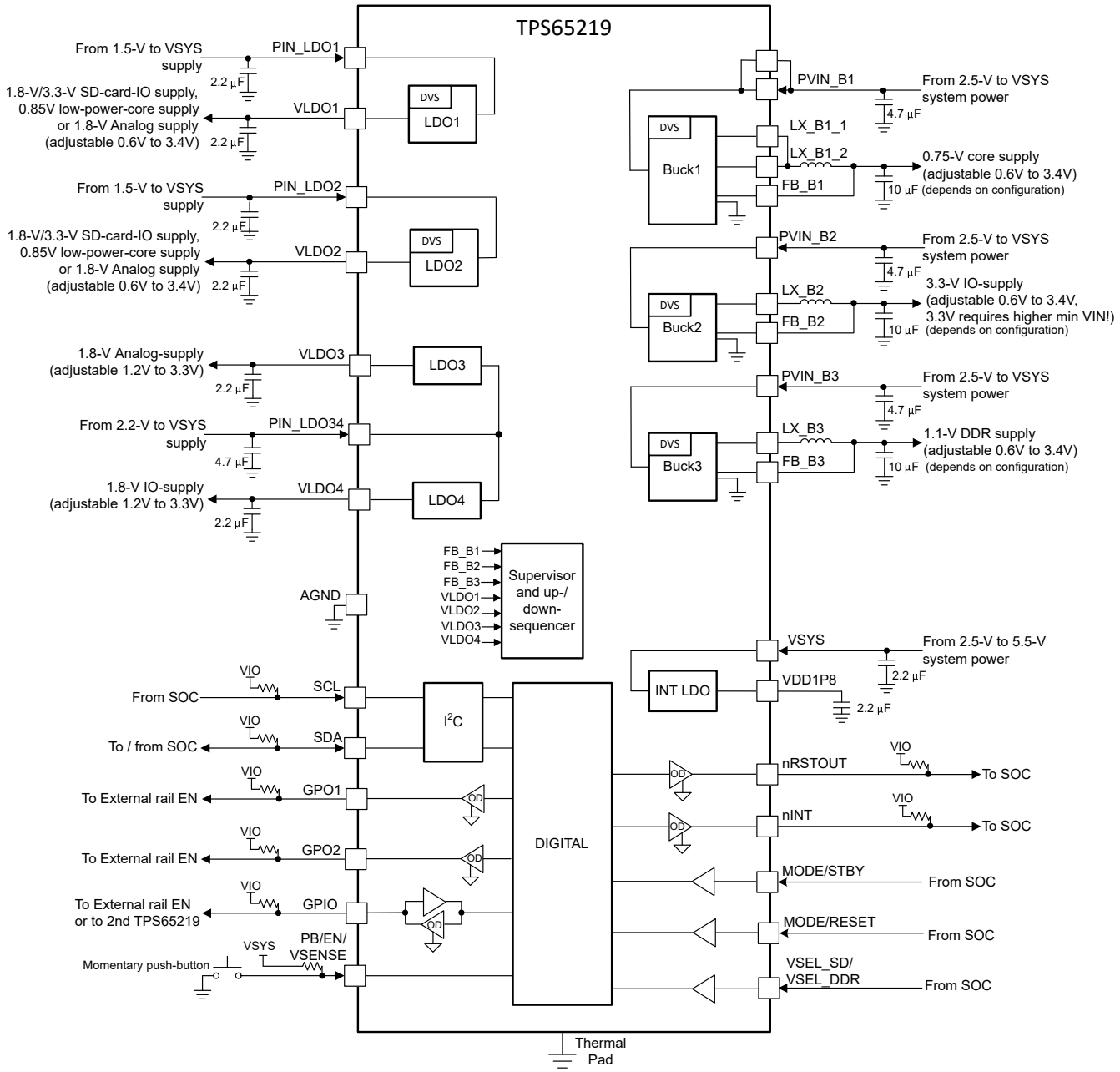


Figure 2-1. TPS65219 Functional Block Diagram

3 TPS65219 Variants

There are multiple variants of the TPS65219 PMIC that come factory programmed with unique register settings to power the AM62x processor and peripherals. Selecting the correct orderable part number (OPN) depends on the application use case, specially the input supply, memory type and CORE voltage. Section 3.1 compares the main NVM settings for the orderable part numbers that are currently available for industrial applications. Similarly Section 3.2 shows the main NVM settings for the OPN that is currently available to support automotive applications. These tables also includes the resources that are available to support new designs, including the technical reference manuals and AM62x starter kit. For additional detailed information, please refer to the device data sheet.

Note

Each orderable part number has a technical reference manual (TRMs) that shows the default register settings. The NVM register settings are identified with a "X" in the reset column of the register map in the data sheet. If none of the pre-programmed orderable part numbers (OPNs) meet the application requirements, refer to Section 4 for information about the options for a custom NVM.

3.1 TPS65219 NVMs for Industrial Applications

Table 3-1. TPS65219 NVMs for AM62x Industrial Applications

		TPS6521901	TPS6521902	TPS6521903	TPS6521904	TPS6521907	TPS6521908
Use Case	**Vsys**	**5 V**	**3.3 V**	**3.3 V**	**3.3 V**	**5 V**	**3.3 V**
	VDD_CORE (3)	**0.75 V**	**0.75 V**	**0.75 V**	**0.85 V**	**0.85 V**	**0.85 V**
	External Memory	**DDR4**	**LPDDR4**	**DDR4**	**DDR4**	**DDR4**	**LPDDR4**
Technical Reference Manual (TRM)		SLVUCH3	SLVUCL0	SLVUCJ2	SLVUCL1	SLVUCL9	SLVUCM0
Hardware (2)		TPS65219EVM		AM62B starter kit with PMIC	AM62B starter kit with PMIC		
BUCK1	**Vout**	0.75 V	0.75 V	0.75 V	0.85 V	0.85 V	0.85 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
BUCK2	**Vout**	3.3 V	1.8 V	1.8 V	1.8 V	3.3 V	1.8 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
BUCK3	**Vout**	1.2 V	1.1 V	1.2 V	1.2 V	1.2 V	1.1 V
	Bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth	High bandwidth
LDO1	**Vout**	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)	3.3 V/1.8 V (Bypass)
LDO2	**Vout**	0.85 V	0.85 V	0.85 V	1.8 V	1.8 V	1.2 V (Disabled)
LDO3	**Vout**	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
LDO4	**Vout**	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
GPIOs	**GPO1**	Enabled	Disabled	Disabled	Disabled	Enabled	Disabled
	GPO2	Disabled	Enabled	Enabled	Enabled	Disabled	Enabled
	GPIO	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
MODE/RESET	**Config**	Warm Reset	Warm Reset	Warm Reset	Warm Reset	Warm Reset	Warm Reset
	Polarity	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset	High= Normal operation Low=Warm Reset
MODE/SBY	**Config**	Mode and Standby	Mode and Standby	Mode and Standby	Mode and Standby	Mode and Standby	Mode and Standby
	Polarity	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM	High=Active State & Forced-PWM Low=Stby State & Auto-PFM

Table 3-1. TPS65219 NVMs for AM62x Industrial Applications (continued)

		TPS6521901	TPS6521902	TPS6521903	TPS6521904	TPS6521907	TPS6521908
Use Case	**Vsys**	**5 V**	**3.3 V**	**3.3 V**	**3.3 V**	**5 V**	**3.3 V**
	VDD_CORE (3)	**0.75 V**	**0.75 V**	**0.75 V**	**0.85 V**	**0.85 V**	**0.85 V**
	External Memory	**DDR4**	**LPDDR4**	**DDR4**	**DDR4**	**DDR4**	**LPDDR4**
VSEL_SD/DDR	**Config**	SD	SD	SD	SD	SD	SD
	Rail	LDO1	LDO1	LDO1	LDO1	LDO1	LDO1
	Polarity	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V	High = LDO1_VSET Low = 1.8 V
EN/PB/VSENSE pin config		Enable	Push-button	Push-button	Push-button	Enable	Enable
First Supply detection (1)		Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

(1) First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.

(2) The AM62 starter kit comes with the TPS6521904 PMIC by default, supporting VDD_CORE=0.85V. To support VDD_CORE=0.75V, the following changes are required: TPS6521904 PMIC needs to be replaced with TPS6521903, R699 needs to be uninstalled, and R123 needs to be mounted.

(3) See Section 5 for a comparison of the two VDD_CORE operating points.

3.2 TPS65219-Q1 NVMs for Automotive Applications

Table 3-2. TPS65219-Q1 NVMs for AM62x-Q1 Automotive Applications

		TPS6521920W-Q1
Use Case	**Vsys**	**3.3 V**
	VDD_CORE(2)	**0.75 V**
	External Memory	**LDDR4**
Technical Reference Manual (TRM)		SLVUCN8
Hardware		AM62x starter kit for low-power Sitara processors
BUCK1	Vout	0.75 V
	Bandwidth	High bandwidth
BUCK2	Vout	1.8 V
	Bandwidth	High bandwidth
BUCK3	Vout	1.1 V
	Bandwidth	High bandwidth
LDO1	Vout	3.3 V/1.8 V (Bypass)
LDO2	Vout	0.85 V
LDO3	Vout	1.8 V
LDO4	Vout	2.2 V
GPIOs	GPO1	Disabled
	GPO2	Enabled
	GPIO	Disabled
MODE/RESET	Config	Warm Reset
	Polarity	High= Normal operation Low=Warm Reset
MODE/SBY	Config	Mode
	Polarity	High=Forced-PWM Low=Auto-PFM
VSEL_SD/DDR	Config	SD
	Rail	LDO1
	Polarity	High = LDO1_VSET Low = 1.8 V
EN/PB/VSENSE pin config		Enable

Table 3-2. TPS65219-Q1 NVMs for AM62x-Q1 Automotive Applications (continued)

		TPS6521920W-Q1
Use Case	**Vsys**	**3.3 V**
	VDD_CORE(2)	**0.75 V**
	External Memory	**LDDR4**
First Supply detection (1)		Enabled

(1) First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.
(2) See Section 5 for a comparison of the two VDD_CORE operating points.

4 TPS6521905 User-Programmable NVM

Figure 4-1 shows the supply options that are available. This Application note described the pre-configured NVMs that are available to power the AM62x for different use cases. If none of the orderable part numbers (OPNs) described in this document meet the application requirements or minor changes to the default settings are needed, a custom NVM is required. For high volume opportunities, TI creates a new orderable part number with custom NVM settings. For low volume opportunities, customers can use the resources listed in Table 4-1 to program the PMIC in a production line or through third party programming service.

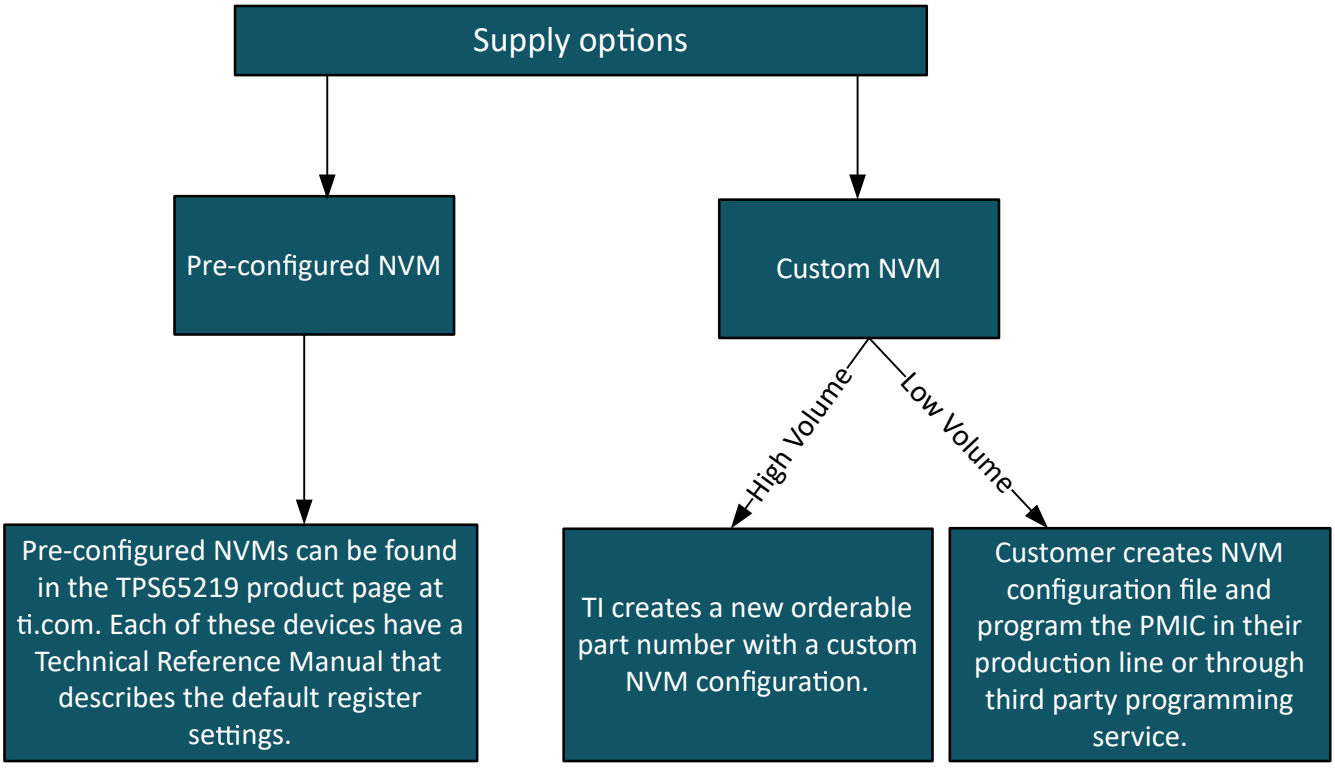


Figure 4-1. Supply Options

Table 4-1. TPS6521905 Programming Resources

Resource	Link
Programming Guide	TPS65219 Non-Volatile Memory (NVM) Programming Guide
Graphical User Interface (GUI)	TPS65219 graphical user interface
Socketed EVM	TPS65219 non-volatile memory (NVM) programming board
TPS6521905 data sheet	User-programmable power management IC (PMIC) with three step-down DC/DC converters and four LDOs

5 AM62x Core Voltage Selection

VDD_CORE is the Core supply of the AM62x processor. This domain has two operating points. Table 5-1 compares the 0.75V and 0.85V operating points in terms of frequency, power consumption, power mapping and sequencing requirements. Since AM62x does not support dynamic voltage scaling, different TPS65219 orderable part numbers are used to support the 0.75 V or 0.85 V operating points.

Table 5-1. CORE Voltage Selection

	VDD_CORE	
	0.75 V (Flexible Core)	**0.85 V (Lowest BOM option)**
Maximum operating frequency on A53SS (Cortex-A53x)	Up to 1.25 GHz	Up to 1.4 GHz
Power Consumption	lower power consumption VDD_CORE (1)	higher power consumption (1)
PMIC and Processor Power Mapping	Requires two PMIC rails; One to supply VDD_CORE at 0.75V and a second PMIC rail to supply VDD*R*_CORE at 0.85V. Buck1, when configured to output 0.75V, is used to supply VDD_CORE. LDO2, when configured to output 0.85V, is used to supply VDDR_CORE.	Lowest BOM option. Allows suppling VDD_CORE (Core supply) and VDDR_CORE (RAM supply) from the same PMIC rail. Buck1, when configured to output 0.85V, is used to supply both CORE rails.
Sequencing	Power-up and power-down sequence requirements. VDD_CORE needs to ramp up before VDDR_CORE. VDD_CORE needs to ramp down after VDDR_CORE.	No sequencing requirements for the CORE supplies as they are both supplied by the same PMIC rail.

(1) For information on the processor power consumption, see the AM62x Power Estimation Tool application note.

6 VSYS Voltage Ramp

The TPS65219 power-up sequence is gated by the following main steps: Voltage on VSYS goes above the POR_Rising threshold, PMIC loads the NVM content into the register map and then waits for an ON request before executing the power-up sequence. The first ON request can be bypassed by enabling the first supply detection feature (FSD) in the *PU_ON_FSD* register field. When *PU_ON_FSD*=0x1, PMIC starts executing the power-up sequence after the NVM settings are loaded to the register map, without waiting for an ON request. In this scenario, customers must ensure the pre-regulator supplying the VSYS reaches a stable output voltage before the PMIC starts executing the power-up sequence. The voltage on VSYS must reach the targeted Vout in approximately 2.3ms after VSYS goes above the POR_threshold.

Note

If FSD is enabled (*PU_ON_FSD*=0x1) and VSYS has a slow ramp, PMIC will try to enable the first rail without having the required input to output voltage headroom. This conditions create a fault on the PMIC.

Figure 6-1 shows an example where FSD is enabled and VSYS has a slow ramp.

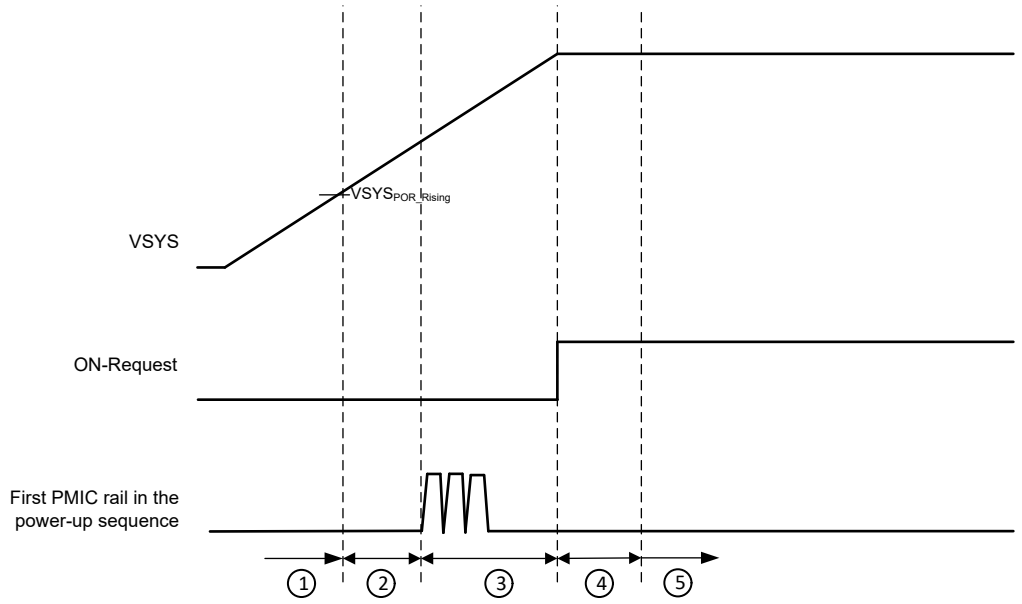
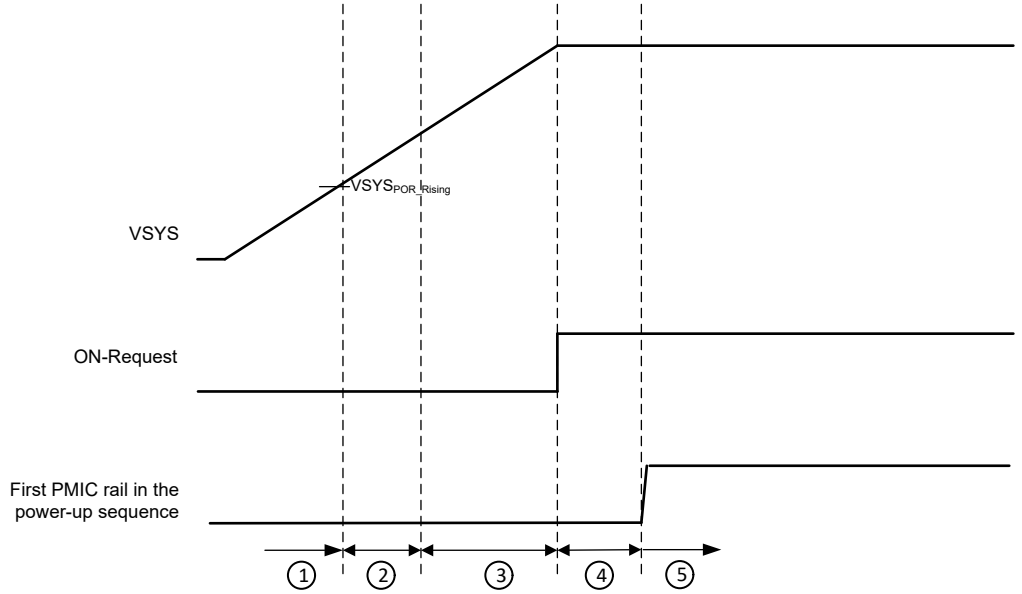


Figure 6-1. VSYS Slow Ramp with FSD Enabled

- **Step 1**: VSYS reaches the POR_Rising threshold.
- **Step 2**: NVM settings are loaded to the registers in approximately 2.3ms.
- **Step 3**: Since FSD is enabled, PMIC starts executing the power-up sequence but the voltage on VSYS is still too low and does not meet the input to output headroom. The first PMIC rail in the power-up sequence shows three voltage peaks which represent the first power-up and the two attempts configured in the retry counter (MASK_RETRY_COUNT).
- **Step 4**: the enable pin goes high and the pin deglitch takes effect.
- **Step 5**: the PMIC is not able to execute the power-up sequence because the device stayed in Initialize state after the power-up attempts in step#3. A power-cycle on VSYS with a faster ramp is required to get the PMIC out of the Initialize state.

Figure 6-2 shows an example where FSD is disabled and VSYS has a slow ramp.



- **Step 1**: VSYS reaches the POR_Rising threshold.
- **Step 2**: NVM settings are loaded to the registers in approximately 2.3ms.
- **Step 3**: Since FSD is disabled, PMIC waits for an ON request to execute the power-up sequence.
- **Step 4**: the enable pin goes high and the pin deglitch takes effect.
- **Step 5**: the PMIC starts executing the power-up sequence starting with the rails assigned to the first slot.

Figure 6-2. VSYS Slow Ramp with FSD Disabled

7 Power Block Diagrams

There are several considerations to take into account when designing the TPS65219 to power the AM62 processor and the peripherals.

- Will the application be using LPDDR4 or DDR4 memory?
- Does an SD card need to be supported?
- What will the system supply voltage be?
- Are there any external discrete ICs that will require fully controlled sequencing?
- Does system application prioritize highest integration or lowest power consumption?

Each of these questions impact the design, configuration, setup, among others, of the power block diagram and plays a role designing the most robust power solution. The sections below describe how the TPS65219 PMIC can supply the AM62x processor on different application requirements.

All the TPS65219 variants described in this application note have LDO1 configured as bypass to supply the SD card dual-voltage I/O (3.3 V and 1.8 V). A processor GPIO control signal with a logic high default value and an external pull-up is used to set SD IO to 3.3 V initially. After the power-up sequence, the processor can set GPIO signal low to select 1.8 V level as needed for high-speed card operation per SD specification. This bypass configuration allows control of the LDO1 voltage from 3.3 V to 1.8 V without the need to establish I2C communication during boot from SD card operations. The bypass configuration on LDO1 requires connecting its input supply pin (PVIN_LDO1) to 3.3 V.

7.1 TPS6521901 Powering AM62x

VSYS = 5 V | Memory: DDR4 | VDD_CORE = 0.75 V

Figure 7-1 shows the TPS6521901 variant powering the AM62x processor on a system with 5 V input supply and DDR4 memory. The 5 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx). Buck1, Buck2 and Buck3 are used to supply VDD_CORE at 0.75 V, 3.3 V VDDSHVx IO and DDR IO respectively. Since Buck2 (3.3 V PMIC rail) is programmed to ramp up first in the power-up sequence, it can be used as the input supply for some of the LDOs to minimize power dissipation. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is used to supply the VDDR_CORE. LDO3 supports the 1.8 V analog domain and LDO4 supports the 2.5 V VPP for the DDR4 memory. This power solution requires an external discrete buck regulator to supply the 1.8 V VDDSHV IO domain. This external discrete can be enabled using the GPO1 of the PMIC. TPS6521901 comes pre-programmed to enable GPO1 in the second slot of the power-up sequence. The external discrete must have active discharge and ramp up to an stable output voltage before the PMIC starts powering up the rails in the next slot. The remaining two general purpose pins (GPIO and GPO2) are free digital resources that are disabled by default but can be enabled through I2C after the PMIC completes the power-up sequence (after nRSTOUT is released).

Note

Refer to the TPS6521901 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

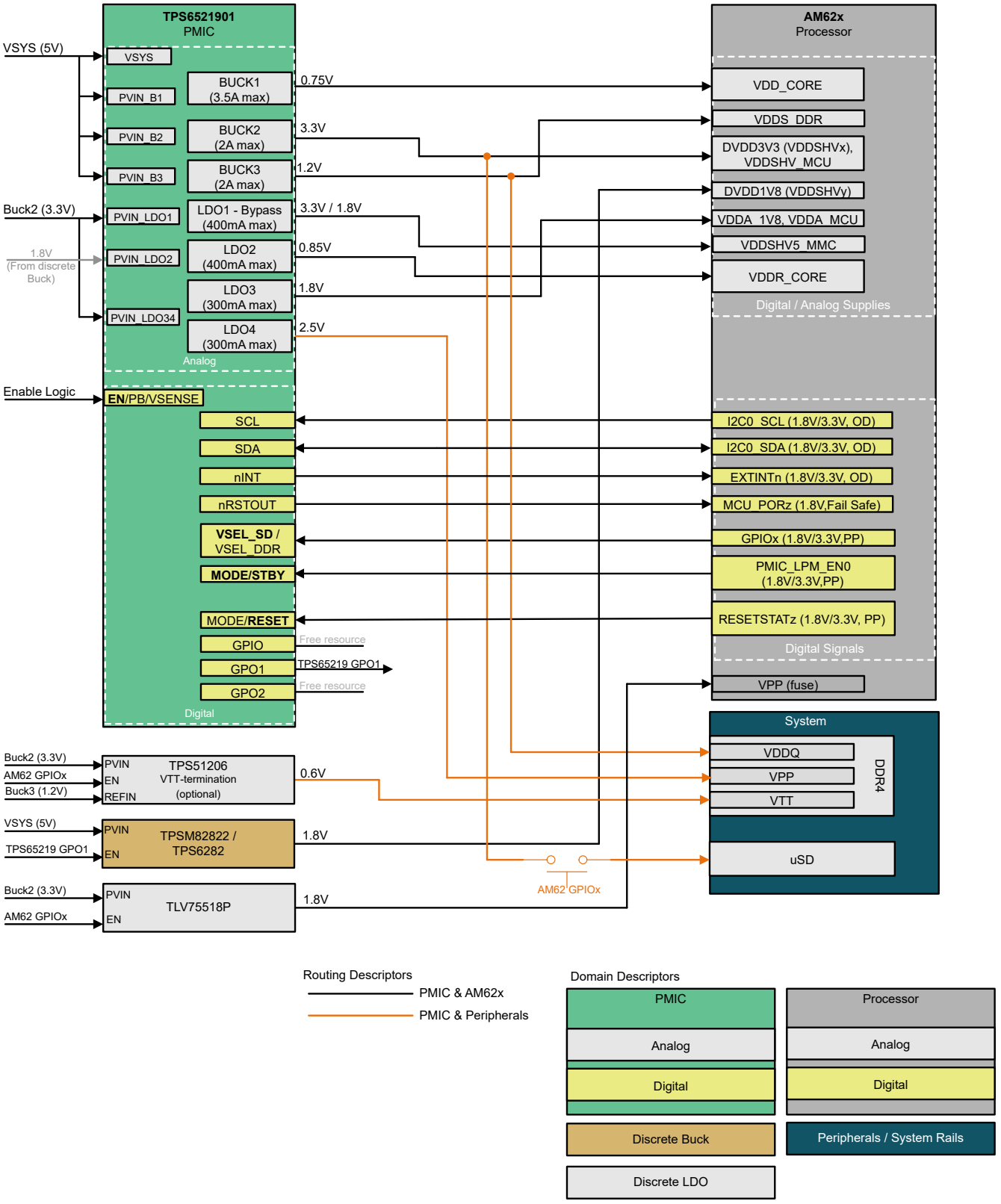


Figure 7-1. TPS6521901 Powering AM62

7.2 TPS6521902 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: LPDDR4 | VDD_CORE = 0.75 V

Figure 7-2 shows the TPS6521902 variant powering the AM62x processor on a system with 3.3 V input supply and LDDR4 memory. Buck1, LDO3, LDO2, and LDO1 are used to supply the same AM62x domains that were described in the previous block diagram. The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 DVDDSH IO domain. This external power switch will be enabled/disabled by the PMIC and must have an active discharge. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence). Buck3 and Buck2 supports the 1.1 V and 1.8 V required by VDDS_DDR and the 1.8 V DVDD3V3 IO domain. They are also used to support the required voltages on the LPDDR4 memory. LDO4 is a free 2.5 V power resource that can be used for external peripherals like the Ethernet PHY. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed.

The TPS6521902 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the TPS6521902 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

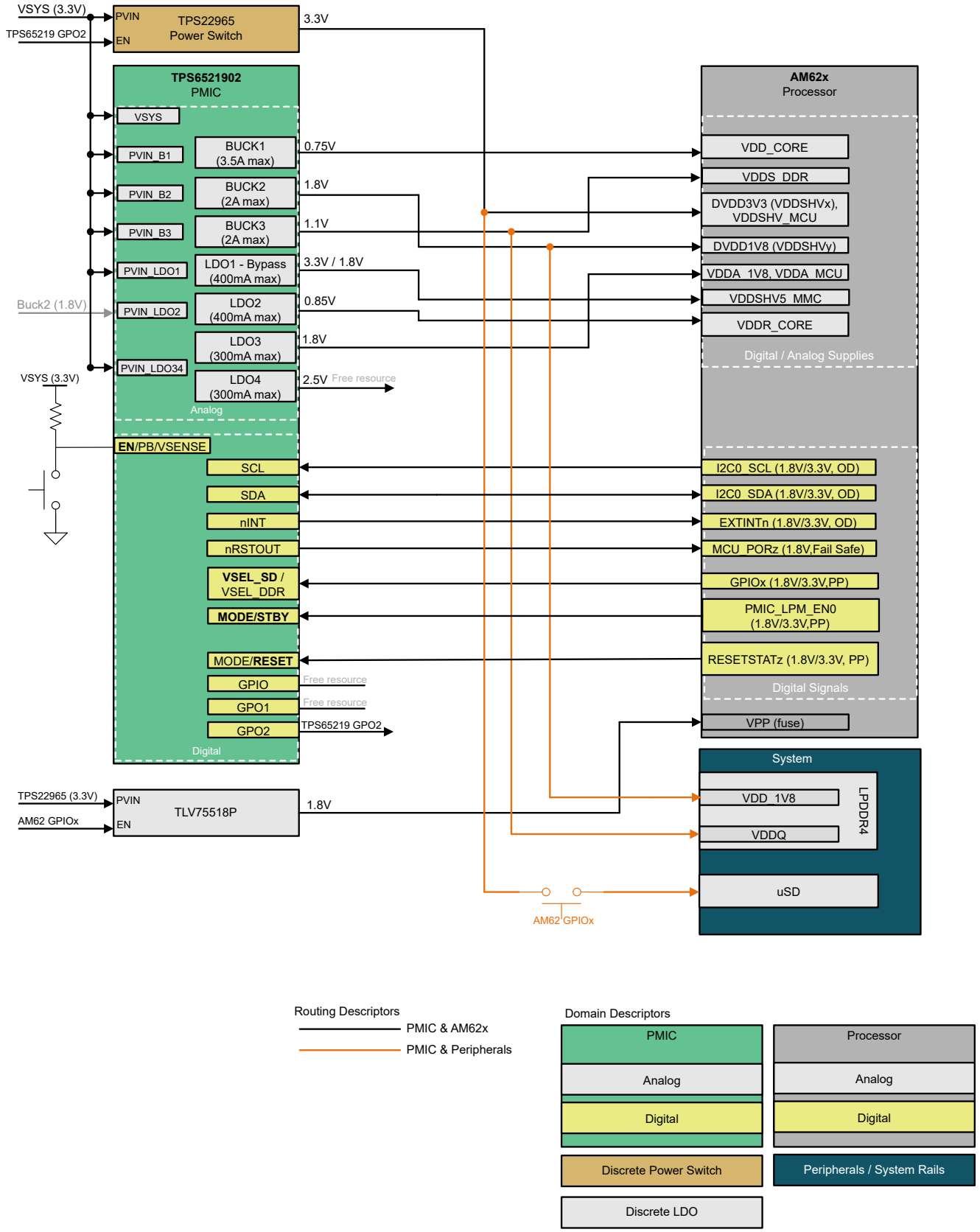


Figure 7-2. TPS6521902 Powering AM62

7.3 TPS6521903 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: DDR4 | VDD_CORE = 0.75 V

Figure 7-3 shows the TPS6521903 variant powering the AM62x processor on a system with 3.3 V input supply and DDR4 memory. This PMIC NVM configuration is similar to the TPS6521902 but has Buck3 configured to supply 1.2V (DDR4) instead of LPDDR4. The 3.3 V, coming from the pre-regulator, can be combined with a power switch to supply the 3.3 DVDDSH IO domain. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. GPO2 can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence. Buck3 is used to supply the VDDS_DDR and together with the 1.8 V on Buck2 they support the voltages needed for the DDR4 memory. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed.

The TPS6521903 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the TPS6521903 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

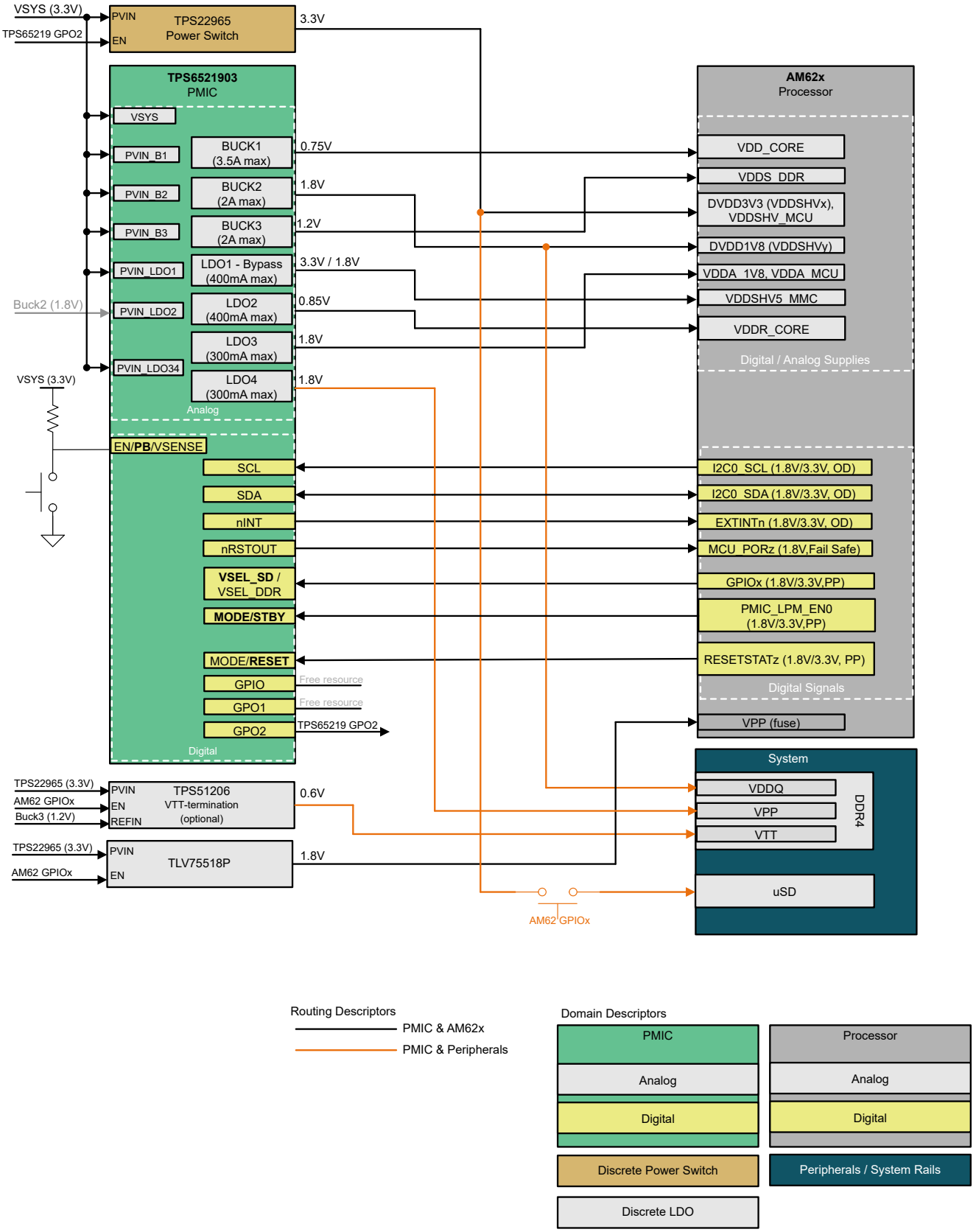


Figure 7-3. TPS6521903 Powering AM62x

7.4 TPS6521904 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: DDR4 | VDD_CORE = 0.85 V

Figure 7-4 shows the TPS6521904 variant powering the AM62x processor on a system with 3.3 V input supply and DDR4. This configuration is similar to the TPS6521903 but in this scenario, VDD_CORE is operated at 0.85 V instead of 0.75 V. As stated on the AM62x data sheet, "VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85 V". This requirement on the processor allows to have both, VDD_CORE and VDDR_CORE supplied by the same PMIC rail (Buck1). LDO2 is a free power resource configured as bypass (similar to load switch) and pre-programmed for 1.8V output which can be used to supply external peripherals. Similarly to the TPS6521903, this configuration also has GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. The configuration can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence).

The TPS6521904 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

This variant is used on the AM62B starter kit with PMIC and design files are available to be leveraged for new designs. Refer to the TPS6521904 Technical Reference Manual (Rev. A) for a description of the NVM settings and power-up/power-down sequence diagrams.

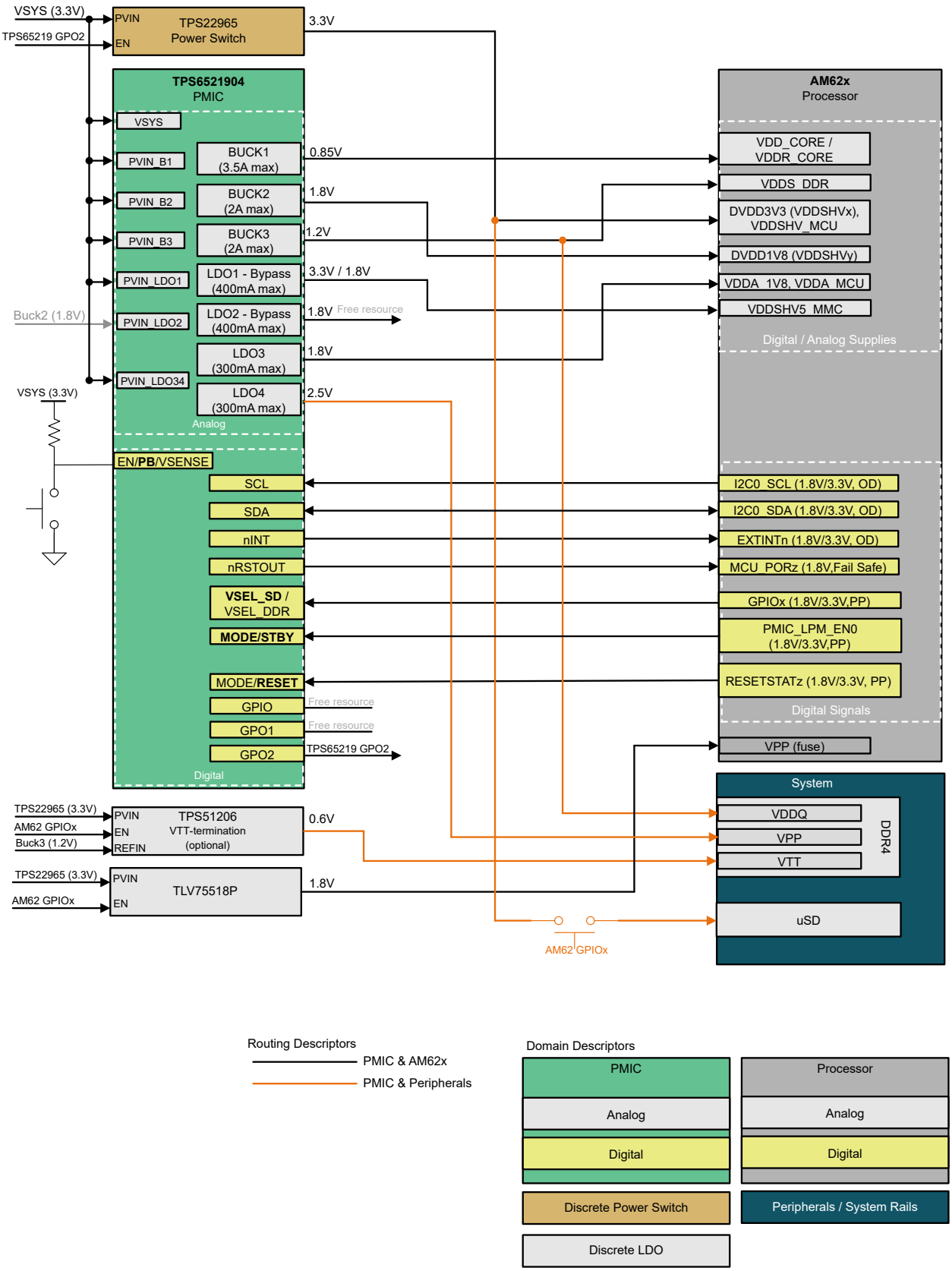


Figure 7-4. TPS6521904 Powering AM62x

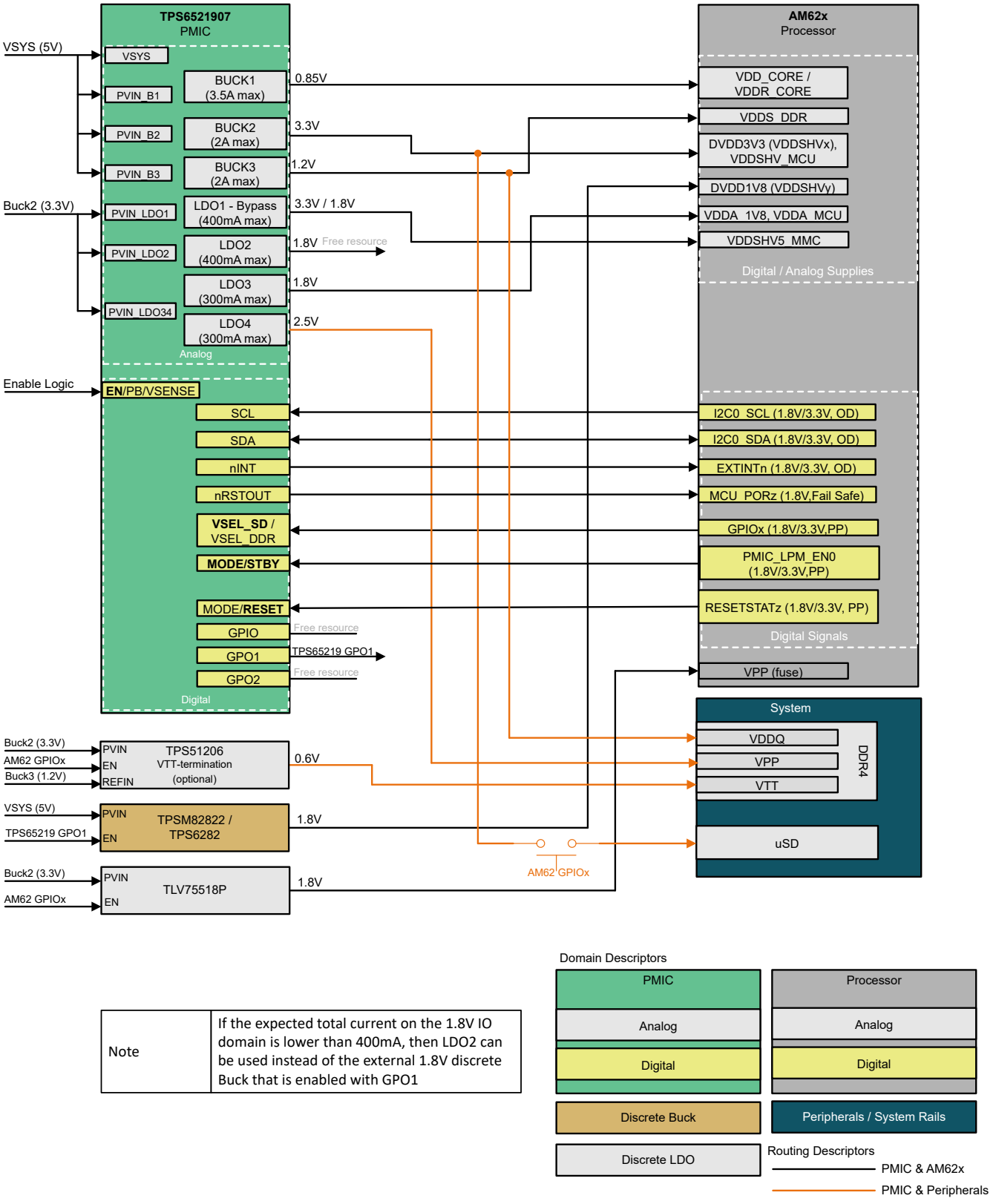
7.5 TPS6521907 Powering AM62x

VSYS = 5 V | Memory: DDR4 | VDD_CORE = 0.85 V

Figure 7-5 shows the TPS6521907 variant powering the AM62x processor on a system with 5 V input supply and DDR4 memory. This PMIC NVM is similar to the TPS6521901 but it supports VDD_CORE=0.85 V instead of 0.75 V. The 5 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx). Buck1 is used to supply the CORE rails at 0.85V. Buck2 and Buck3 supply the 3.3 V VDDSHVx IO and DDR IO respectively. Since Buck2 (3.3 V PMIC rail) is programmed to ramp up first in the power-up sequence, it can be used as the input supply for some of the LDOs to minimize power dissipation. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is a free resource that can be used to supply external peripherals. LDO3 supports the 1.8 V analog domain and LDO4 supports the 2.5 V VPP for the DDR4 memory. This power solution requires an external discrete buck regulator to supply the 1.8 V VDDSHV IO domain. This external discrete can be enabled using the GPO1 of the PMIC. TPS6521907 comes pre-programmed to enable GPO1 in the second slot of the power-up sequence. The external discrete should have active discharge and must ramp up and reach a stable output voltage before the PMIC starts powering up the rails in the next slot. The remaining two general purpose pins (GPIO and GPO2) are free digital resources that are disabled by default but can be enabled through I2C after the PMIC completes the power-up sequence.

Note

Refer to the TPS6521907 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.



Note	If the expected total current on the 1.8V IO domain is lower than 400mA, then LDO2 can be used instead of the external 1.8V discrete Buck that is enabled with GPO1

Figure 7-5. TPS6521907 Powering AM62

7.6 TPS6521908 Powering AM62x

VSYS = 3.3 V or 5 V | Memory: LPDDR4 | VDD_CORE = 0.85 V

Figure 7-6 shows the TPS6521908 variant powering the AM62x processor on a system with 3.3 V input supply and LDDR4. In this configuration, Buck1 is configured with an output voltage of 0.85V to supply the CORE rails. As noted in the AM62x spec, "VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85 V". This requirement on the processor allows to have both, VDD_CORE and VDDR_CORE supplied by the same PMIC rail (Buck1). Buck2 and Buck3 supply the 1.8V IO domain and the LPDDR voltage respectively. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO3 supplies the 1.8V analog domain. LDO2 and LDO4 are free power resource that can be used to supply external peripherals. This NVM variant also has GPO2 pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. It can be used to enable the external power switch and meet the processor sequence requirements. The power switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence).

The TPS6521908 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the TPS6521908 Technical Reference Manual for a description of the NVM settings and power-up/power-down sequence diagrams.

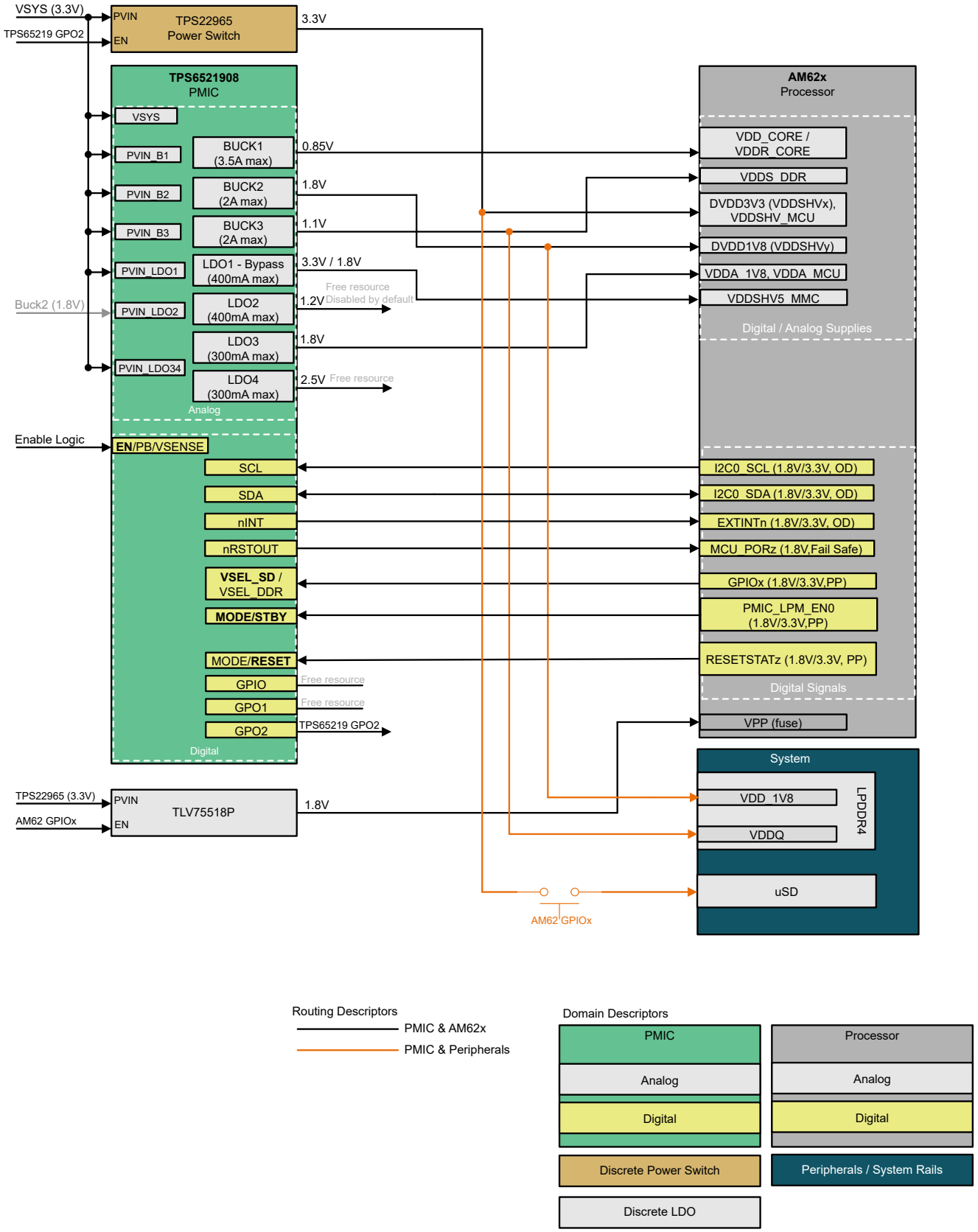


Figure 7-6. TPS6521908 Powering AM62

7.7 TPS6521920W-Q1 Powering AM62x-Q1

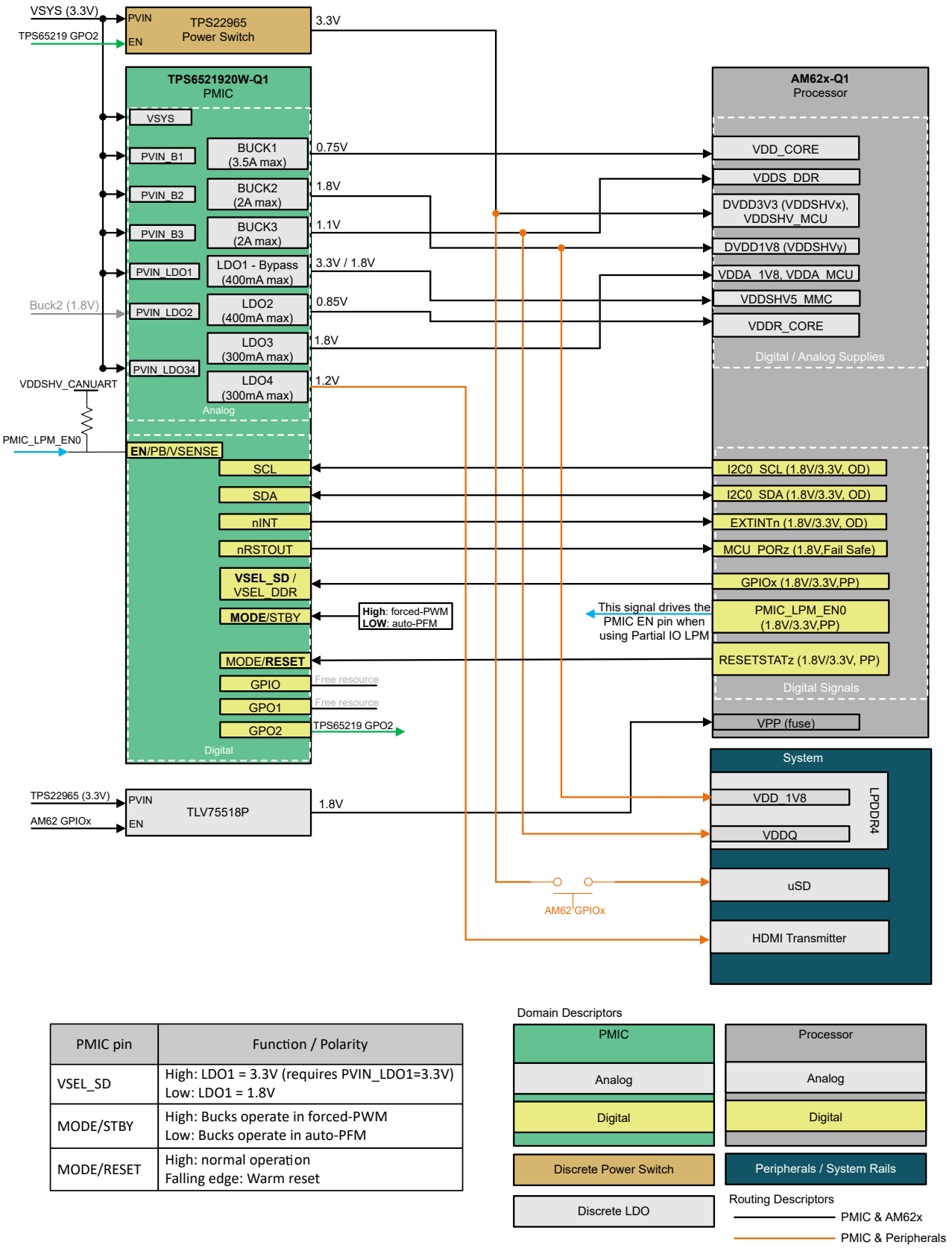
VSYS = 3.3 V or 5 V | Memory: LPDDR4 | VDD_CORE = 0.75 V | Automotive

Figure 7-7 shows the automotive TPS6521920W-Q1 variant powering the AM62x-Q1 processor on a system with 3.3 V input supply and LDDR4 memory. Buck1, Buck2 and Buck3 are used to supply VDD_CORE at 0.75 V, 1.8 V VDDSHVy IO and 1.1 V DDR IO respectively. The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 DVDDSHx IO domain. This external power switch will be enabled/disabled by the PMIC and must have an active discharge. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence). LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is used to supply the VDDR_CORE. LDO3 supports the 1.8 V analog domain. LDO4 is configured to output 1.2 V and can be used to supply the HDMI transmitter. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed.

The TPS6521920W-Q1 also supports 5V input supply. When using VSYS = 5 V, replace the external power-switch with a 3.3 V Buck converter. This external buck converter is enabled by the same PMIC GPO2.

Note

Refer to the *TPS6521920 Technical Reference Manual* for a description of the NVM settings and power-up or power-down sequence diagrams.



PMIC pin	Function / Polarity
VSEL_SD	High: LDO1 = 3.3V (requires PVIN_LDO1=3.3V) Low: LDO1 = 1.8V
MODE/STBY	High: Bucks operate in forced-PWM Low: Bucks operate in auto-PFM
MODE/RESET	High: normal operation Falling edge: Warm reset

Figure 7-7. TPS6521920W-Q1 Powering AM62x

8 References

1. Texas Instruments, *TPS65219 Integrated Power Management IC for ARM Cortex—A53 Processors and FPGAs* data sheet.
2. Texas Instruments, *TPS65219-Q1 Integrated Power Management IC for ARM Cortex—A53 Processors* data sheet.
3. Texas Instruments, *AM62x Sitara™ Processors* data sheet.

9 Revision History

Changes from Revision A (June 2022) to Revision B (September 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *TPS65219 vs TPS65219-Q1* table	2
• Added *TPS6521907 and TPS6521908* columns to table	5
• Added *TPS65219-Q1 NVMs for Automotive Applications* topic	6
• Added *TPS6521905 User-Programmable NVM* topic	8
• Added *AM62x Core Voltage Selection* topic	9
• Added *VSYS Voltage Ramp* topic	10
• Added *TPS6521920W-Q1 Powering AM62x-Q1* topic	25

Changes from Revision * (May 2022) to Revision A (June 2022)	Page
• Added link to TPS65219EVM design files	5
• Updated *AM62x SK E5 EM* with *SK-AM62-P1* and added hyperlink to the design files	5
• Deleted sample availability	5
• Added hyperlink to SK-AM62-P1	17

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265