Application Note

Analysis and Risk Assessment of Adaptive On-time Control Device in Bias Standby Operation

Shuai Fan, Edwin Zang, Junjie Mai

ABSTRACT

Synchronous buck converter with adaptive constant on-time (D-CAP™) control structure is widely used in various electronic systems, because of its fast transient performance, few external components for low cost and small solution size. In some special applications, it needs the D-CAP™ buck converter to operate in the standby state with pre-bias output and floated input. For previous literature about D-CAP™ structure, most of them focused on normal power transfer operation and loop performance. But the research and the assessment of the pre-bias standby operation has not been involved. Based on the basic logic of the D-CAP™ control, this application note will do a deep analysis and risk assessment about the pre-bias standby operation which has an important meaning in time saving and cost reduction.

Table of Contents

List of Figures

List of Tables

Trademarks

D-CAP™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

Copyright © 2022 Texas Instruments Incorporated

1 Introduction

Synchronous buck converter with adaptive constant on-time (D-CAP™) structure [1-2] is widely used as a second-stage source in electronic systems to supply various load, such as MCU, FPGA, and another signal device. In some applications, for the purpose of main source off-line operation, there will exist a backup source (such as battery or super capacitor) to support load after the main power supply being cut off. As shown in Figure 1-1, the Buck converter of main power source will encounter to operate with bias output and floating input. Actually, several of TI's adaptive on-time control converters already can support normal output pre-bias start up [4-5] with input side clamping to a voltage source. However, because of unclear conception about this special conditional with input floating, there is a common way which uses a controlled switch to avoid power flow back to input of Buck converter. But it will increase the cost and the size of the system. Based on the buck converters with the normal pre-bias start up function, this paper will make a deep analysis of the floating-input pre-bias output operation and assess the feasibility of removing the controlled switch for cost saving purpose.

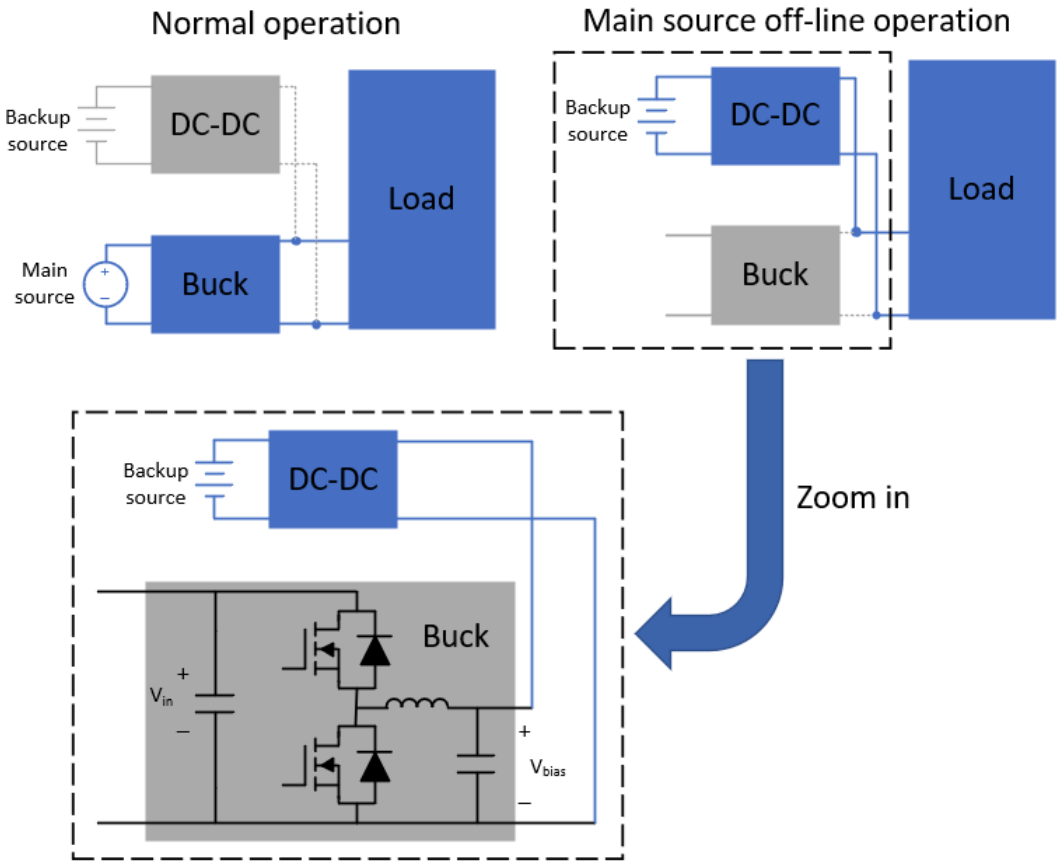

Figure 1-1. Floating Input and Bias Output Block Diagram

Copyright © 2022 Texas Instruments Incorporated

2 Analysis of the Floating-Input Pre-bias Output Operation

From the topology of Buck converter shown in Figure 1-1, it can be seen as that output is clamped by a bias voltage source V_{bias}. Because of the existing of body diode of MOSFET, the input voltage V_{in} will be clamped by V_{bias} through the body diode of the high side MOSFET, initially. Input voltage is shown in Equation 1. Actually, most of TI's IC has two basic functions : Enable function and UVLO (under voltage lock out). Device will shut down, if input voltage is lower than UVLO threshold or logic level at Enable pin is ineffective. If V_{bias} is a low voltage which can cause V_{in} to be lower than the UVLO threshold, it is obvious that the device will not start up.

$$V_{in}=V_{bias}-V_{diode} \quad (1)$$

If V_{in} is higher than UVLO threshold and Enable pin is logic effective, the device will start up and implement its logic. In this case, there's another way that use a controlled signal to let Enable pin be ineffective, which can avoid the converter to operate to make sure there is no continuous energy flow into input side . But it will need more external components to achieve that or occupy more digital I/O resource if MCU is used.

This application note's discussion focuses on the situation $V_{bias}-V_{diode}>V_{UVLO}$ and Enable pin directly being enabled from V_{in}. Generally, D-CAP™ structure device can be divided to two types. One type is the PSM (pulse-skip mode) device. PSM device has the logic ZC (zero-cross) detection and will reduce its frequency in light-load condition, which can implement a better light-load efficiency. ZC logic will monitor the inductor current during the low-side MOSFET turn on time, if the inductor current trend to be lower than zero, the low side MOSFET will turn off. It means that the inductor current will not be negative, if ZC logic is implemented. Another is the FCCM (force continuous conductive mode) device without the ZC, which implement a constant steady-state frequency under all load conditions. Because different types device can cause different behaviors, this application note will discuss the operation of PSM and FCCM mode device separately.

2.1 Analysis of FCCM Device

As mentioned above, FCCM device doesn't have the ZC logic. It means that the turn on time of high side MOSFET and the low side MOSFET is complemented, if deadtime is neglected. Figure 2-1 shows the basic logic block of adaptive constant on-time (D-CAP™) control [3], when analysis the FCCM device, the ZC part can be neglected.

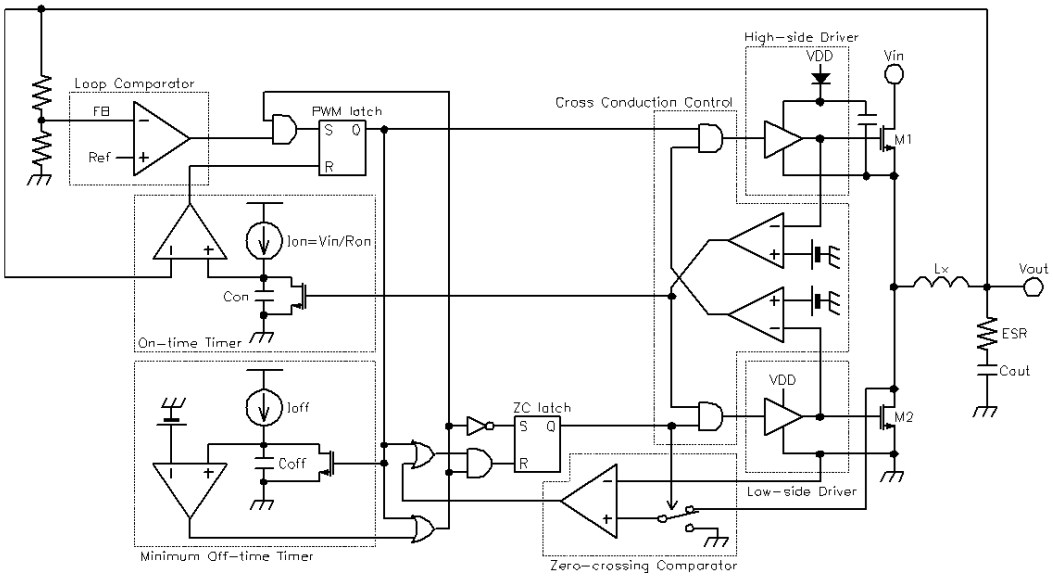

Figure 2-1. D-CAP™ Mode With Adaptive On-Time Modulator Block Diagram

From the operation logic of D-CAP structure, the device will compare the output feedback (FB) and reference voltage (Ref), the high side MOSFET will turn on when bias output voltage is lower than the target. If the bias output voltage is higher than target, high side will turn off and the lower side will turn on. The inductor current will ramp down, until it triggers negative operation current (NOC) protection. Because the logic priority of NOC is higher than the above compare logic, after triggering NOC, high side MOSFET will turn on, and the on time

Copyright © 2022 Texas Instruments Incorporated

is same as the normal operation which is relative to input voltage V_{in} and output voltage V_{out}, as shown in the Equation 2.

$$T_{on}=\frac{V_{bias}}{V_{in}*F_{sw}} \quad (2)$$

Where $F_{sw}=1/(R_{on}*C_{on})$, shown in Figure 2-1.

Because high side will turn on and transfer negative current to V_{in} side. It is difficult to judge the final state of V_{in} by a direct logic, so the hypothetical backstepping logic can be used. Suppose V_{in} can be a stable and constant voltage finally. Because there is no load in V_{in} side, so if V_{in} can be stable, the average inductor current must be zero. It means the absolute value of peak inductor current and valley inductor current is same, as shown in Figure 2-2.

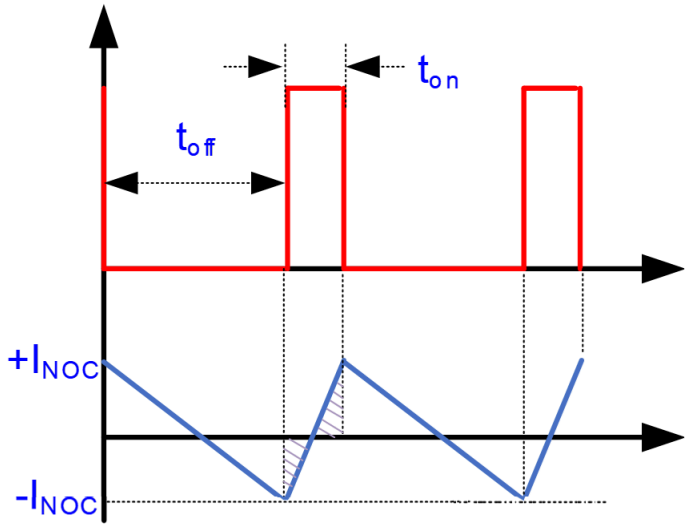

Figure 2-2. Supposed Stable Waveform of FCCM Mode, V_{out} > Target

From Figure 2-2, the turn-off time of high side switch is show in following.

$$T_{off}=\frac{2LI_{NOC}}{V_{bias}} \quad (3)$$

From the basic relationship between V_{in} and V_{out}, V_{in} is shown in following formula.

$$V_{in}=\frac{V_{bias}}{\left(1-\frac{t_{off}}{t_{off}+t_{on}}\right)} \quad (4)$$

Substitute Equation 2, Equation 3 into Equation 4, Vin can be written as Equation 5.

$$V_{in}=\frac{T_s{V_{bias}}^2}{(V_{bias}/F_{sw}-2LI_{NOC})} \quad (5)$$

From Equation 5, the stable value of V_{in} is related to I_{NOC} and inductor value *L*. If $V_{bias}/F_{sw}<=2LI_{NOC}$, it means V_{in} can be stable with a non-infinite constant value; if $V_{bias}/F_{sw}>2LI_{NOC}$, V_{in} can be a stable with a constant value, but it is determined by I_{NOC} and *L*. Generally, $V_{bias}/F_{sw}-2LI_{NOC}$ is a small value if the converter is reasonably designed, so V_{in} may be very large in this condition. So there exists the risk of over voltage damage.

If the output voltage is lower than the target, the minimum off time of high-side switch will always be triggered. So, on time is same as Equation 3, off time is shown in Equation 6. In steady sate, the voltage-second balance is established, as shown in Equation 7. By substitute Equation 2, Equation 6 into Equation 7, V_{in} can be written as

Copyright © 2022 Texas Instruments Incorporated

Equation 8. Generally, the minimum off time is much smaller than $1/F_{sw}$, so V_{in} will be closed to V_{bias}. It is not a high value that can casue damage.

$$T_{off}=T_{off\_min} \tag{6}$$

$$(V_{in}-V_{bias})*T_{on}/L=V_{bias}*T_{off}/L \tag{7}$$

$$V_{in}=\frac{V_{bias}}{(1-F_{sw}*T_{off\_min})} \tag{8}$$

Although the input voltage will not be a high value if V_{out} <V_{target}. But if consider the regulation and fluctuation, the operation of FCCM device has relative high risk of damage on the whole. Because the input voltage may ramp up to a very high value. For FCCM device, it suggests to use Enable function to shut down itself, and keep the bias standby operation safety. Most of TI's power DC/DC device support the enable function, can control the operate and shut down of converter flexibility.

2.2 Analysis of PSM Device

Same as the FCCM device, it also can be divided into two conditions: V_{bias} > V_{target} and V_{bias} < V_{target}.

Because ZC detection exists in PSM mode device. If the bias output voltage is higher than target, high side will be off state and the lower side will turn off if inductor current is closed to zero. So, V_{in} will be clamped by the V_{bias} through the high-side body diode, as shown in Equation 1.

If bias output voltage is lower than target, the minimum off time will be triggered. Because the logic priority of minimum off time is higher than ZC and there is no load in V_{in} side, after the inductor current reaching the zero level, the low side MOSFET will not turn off through ZC logic. Only after high side MOSFET waiting a minimum off time, low side MOSFET will turn off and high side MOSFET will turn on, which cause a negative current same as the FCCM device, as shown in Figure 2-3. If bias output voltage is lower than target, PSM device will operate as FCCM device with the minimum off time. V_{in} is same as that in Equation 4.

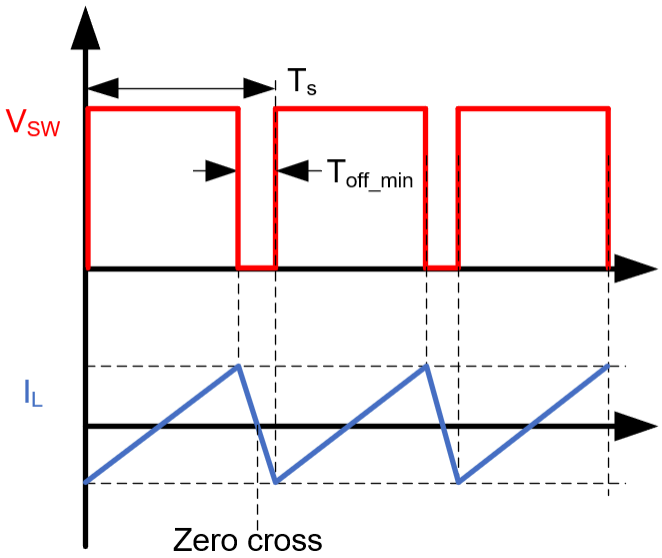

Figure 2-3. Stable Waveform of Eco Mode, V_{out} < Target

3 Experimental Verification

In this section, device TPS56524(2/7) [4] is used to verify the analysis and derivation results. TPS56524(2/7) is a high-performance synchronous buck converter with D-CAP3 control structure. It can support input voltage from 3 V to 16 V and 5 A output current with such a small package of SOT-563. TPS565242 is PSM device and TPS565247 is FCCM device. In the experiment, the set up is show in Figure 3-1, with floating input and bias output.

Copyright © 2022 Texas Instruments Incorporated

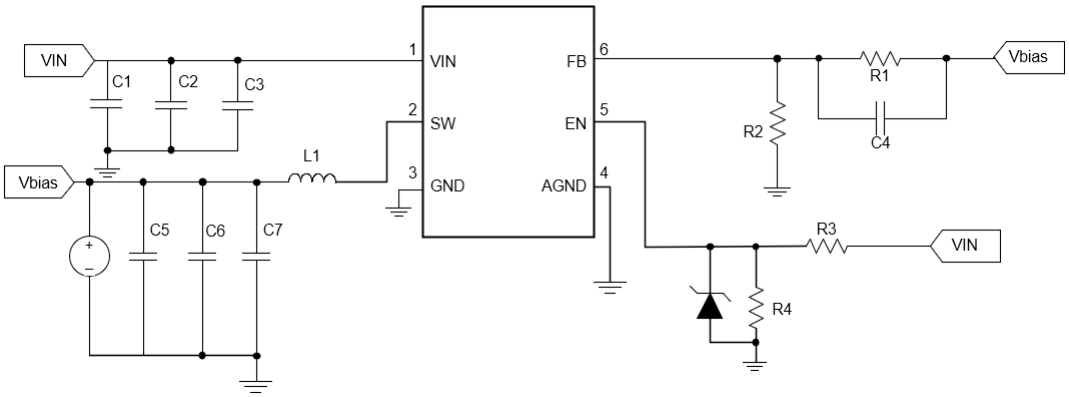

Figure 3-1. Experiment Schematic

3.1 FCCM device

3.1.1 Bias Voltage > Target

In the experiment, the target output voltage is 5 V, bias output is 5.05 V. From the test result in Table 3-1, the calculated input voltage based in Equation 5 is 20 V. The measured value is 18.4 V, it has exceeded the absolute max value in data sheet, it may cause permanent device damage.

Table 3-1. Test Result of Vbias>Vtarget in FCCM Device

Test device	V_{bias}	F_{sw}	L	I_{NOC}(measured)	V_{in} from Eq(5)	V_{in} measured
TPS565247	5.05 V	574KHz	1.1uH	3.08 A	20V	18.4 V

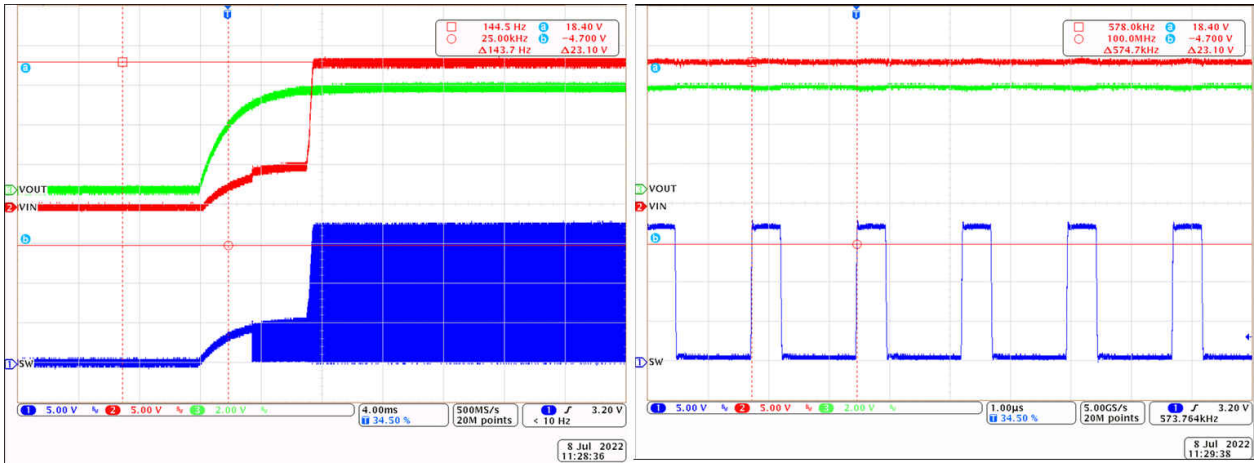

Figure 3-2. Test Waveform of V_{bias}>V_{target} in FCCM Device

3.1.2 Bias Voltage < Target

In the experiment, the target output voltage is 5 V, bias output is 4.95 V. It should be noticed that TPS565247 has the large duty operation function. From the data sheet, if Vin/Vbias< 1.6, and Vbias< target, the frequency will smoothly reduce with the ratio Vin/Vbias, the minimum switching frequency is limited about 200 KHz. Based on bias output voltage and Equation 8, even though with normal frequency (570 KHz), Vin will not exceed 1.6 Vbias. So the switching frequency will reduce to minimum 200 KHz, as shown in Figure 3-3. From the test result in Table 3-2, the calculated input voltage based in Equation 8 is 5.055 V, very closed to measured value.

Table 3-2. Test Result of V_{bias}<V_{target} in FCCM Device

Test device	V_{bias}	F_{sw}	T_{off_min}	V_{in} from eq(5)	V_{in} measured
TPS565247	4.95 V	200 KHz	104 ns	5.055 V	5.08 V

Copyright © 2022 Texas Instruments Incorporated

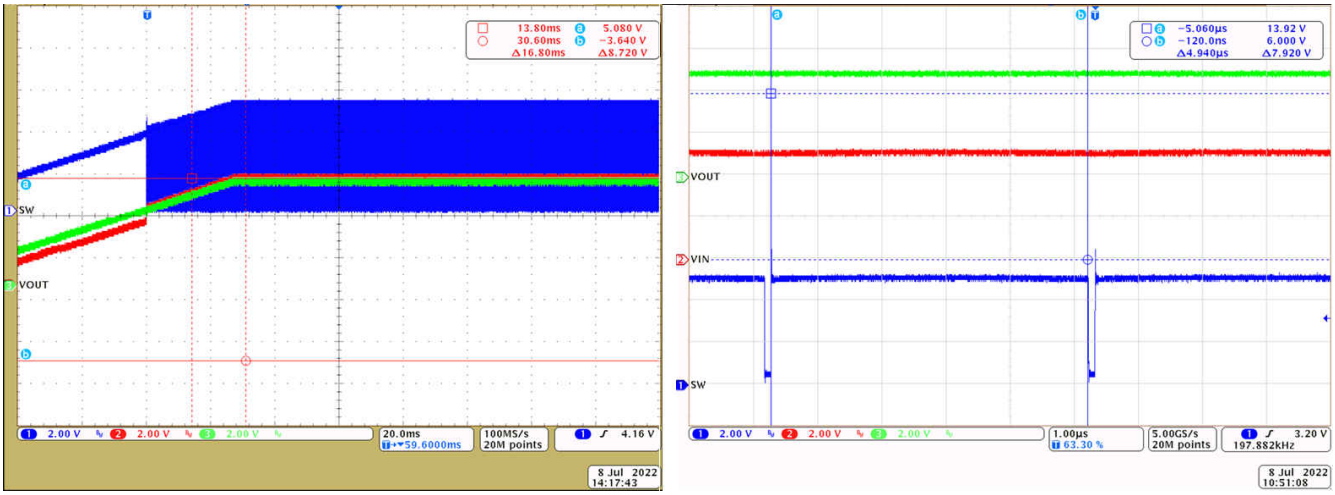

Figure 3-3. Test Waveform of V_{bias}<V_{target} in FCCM Device

3.2 PSM device

3.2.1 Bias Voltage > Target

In the experiment, the target output voltage is 5 V, bias output is 5.05 V. From the test result in Table 3-3, V_{in} is very close to the bias voltage, which confirm the derivation in Equation 1.

Table 3-3. Test Result of V_{bias}>V_{target} in PSM Device

Test device	V_{bias}	V_{in} measured
TPS565242	5.05 V	4.52 V

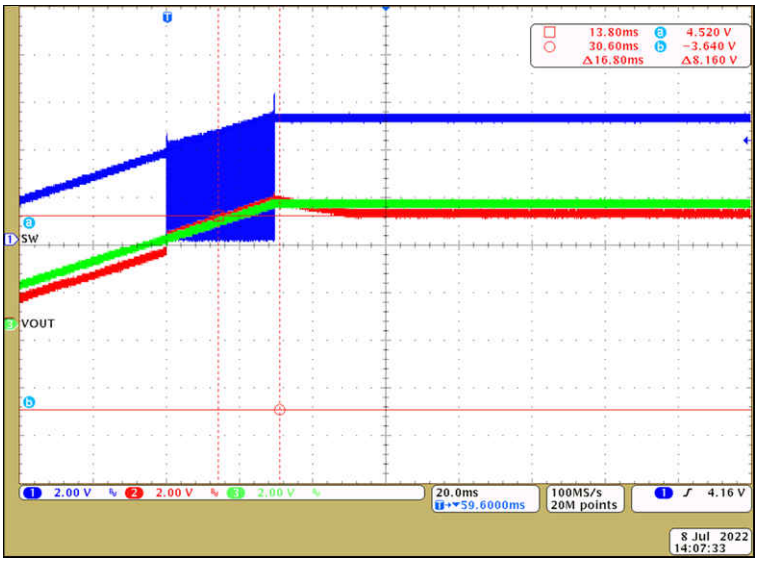

Figure 3-4. Test Waveform of V_{bias} > V_{target} in PSM Device

3.2.2 Bias Voltage < Target

In the experiment, the target output voltage is 5 V, bias output is 4.95 V. From the test result in Figure 3-5, the result is basically same as FCCM device in Equation 8.

Copyright © 2022 Texas Instruments Incorporated

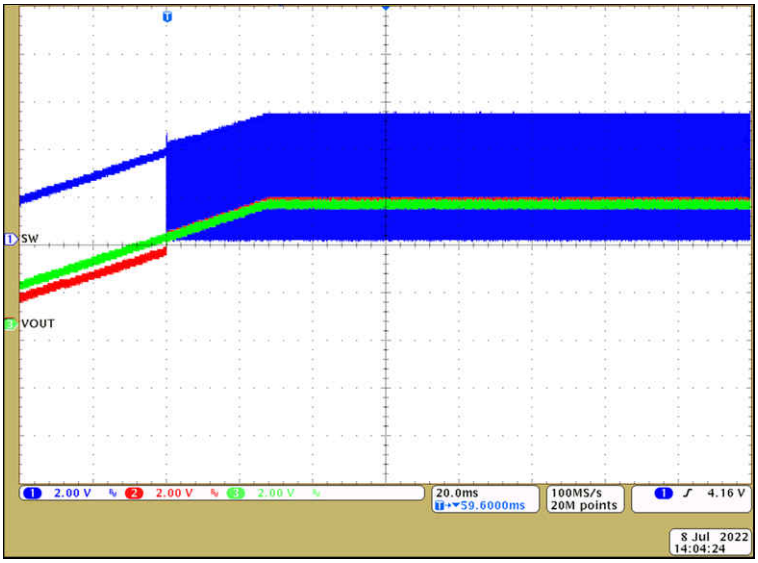

Figure 3-5. Test Waveform of V_{bias} < V_{target} in PSM Device

In summary, the input voltage of PSM mode device is very closed to the V_{bias} voltage, both in V_{bias}<V_{target} and V_{bias}>V_{target} condition and can operate safely.

4 Summary

For the floating input and bias output operation of the adaptive constant on-time (D-CAP) control device, the assessment of safe operation needs to discuss case by case. If the bias voltage is lower than UVLO threshold, device can operation safely both for FCCM and PSM device. If the bias voltage is higher than UVLO threshold, for FCCM device, it may encounter over voltage damage risk. Use enable function let device shut down is the most direct method to avoid energy flow into V_{in} side, but it is not the most simple method for PSM device. Based on the analysis in this application note, PSM device can operate safely if the bias voltage is higher than UVLO threshold. It means it is no need to use external control signal or switch, which can save the cost and system size.

5 References

1. Texas Instruments, *Stability Analysis and Design of D-CAP2 and D-CAP3 Converter – Part 1: How to Select Output*, application note.
2. Texas Instruments, *Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications*, application note.
3. Texas Instruments, *D-CAP™ Mode With All-Ceramic Output Capacitor Application* , application note.
4. Texas Instruments, *TPS56524x 3-V to 16-V Input Voltage, 5-A Synchronous Buck Converter in a SOT-563 Package*, data sheet.
5. Texas Instruments,*TPS56320x 4.5-V to 17-V Input, 3-A Synchronous Step-Down Voltage Regulator in SOT-23*, data sheet.

Copyright © 2022 Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated