Application Note

Powering the AM64x with the TPS65220 or TPS65219 PMIC

ABSTRACT

This application note can be used as a guide for integrating the TPS65220 or TPS65219 Power Management IC (PMIC) into non-automotive systems powering the Industrial AM64x Sitara Processor. An orderable part number comparison table details the configurations of several factory programmed TPS65220 and TPS65219 variants that can support different AM64x use cases. Example power maps are provided to assist the design process.

Table of Contents

1 Introduction ...............................................................................................................................2
2 TPS65220 and TPS65219 Overview .......................................................................................2 2.1 TPS65220 and TPS65219 Functional Block Diagram ..............................................................4
3 TPS65220 and TPS65219 Variants ............................................................................................6
4 TPS6522053 Powering AM64x ...............................................................................................7 4.1 TPS6521901 Powering AM64x ..........................................................................................10 4.2 TPS6521902 Powering AM64x ..........................................................................................12 4.3 TPS6521903 Powering AM64x ..........................................................................................14 4.4 TPS6521904 Powering AM64x ..........................................................................................16
5 References .................................................................................................................................18

List of Figures

Figure 2-1. TPS65220 Functional Block Diagram ......................................................................4 Figure 2-2. TPS65219 Functional Block Diagram ......................................................................5 Figure 4-1. TPS6522053 Powering AM64x ................................................................................7 Figure 4-2. TPS6522053 Power-Up Sequence ..........................................................................8 Figure 4-3. TPS6522053 Power-Down Sequence ......................................................................9 Figure 4-4. TPS6521901 Powering AM64x ..............................................................................10 Figure 4-5. TPS6521901 Power-Up Sequence .........................................................................11 Figure 4-6. TPS6521901 Power-Down Sequence ....................................................................11 Figure 4-7. TPS6521902 Powering AM64x ..............................................................................12 Figure 4-8. TPS6521902 Power-Up Sequence .........................................................................12 Figure 4-9. TPS6521902 Power-Down Sequence ....................................................................13 Figure 4-10. TPS6521903 Powering AM64x ..........................................................................14 Figure 4-11. TPS6521903 Power-Up Sequence .......................................................................15 Figure 4-12. TPS6521903 Power-Down Sequence ...................................................................15 Figure 4-13. TPS6521904 Powering AM64x ..........................................................................16 Figure 4-14. TPS6521904 Power-Up Sequence .......................................................................17 Figure 4-15. TPS6521904 Power-Down Sequence ...................................................................17

List of Tables

Table 2-1. TPS65220 and TPS65219 Power Resources .................................................................2 Table 2-2. TPS65220 and TPS65219 Features Comparison .........................................................3 Table 3-1. TPS65220 and TPS65219 Variant Comparison Table ....................................................6

Trademarks

Sitara™ is a trademark of Texas Instruments.
Arm® is a registered trademark of Arm Ltd.
All trademarks are the property of their respective owners.
1 Introduction

The TPS65220 PMIC is a cost and space optimized solution specially designed to power the AM64x processor and its principal peripherals. A hardware solution is readily available with the AM64x SK EVM Revision 2 using TPS65220 PMIC (SK-AM64B). In addition, functional spin TPS65219 PMIC has flexible mapping and comes in several factory programmed variants to support different AM64x use cases. The AM64x is within the Sitara™ family of Arm® processors, and provides highly flexible, real-time, and low latency processing for a broad range of industrial applications. To be used in applications from motor drives to Programmable Logic Controllers (PLCs), this processor provides powerful computing while supporting power management features designed for portable or power-sensitive systems. Powering a processor such as the AM64x family demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing.

The AM64x processor requires at minimum, power for seven main rails. These include the core supply rails (VDD_CORE and VDDR_CORE), DDR IO supply (VDDS_DDR), and 1.8 V and 3.3 V digital and analog IO rails (VDDSHVx, VDDSHV_MCU, VDDSHVy, VDDA_MCU). This application note discusses the TPS65220 and TPS65219 power management IC (PMIC) and their full feature-set, specially designed to power the AM64 Sitara™ processor and its principal peripherals.

2 TPS65220 and TPS65219 Overview

The TPS65220 and TPS65219 PMICs each contain seven regulators, 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) are configurable for load switch and bypass mode to support dynamic SD card voltages, while LDO3 and LDO4 (2×300 mA) are configurable as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65220 and TPS65219 PMIC each provides the full power package to supply the AM64x SoC, as well as many other SoCs. Table 2-1 provides a summary of the TPS65220 and TPS65219 Power Resources.

TPS65220 is characterized for -40°C to +125°C ambient temperature, and TPS65219 is characterized for -40°C to +105°C ambient temperature. The extended PMIC temperature range of TPS65220 allows support of AM64x based systems operating at higher temperatures. For safety sensitive applications, TPS65220 is functional safety capable. Therefore the TPS65220 development process is a TI-quality managed process, also functional safety FIT rate calculation and Failure mode distribution (FMD) is available for TPS65220. The TPS65220 device also provides flexibility in switching frequency, since it can support depending on programmed NVM settings either 2.3 MHz fixed frequency or 2.3MHz quasi-fixed frequency allowing low IQ/auto-PFM and Forced PWM modes. Table 2-2 provides a features comparison between the TPS65220 and TPS65219.

<table>
<thead>
<tr>
<th>Table 2-1. TPS65220 and TPS65219 Power Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td><strong>BUCK1</strong></td>
</tr>
<tr>
<td><strong>BUCK2</strong></td>
</tr>
<tr>
<td><strong>BUCK3</strong></td>
</tr>
<tr>
<td><strong>LDO1</strong></td>
</tr>
<tr>
<td><strong>LDO2</strong></td>
</tr>
<tr>
<td><strong>LDO3</strong></td>
</tr>
<tr>
<td><strong>LDO4</strong></td>
</tr>
</tbody>
</table>

- **BUCK1**: 2.3 MHz quasi-fixed frequency. TPS65220 can also support fixed frequency depending on configuration. Low IQ/auto-PFM and Forced PWM modes supported. Programmable power sequencing and default voltages. Integrated voltage supervisor for undervoltage. Supports dynamic voltage scaling (not needed when powering AM64x).
- **LDO1/LDO2**: Configurable as load switch and bypass-mode supporting SD-Card. Integrated voltage supervisor for undervoltage.
- **LDO3/LDO4**: Configurable as load switch. Integrated voltage supervisor for undervoltage.
<table>
<thead>
<tr>
<th>Feature</th>
<th>TPS65220</th>
<th>TPS65219</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency</td>
<td>Up to 2.3 MHz. Capable of either quasi-fixed frequency or fixed-frequency depending on device configuration (programmed NVM settings). Quasi-fixed frequency: • Auto-PFM • Forced-PWM Fixed-frequency: • Spread spectrum available</td>
<td>Up to 2.3 MHz Quasi-fixed frequency: • Auto-PFM • Forced-PWM</td>
</tr>
<tr>
<td>Operating Free-Air Temp $T_A$</td>
<td>-40°C to 125°C</td>
<td>-40°C to 105°C</td>
</tr>
<tr>
<td>Operating Junction Temp $T_J$</td>
<td>-40°C to 150°C</td>
<td>-40°C to 125°C</td>
</tr>
<tr>
<td>Functional Safety Capable</td>
<td>Functional Safety Capable (TI Quality managed process, Functional safety FIT rate calculation, and Failure Mode Distribution is available)</td>
<td>No</td>
</tr>
<tr>
<td>EVM availability</td>
<td>SK-AM64B EVM boards available on Ti.com starting September 2022.</td>
<td>TPS65219EVM (PMIC only. Does not include processor)</td>
</tr>
<tr>
<td>Package</td>
<td>One package option: • 5 mm × 5 mm, 0.5 mm pitch VQFN</td>
<td>Two package options: • 4 mm × 4 mm, 0.4 mm pitch VQFN • 5 mm × 5 mm, 0.5 mm pitch VQFN</td>
</tr>
</tbody>
</table>
2.1 TPS65220 and TPS65219 Functional Block Diagram

Figure 2-1. TPS65220 Functional Block Diagram
Figure 2-2. TPS65219 Functional Block Diagram
There are five different orderable part number (OPN) variants of the TPS65220 and TPS65219 PMIC that come factory programmed to power the AM64x processor. Selecting the right OPN will be based on the application use case and design requirements. Table 3-1 compares the NVM configurations from the output voltages on each rail to the configuration of the digital pins as well as the package options. This table also includes the reference hardware that is available to support new designs. For additional detailed information, please refer to the device data sheet and technical reference manual (TRM) available at TI.com.

### Table 3-1. TPS65220 and TPS65219 Variant Comparison Table

<table>
<thead>
<tr>
<th>Use Case</th>
<th>Vsys</th>
<th>Vsys</th>
<th>Vsys</th>
<th>Vsys</th>
<th>Vsys</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Memory</td>
<td>LPDDR4</td>
<td>DDR4</td>
<td>LPDDR4</td>
<td>DDR4</td>
<td>DDR4</td>
</tr>
<tr>
<td>BUCK1</td>
<td>Vout</td>
<td>0.75V</td>
<td>0.75V</td>
<td>0.75V</td>
<td>0.85V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
</tr>
<tr>
<td>BUCK2</td>
<td>Vout</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
</tr>
<tr>
<td>BUCK3</td>
<td>Vout</td>
<td>1.1 V</td>
<td>1.2 V</td>
<td>1.1 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
<td>High Bandwidth</td>
</tr>
<tr>
<td>LDO1</td>
<td>Vout</td>
<td>3.3 V (Bypass)</td>
<td>3.3 V (Bypass)</td>
<td>3.3 V</td>
<td>3.3 V (Bypass)</td>
</tr>
<tr>
<td>LDO2</td>
<td>Vout</td>
<td>0.85 V</td>
<td>0.85 V</td>
<td>0.85 V</td>
<td>1.8 V (Bypass)</td>
</tr>
<tr>
<td>LDO3</td>
<td>Vout</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>LDO4</td>
<td>Vout</td>
<td>2.5 V</td>
<td>2.5 V</td>
<td>2.5 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>GPIO</td>
<td>GPO1</td>
<td>Disabled</td>
<td>Enabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>GPIO</td>
<td>GPO2</td>
<td>Enabled</td>
<td>Disabled</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>GPIO</td>
<td>GPIO</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>Multi-Device</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>MODE_RESET</td>
<td>Config</td>
<td>Warm reset</td>
<td>Warm reset</td>
<td>Warm reset</td>
<td>Warm reset</td>
</tr>
<tr>
<td>MODE_STANDBY</td>
<td>Config</td>
<td>Mode and Standby</td>
<td>Mode and Standby</td>
<td>Mode and Standby</td>
<td>Mode and Standby</td>
</tr>
<tr>
<td>VSEL_SD_DDR</td>
<td>Config</td>
<td>SD</td>
<td>SD</td>
<td>SD</td>
<td>SD</td>
</tr>
<tr>
<td>Polarity</td>
<td>High = VOUT Low = 1.8 V</td>
<td>High = VOUT Low = 1.8 V</td>
<td>High = VOUT Low = 1.8 V</td>
<td>High = VOUT Low = 1.8 V</td>
<td></td>
</tr>
<tr>
<td>Rail</td>
<td>LDO1</td>
<td>LDO1</td>
<td>LDO1</td>
<td>LDO1</td>
<td></td>
</tr>
<tr>
<td>EN_PB_VSENSE</td>
<td>Config</td>
<td>Enable</td>
<td>Enable</td>
<td>Push-button</td>
<td>Push-button</td>
</tr>
<tr>
<td>Additional Features</td>
<td>Temperature Range</td>
<td>$T_A : -40^\circ C$ to $25^\circ C$</td>
<td>$T_A : -40^\circ C$ to $105^\circ C$</td>
<td>$T_A : -40^\circ C$ to $125^\circ C$</td>
<td>$T_A : -40^\circ C$ to $125^\circ C$</td>
</tr>
<tr>
<td>Functional Safety Capable</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>Orderable Part Number</td>
<td>Package size 5 x 5 mm</td>
<td>TPS6522053RHBR</td>
<td>TPS6521901RHBR</td>
<td>TPS6521902RHBR</td>
<td>TPS6521903RHBR</td>
</tr>
<tr>
<td>Design Resources</td>
<td>Reference Hardware</td>
<td>SK-AM64B EVM</td>
<td>TPS65219EVM (PMIC only. Does not include processor)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

[1] First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.
4  TPS6522053  Powering AM64x

Use case: VSYS=3.3V, LPDDR4 Memory, Extended Temperature Range, Functional Safety Capable

Figure 4-1 shows the TPS6522053 variant powering the AM64x processor on a system with 3.3 V input supply and LPDDR4 memory. The 3.3 V coming from the pre-regulator is connected to the main input supply for the reference system (VSYS) and to the power input of the buck converters (PVIN_Bx) and LDO1, LDO3, and LDO4 (PVIN_LDO1, PVIN_LDO34). The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 V VDDSHVx IO domain. Buck1 is used to supply VDD_CORE at 0.75 V. Buck3 and Buck2 support the 1.1 V and 1.8 V required by VDDS_DDR and the DVDD1V8 domain. They are also used to support the required voltages on the LPDDR4 memory. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 6ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage with the 6ms duration of the second slot (before the PMIC starts the next slot in the power-up sequence). LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is used to supply the VDDR_CORE. LDO3 supports the 1.8 V analog domain. LDO4 is a free 2.5 V power resource that can be used for external peripherals like the Ethernet PHY. GPIO and GPO1 are free digital resources that are disabled by default but could be enabled through I2C if needed. Figure 4-2 and Figure 4-3 shows the power-up and power-down sequence programmed on TPS6522053.

Figure 4-1. TPS6522053 Powering AM64x
Figure 4-2. TPS6522053 Power-Up Sequence

* ~0 at first power-up if FSD is enabled
Figure 4-3. TPS6522053 Power-Down Sequence
4.1 TPS6521901 Powering AM64x

Use case: VSYS=5V, DDR4 Memory

Figure 4-4 shows the TPS6521901 variant powering the AM64x processor on a system with 5 V input supply and DDR4 memory. The 5 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx). Buck1, Buck2 and Buck3 are used to supply VDD_CORE at 0.75 V, 3.3 V VDDSSHVx IO and DDR IO respectively. Since Buck2 (3.3 V PMIC rail) is programmed to ramp up first in the power-up sequence, it can be used as the input supply for some of the LDOs to minimize power dissipation. LDO1, configured as bypass, allows dynamic SD card voltage changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). LDO2, is used to supply the VDDA_CORE. LDO3 supports the 1.8 V analog domain and LDO4 supports the 2.5 V VPP for the DDR4 memory. This power solution requires an external discrete buck regulator to supply the 1.8 V VDDSSHV IO domain. This external discrete can be enabled using the GPO1 of the PMIC. TPS6521901 comes pre-programmed to enable GPO1 in the second slot of the power-up sequence with a duration of 10 ms. The external discrete must ramp up and reach a stable output voltage within the 10 ms duration of the second slot (before the PMIC starts the 3rd slot of the power-up sequence). The remaining two general purpose pins (GPIO and GPO2) are free digital resources that are disabled by default but can be enabled through I2C after the PMIC completes the power-up sequence. Figure 4-5 and Figure 4-6 shows the power-up and power-down sequence programmed on TPS6521901.
**Figure 4-5. TPS6521901 Power-Up Sequence**

- VSYS & PVIN_Bx (&PVIN_LDOx)
- ON-request
- IEEPROM-load, ~2.3ms
- DVDD3V3 (VDDSHVx)
- Buck2, 3.3V
- GPO1, external 1.8V rail
- Peripheral
- VDDA_1V8
- LDO1, 3.3V / 1.8V
- VDDS_DDR
- Buck3, 1.2V
- VDD_CORE
- Buck1, 0.75V
- VDDR_CORE
- LDO2, 0.85V
- MCU_OSC0_XI
- MCU_OSC0_XD
- MCU_PORz
- nRSTOUT
- ~0 at first power-up if FSD is enabled

**Figure 4-6. TPS6521901 Power-Down Sequence**

- OFF-request
- MCU_PORz
- nRSTOUT
- VDDS_DDR
- Buck3, 1.2V
- VDD_CORE
- Buck1, 0.75V
- VDDR_CORE
- LDO2, 0.85V
- MCU_OSC0_XI
- MCU_OSC0_XD
- VDDA_1V8
- Buck3, 1.2V
- Peripheral
- LDO1, 3.3V / 1.8V
- VDDCORE
- LDO3, 1.8V
- VDD2V_DDR
- Buck2, 3.3V
- VDD3V3 (VDDSHVx)
- Buck2, 3.3V
- 2.5V-IO / DDR
- LDO4, 2.5V

* ~0 at first power-up if FSD is enabled

* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt.

**Figure 4-6. TPS6521901 Power-Down Sequence**
4.2 TPS6521902 Powering AM64x

Use case: VSYS=3.3V, LDDR4 Memory

Figure 4-7 shows the TPS6521902 variant powering the AM64x processor on a system with 3.3 V input supply and LDDR4 memory. Buck1, LDO3, LDO2, and LDO1 are used to supply the same AM64x domains that were described in the previous block diagram. The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 V VDDSHVx IO domain. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC starts the next slot in the power-up sequence). Buck3 and Buck2 supports the 1.1 V and 1.8 V required by VDDS_DDR and the 1.8 V DVDD3V3 IO domain. They are also used to support the required voltages on the LPDDR4 memory. LDO4 is a free 2.5 V power resource that can be used for external peripherals like the Ethernet PHY. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed. Figure 4-8 and shows the power-up and power-down sequence programmed on TPS6521902.

Figure 4-7. TPS6521902 Powering AM64x
Figure 4-8. TPS6521902 Power-Up Sequence

* ~0 at first power-up if FSD is enabled

Figure 4-9. TPS6521902 Power-Down Sequence

* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt.
Slot-duration extends up to 8x its configured value.
4.3 TPS6521903 Powering AM64x

Use case: VSYS=3.3V, DDR4 Memory

Figure 4-10 shows the TPS6521903 variant powering the AM64x processor on a system with 3.3 V input supply and DDR4 memory. Buck1, Buck2, LDO3, LDO2, LDO1, and GPO2 are used to power/enable the same domains that were described in the previous power block diagrams. The 3.3 V, coming from the pre-regulator, can be combined with a power switch to supply the 3.3 V VDDSHVx IO domain. The GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence). Buck3 is used to supply the VDDS_DDR and together with the 1.8 V on Buck2 they support the voltages needed for the DDR4 memory. GPIO and GPO1 are free digital resources that are disable by default but could be enabled through I2C if needed. Figure 4-11 and Figure 4-12 shows the power-up and power-down sequence programmed on TPS6521903.
Figure 4-11. TPS6521903 Power-Up Sequence

Figure 4-12. TPS6521903 Power-Down Sequence

* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.
4.4 TPS6521904 Powering AM64x

Use case: VSYS=3.3V, DDR4 Memory, VDD_CORE=0.85V

Figure 4-13 shows the TPS6521904 variant powering the AM64x processor on a system with 3.3 V input supply and DDR4. This configuration is similar to the TPS6521903 but in this scenario, VDD_CORE is operated at 0.85 V instead of 0.75 V. As stated on the AM64x data sheet, "VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85 V". This requirement on the processor allows to have both, VDD_CORE and VDDR_CORE supplied by the same PMIC rail (Buck1). LDO2 is a free power resource pre-programmed for 1.8V output which can be used to supply external peripherals. Similarly to the TPS6521903, this configuration also has GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 10 ms. The configuration can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 10 ms duration of the second slot (before the PMIC start the next slot in the power-up sequence). Figure 4-14 and Figure 4-15 shows the power-up and power-down sequence programmed on TPS6521904.
Figure 4-14. TPS6521904 Power-Up Sequence

Figure 4-15. TPS6521904 Power-Down Sequence
5 References

1. Texas Instruments, **TPS65219 Integrated Power Management IC for ARM Cortex—A53 Processors and FPGAs** data sheet.
2. Texas Instruments, **AM64x Sitara™ Processors** data sheet.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated