Application Note

Solving Assembly Issues with Chip Scale Power MOSFETs

ABSTRACT

Texas Instruments has shipped billions of chip scale power MOSFETs that go into a variety of applications and end equipment types. Because of their small size, high performance and proven reliability, customers often favor these devices over conventional, plastic packaged parts. In general, the small percentage of assembly issues discussed below can be avoided by following the recommendations in the documentation referenced in this article.

Table of Contents

List of Figures

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1 Solving Assembly Issues with Chip Scale Power MOSFETs

Texas Instruments manufactures high performance power MOSFETs in chip scale silicon, land grid array (LGA) packages with metalized pads and wafer level chip scale packages (WLCSP) with die-sized ball grid array (DSBGA) interconnect allowing attachment to a printed circuit board (PCB) using standard surface mount technology (SMT) assembly processes. Occasionally, manufacturers have reported problems processing these devices and achieving acceptable results. The article discusses some of the common issues and their recommended solutions. Figure 1-1, Figure 1-2, and Figure 1-3 shows TI LGA and WLCSP MOSFETs.

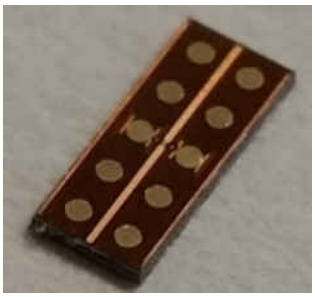

Figure 1-1. TI LGA MOSFETs

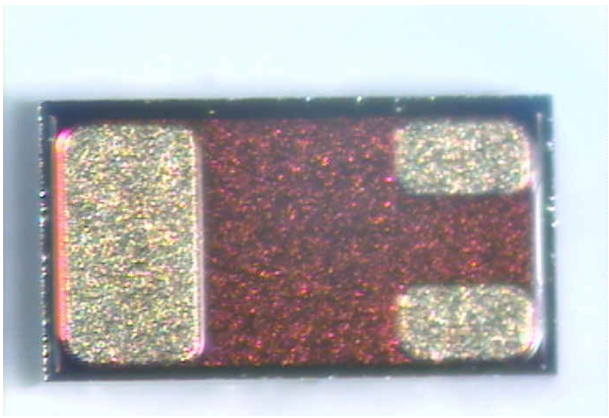

Figure 1-2. TI LGA MOSFETs

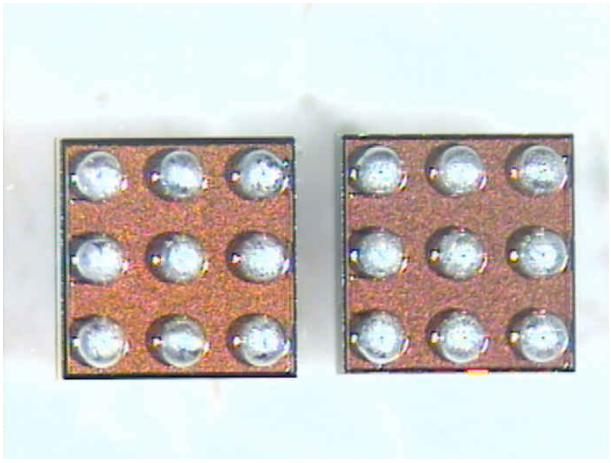

Figure 1-3. TI WLCSP MOSFETs

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2 Land Grid Area (LGA) MOSFET Packaging Technology

In 2013, TI introduced P and N-channel MOSFETs in the F4 FemtoFET™LGA package. Since then, two more packages, F3 and F5, and numerous devices have filled out the FemtoFET™ product portfolio. Additionally, LGA technology has been extended to include single and dual FETs for multiple applications where small size and high performance are advantageous. Figure 2-1 and Figure 2-2 shows illustrations of the F4 and F5 FemtoFET™ devices.

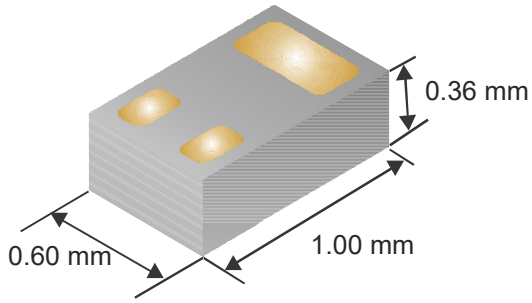

Figure 2-1. F4 FemtoFET™ Package

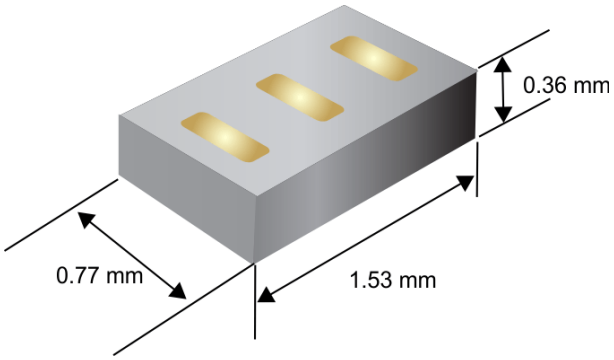

Figure 2-2. F5 FemtoFET™ Package

3 Wafer Level Chip Scale Packaging Technology

WLCSP is another family of chip scale MOSFETs similar to LGA devices using DSBGA interconnect instead of metalized pads on the chip as shown in Figure 1-3.

4 Common Issues

Common problems reported by customers include misalignment, tilting, poor/no solder joint, solder balls and chipping/cracking of the device. Figure 4-1, Figure 4-2, and Figure 4-3 show examples of common assembly issues.

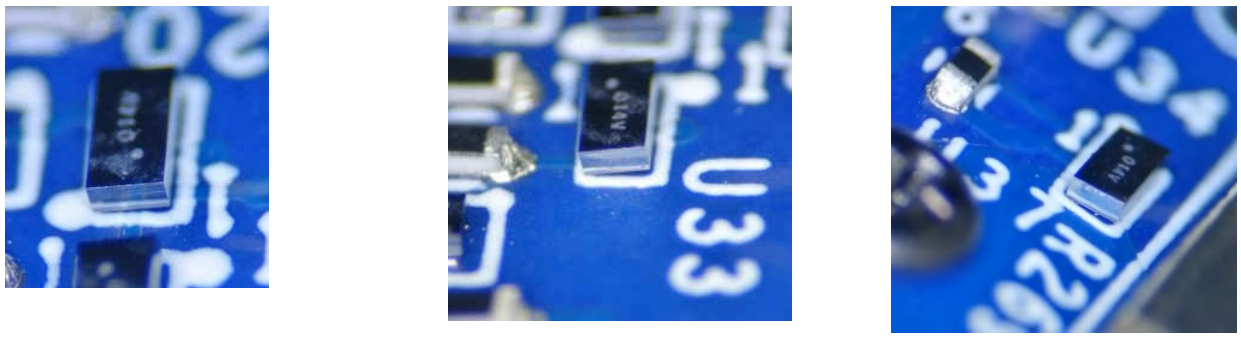

Figure 4-1. Examples of Tilted Packages Post Reflow

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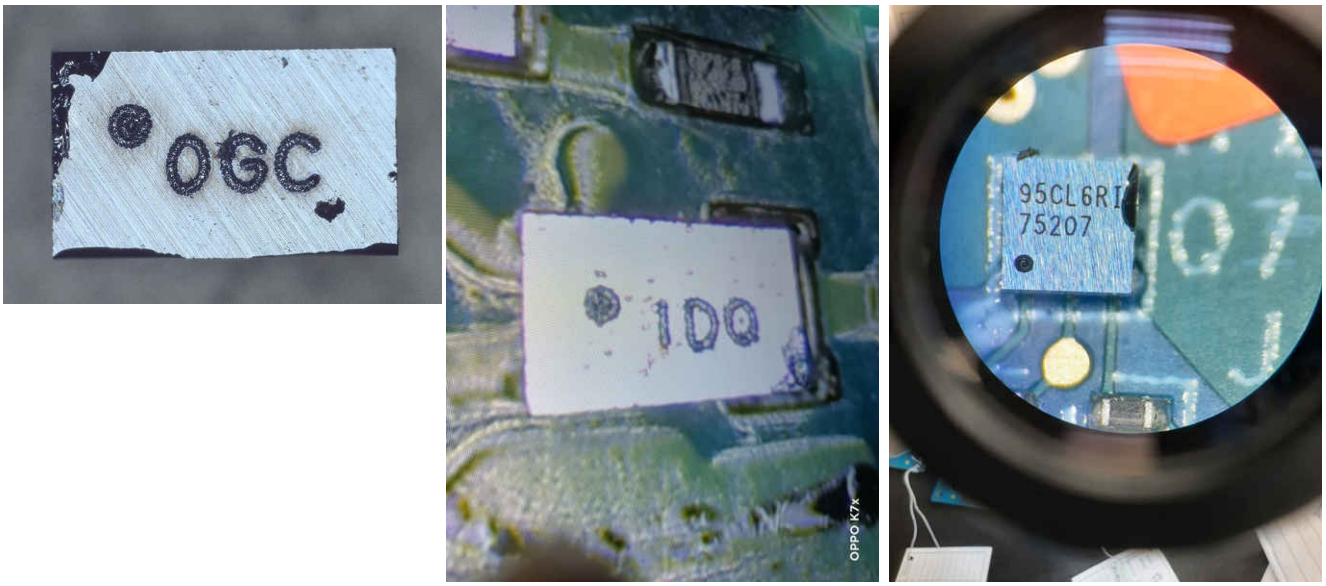

Figure 4-2. Examples of Chipped Packages

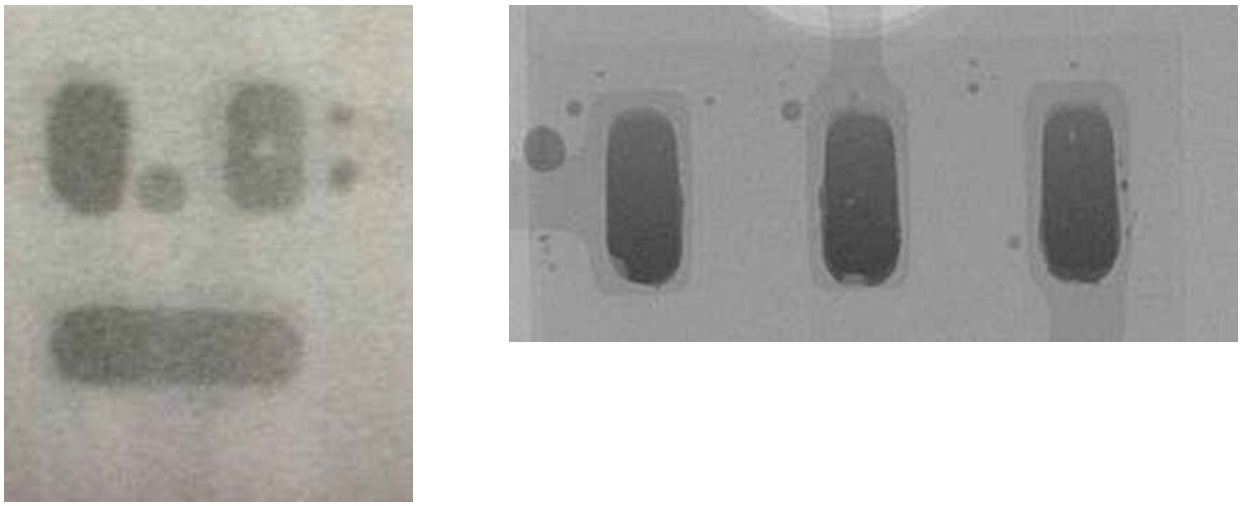

Figure 4-3. X-ray Images of Solder Balls

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5 Best Practices

Before starting a new design, the following documents provide detailed information, from PCB pad design to IR reflow profiles, required for PCB assembly of TI LGA and WLCSP FETs: *FemtoFET™ Surface Mount Guide* and *AN-1112 DSBGA Wafer Level Chip Scale Package*. Because of their construction, a silicon die (no plastic over molding, wire bonds or lead frame) with metalized or solder-bumped pads, care must be taken during the assembly process. When customers report an assembly problem, the first question to ask is *did they follow TI's recommended PCB layout and stencil patterns included in the MOSFET data sheets*? These have been optimized by TI through design of experiment (DOE) studies, used to qualify the packages, and are key to successful PCB assembly

6 Considerations When There are Problems

The following checklists detail where to look when there are problems with assembly. Most common issues with LGA and WLCSP packages are due to inaccurate component placement, incomplete contact with the PCB or mishandling of the device.

6.1 Tilted or Misaligned Packages

Tilting or misalignment of devices sometimes occurs during assembly. The following are some areas to look at when trying to resolve these issues.

1. Check the printed solder paste from top and side view or read from solder paste inspection (SPI) data to make sure the solder volumes are consistent.
2. Check the PCB land pattern design. Pads larger than recommended in the data sheet allow more space for the package to shift and rotate.
3. It is critical that the package is picked up at its center. The package might shift inside the tape and reel pocket during transportation and might not be picked up accurately. Package placement needs to be adjusted using the package outline to the center of the PCB pads.
4. Do not allow the package to free fall onto the PCB. Upon placement, the package needs to be level and in contact with the solder paste printed on the PCB pads. Placement force should not exceed 3N.
5. Sometimes tilting can be due to handling, movement of the conveyor belt, or airflow from the fan inside the reflow oven.
6. Visually inspect the package at a side view after placement and before reflow soldering. Inspect the package again post reflow. This can help isolate where the tilting occurs in the process.
7. Review X-rays to see if there are any abnormal voids in the solder joint that can cause package to tilt.

6.2 Solder Balls, Poor, or no Solder

Assembly issues such as solder balls, poor, or no solder joints can occur during reflow soldering.

1. Review the solder paste used. TI recommends using type 3 (25 to 45-micron particle size range) or finer, no-clean or water-soluble solder paste.
2. Flux content of solder paste can lead to solder balls. TI's qualification of these package used solder pastes with flux content between 10.5% and 10.8% with minimal solder balls. Other paste formulations can perform differently.
3. Allow solder paste to warm up to room temperature per supplier recommendations.
4. Do not exceed solder paste floor life per supplier guidelines.
5. Solder paste needs to be stirred thoroughly before printing. Component placement and reflow must follow paste printing as soon as possible to minimize flux evaporation and moisture absorption.
6. The PCB can absorb moisture causing solder balls. Pre-baking the PCB before assembly can drive the moisture out.
7. Avoid applying too much pressure during component placement. Depending on the pick and place machine, this can be controlled by adding 0.05mm to measured component thickness or by setting the minimum force. Placement force must not exceed 3N.
8. Follow the TI PCB layout and stencil pattern recommendations for best results. For LGA parts, solder mask defined (SMD) are recommended. For WLCSP FETs, non-solder mask defined (NSMD) are recommended.
9. Check the reflow profile. TI has several recommended IR reflow profiles depending on PCB thickness and component density. Contact your TI representative for more details.

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6.3 Chipped or Cracked Devices

Chipped or cracked packages are usually caused by handling before, during or after PCB assembly. This can lead to increased leakage current and long-term reliability issues. Chip scale MOSFETs are silicon die with solderable pads or balls and must be handled carefully during assembly to avoid cracking or chipping. Here are some useful tips

1. Most handling is performed by machine processes during PCB assembly. Minimize manual handling.
2. When manual handling is required, never use metal tweezers to pick up a device. Refer to the *WCSP Handling Guide* for handling guidance of these devices.
3. Check the pick and place nozzle size. TI recommends using a nozzle with no larger than 75% of the shorter side of the package.
4. Choose nozzle with soft tip instead of metal.
5. Placement force should not exceed 3N.
6. Do not poke or probe the body of the device with a metallic oscilloscope or digital multimeter probe.

7 Summary

High performance power MOSFETs in innovative chip scale silicon packages from Texas Instruments fit into many applications where space is at a premium. These LGA and WLCSP devices have gained traction in the market and are being used in multiple end equipment types. This article discussed common issues customers have reported during PCB assembly of these components and provides guidance to identify and correct these problems. For best results, engineers and PCB designers should closely follow the recommended PCB land and stencil recommendations in the MOSFET data sheet and design documents referenced in this article.

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8 References

Check out these documents to learn more about these devices and additional details on PCB assembly:

- Texas Instruments, *FemtoFET™ Surface Mount Guide*
- Texas Instruments, *E2E™ Forum: FemtoFET MOSFETs: small as sand but it's all about that pitch*
- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package*, application note.
- Texas Instruments, *WCSP Handling Guide*

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