ABSTRACT

This application note can be used as a guide for integrating the TPS65219 Power Management IC (PMIC) into systems powering the AM243x Sitara™ Microcontroller. An orderable part number comparison table details the configurations of several factory programmed TPS65219 variants that can support different AM243x use cases. Example power maps are provided to assist the design process.

Table of Contents

1 Introduction............................................................................................................................................................................2
2 TPS65219 Overview................................................................................................................................................................2
  2.1 TPS65219 Functional Block Diagram................................................................................................................................3
3 TPS65219 Variants..................................................................................................................................................................4
4 TPS6521904 Powering AM243x............................................................................................................................................5
  4.1 TPS6521907 Powering AM243x........................................................................................................................................9
  4.2 TPS6521908 Powering AM243x......................................................................................................................................13
5 References........................................................................................................................................................................17

List of Figures

Figure 2-1. TPS65219 Functional Block Diagram................................................................................................................................................3
Figure 4-1. TPS6521904 Powering AM243x........................................................................................................................................6
Figure 4-2. TPS6521904 Power-Up Sequence........................................................................................................................................7
Figure 4-3. TPS6521904 Power-Down Sequence........................................................................................................................................8
Figure 4-4. TPS6521907 Powering AM243x........................................................................................................................................10
Figure 4-5. TPS6521907 Power-Up Sequence........................................................................................................................................11
Figure 4-6. TPS6521907 Power-Down Sequence........................................................................................................................................12
Figure 4-7. TPS6521908 Powering AM243x........................................................................................................................................14
Figure 4-8. TPS6521908 Power-Up Sequence........................................................................................................................................15
Figure 4-9. TPS6521908 Power-Down Sequence........................................................................................................................................16

List of Tables

Table 2-1. TPS65219 Power Resources..................................................................................................................................................2
Table 3-1. TPS65219 Variant Comparison Table........................................................................................................................................4

Trademarks

Sitara™ is a trademark of Texas Instruments.
Arm® is a registered trademark of Arm Ltd.
All trademarks are the property of their respective owners.
1 Introduction

The TPS65219 PMIC is a cost and space optimized solution designed to power the AM243x microcontroller and its principal peripherals. The TPS65219 PMIC has flexible mapping and comes in several factory programmed variants to support different AM243x use cases. The AM243x is within the Sitara™ family of Arm® processors, and provides highly flexible, real-time, and low latency processing for a broad range of industrial, enterprise and communications applications. These processors come in an array of variants with up to four Arm® Cortex® -R5F cores each. Powering a microcontroller such as the AM243x family demands requirements such as sufficient current headroom, tight transient requirements, and a number of rails that can be fully controlled for power up and power down sequencing.

2 TPS65219 Overview

The TPS65219 PMIC contains seven regulators, 3 Buck regulators and 4 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 3.5 A for Buck1, and 2 A each for the remaining buck regulators. LDO1 and LDO2 (2×400 mA) are configurable for load switch and bypass mode to support dynamic SD card voltages, while LDO3 and LDO4 (2×300 mA) are configurable as load switches. With a VIN range of 2.5 V to 5.5 V, the PMIC can support a common 3.3 V or 5 V system voltage. TPS65219 is characterized for -40°C to +105°C ambient temperature. With an I2C interface, three GPIO pins, and three multi-function-pins, the TPS65219 PMIC provides the full power package to supply the AM243x, as well as many other SoCs and FPGAs.

<table>
<thead>
<tr>
<th>Table 2-1. TPS65219 Power Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Voltage</strong></td>
</tr>
<tr>
<td>BUCK1</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>BUCK2</td>
</tr>
<tr>
<td>BUCK3</td>
</tr>
<tr>
<td>LDO1</td>
</tr>
<tr>
<td>LDO2</td>
</tr>
<tr>
<td>LDO3</td>
</tr>
<tr>
<td>LDO4</td>
</tr>
</tbody>
</table>
2.1 TPS65219 Functional Block Diagram

Figure 2-1. TPS65219 Functional Block Diagram
3 TPS65219 Variants

There are three different orderable part number (OPN) variants of the TPS65219 PMIC that come factory programmed to power the AM243x. Selecting the right OPN will be based on the application use case and design requirements. Table 3-1 compares the NVM configurations from the output voltages on each rail to the configuration of the digital pins as well as the package options. For additional detailed information, please refer to the device data sheet and technical reference manual (TRM) available at TI.com.

Note, the AM243x comes in both the ALX Package and the ALV package. The AM243x (ALX Package) body size is 11 mm × 11 mm, and does not support LPDDR4 or DDR4 memory. The AM243x (ALV Package) body size is 17.2 mm × 17.2 mm, which has a benefit of pin-to-pin compatibility with the AM64x. The three TPS65219 orderables detailed in this application note are optimized for the AM243x (ALV Package).

If using the AM243x (ALX Package), LP87334DRHDR PMIC is recommended as the optimized power solution for the AM243x core rails. Please refer to Section 5.3 of Using LP8733xx and TPS65218xx PMICs to Power AM64xand AM243x Sitara Processors, application note for more details on this power solution. If the AM243x (ALX Package) is being used in a system with several peripherals, we recommend user-programming TPS65219 to power both the AM243x core rails and additional peripherals.

Table 3-1. TPS65219 Variant Comparison Table

<table>
<thead>
<tr>
<th>Use Case</th>
<th>TPS6521904</th>
<th>TPS6521907</th>
<th>TPS6521908</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vsys</td>
<td>3.3 V</td>
<td>5 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>External Memory Support</td>
<td>DDR4</td>
<td>DDR4</td>
<td>LPDDR4</td>
</tr>
<tr>
<td>BUCK1 Vout</td>
<td>0.85 V</td>
<td>0.85 V</td>
<td>0.85 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
</tr>
<tr>
<td>BUCK1 Vout</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
</tr>
<tr>
<td>BUCK2 Vout</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>1.1 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
<td>High bandwidth</td>
</tr>
<tr>
<td>LDO1 Vout</td>
<td>1.8 V (Bypass)</td>
<td>3.3 V (Bypass)</td>
<td>3.3 V (Bypass)</td>
</tr>
<tr>
<td>LDO2 Vout</td>
<td>1.8 V (Bypass)</td>
<td>1.8 V</td>
<td>1.2 V (Disabled by default)</td>
</tr>
<tr>
<td>LDO3 Vout</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>LDO4 Vout</td>
<td>2.5 V</td>
<td>2.5 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>GPIO GPO1</td>
<td>Disabled</td>
<td>Enabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>GPIO GPO2</td>
<td>Enabled</td>
<td>Disabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>GPIO GPO3</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>Multi-Device</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>MODE_RESET Config</td>
<td>Warm reset</td>
<td>Warm reset</td>
<td>Warm reset</td>
</tr>
<tr>
<td>MODE_STANDBY Config</td>
<td>Mode and Standby</td>
<td>Mode and Standby</td>
<td>Mode and Standby</td>
</tr>
<tr>
<td>VSEL_SD_DDR Config</td>
<td>SD</td>
<td>SD</td>
<td>SD</td>
</tr>
<tr>
<td>Polarity</td>
<td>High = VOUT</td>
<td>High = VOUT</td>
<td>High = VOUT</td>
</tr>
<tr>
<td>Low = 1.8 V</td>
<td>Low = 1.8 V</td>
<td>Low = 1.8 V</td>
<td>Low = 1.8 V</td>
</tr>
<tr>
<td>Rail</td>
<td>LDO1</td>
<td>LDO1</td>
<td>LDO1</td>
</tr>
<tr>
<td>EN_PB_VSENSE Config</td>
<td>Push-button</td>
<td>Enable</td>
<td>Enable</td>
</tr>
<tr>
<td>First Supply detection [1]</td>
<td>Enabled</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>Orderable Part Number Package size 5 x 5 mm</td>
<td>TPS6521904RHBR</td>
<td>TPS6521907RHBR</td>
<td>TPS6521908RHBR</td>
</tr>
<tr>
<td>Orderable Part Number Package size 4 x 4 mm</td>
<td>TPS6521904RSMR</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Technical Reference Manual</td>
<td>TPS6521904 TRM</td>
<td>TPS6521907 TRM</td>
<td></td>
</tr>
</tbody>
</table>

[1] First Supply detection allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE. At first power-up the EN/PB/VSENSE pin is treated as if it had a valid ON request.
4 TPS6521904 Powering AM243x

Use case: VSYS=3.3V, DDR4 Memory

Figure 4-1 shows the TPS6521904 variant powering the AM243x on a system with 3.3 V input supply and DDR4 memory.

The 3.3 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx) and LDO1, LDO3, and LDO4 (PVIN_LDO1, PVIN_LDO34). The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 V VDDSHVx IO domain. Buck1, Buck2, and LDO3 power the remaining core rails of the AM243x processor. Buck3 and LDO4 support the required voltages to power the DDR4 memory.

LDO1 and LDO2 are free power resources that can be used for external peripherals, such as 3.3-V rail required for I/Os and an additional 2.5-V rail for the Ethernet PHYs. LDO1, configured as bypass, allows dynamic changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). GPIO and GPO1 are free digital resources that are disabled by default but could be enabled through I2C if needed. GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 6ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 6ms duration of the second slot (before the PMIC starts the next slot in the power-up sequence). TPS6521904 comes pre-programmed, but maintains user-programmable functionality as a NVM device that allows full customization of the output voltages, sequencing, GPIO control, and more to best meet system needs.

Figure 4-2 and Figure 4-3 shows the power-up and power-down sequence programmed on TPS6521904.
Figure 4-1. TPS6521904POWERING AM243x
Figure 4-2. TPS6521904 Power-Up Sequence
PMIC Rail Sequence AM243x Domain

OFF-Request

nRSTOUT 10ms

Buck3 / 1.2V

LDO2 / 1.8V

10ms

BUCK1 / 0.85V

BUCK2 / 1.8V

LDO3 / 1.8V

LDO1 / 3.3V-1.8V

LDO4 / 2.5V

VDDS_DDR MCU_PORz

VDD_CORE VDDR_CORE

DVDD1V8

VDDA_1V8

DVDD3V3

DDR4 VPP

MCU_OSC0_XI MCU_OSC0_XO

MCU_OSC0_XI

VDDO_CORE VDDR_CORE

10ms

GPO2

10ms

VSYS

Slot_0 10ms Slot_1 0ms Slot_2 10ms

Figure 4-3. TPS6521904 Power-Down Sequence
4.1 TPS6521907 Powering AM243x

Use case: VSYS=5V, DDR4 Memory

Figure 4-4 shows the TPS6521907 variant powering the AM243x microcontroller on a system with 5 V input supply and DDR4 memory. The 5 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx). Buck1, Buck2 and Buck3 are used to supply VDD_CORE at 0.85 V, 3.3 V VDDSHVx IO and DDR IO respectively. Since Buck2 (3.3 V PMIC rail) is programmed to ramp up first in the power-up sequence, it can be used as the input supply for some of the LDOs to minimize power dissipation. LDO3 supports the 1.8 V analog domain and LDO4 supports the 2.5 V VPP for the DDR4 memory. This power solution requires an external discrete buck regulator to supply the 1.8 V VDDSHV IO domain. This external discrete can be enabled using the GPO1 of the PMIC. TPS6521901 comes pre-programmed to enable GPO1 in the second slot of the power-up sequence with a duration of 10 ms. The external discrete must ramp up and reach a stable output voltage within the 10 ms duration of the second slot (before the PMIC starts the 3rd slot of the power-up sequence).

LDO1 and LDO2 are free power resources that can be used for external peripherals, such as 3.3-V rail required for I/Os. LDO1, configured as bypass, allows dynamic changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). The remaining two general purpose pins (GPIO and GPO2) are free digital resources that are disabled by default but can be enabled through I2C after the PMIC completes the power-up sequence. TPS6521907 comes pre-programmed, but maintains user-programmable functionality as a NVM device that allows full customization of the output voltages, sequencing, GPIO control, and more to best meet system needs. Figure 4-5 and Figure 4-6 shows the power-up and power-down sequence programmed on TPS6521907.
If the expected total current on the 1.8V IO domain is lower than 400mA, then LDO2 can be used instead of the external 1.8V discrete Buck that is enabled with GPO1.

Figure 4-4. TPS6521907 Powering AM243x
Figure 4-5. TPS6521907 Power-Up Sequence
Figure 4-6. TPS6521907 Power-Down Sequence
4.2 TPS6521908 Powering AM243x

Use case: VSYS=3.3V, LDDR4 Memory

Figure 4-7 shows the TPS6521908 variant powering the AM243x microcontroller on a system with 3.3 V input supply and LDDR4 memory.

The 3.3 V coming from the pre-regulator is connected to the main input supply for reference system (VSYS) and to the power input of the buck converters (PVIN_Bx) and LDO1, LDO3, and LDO4 (PVIN_LDO1, PVIN_LDO34). The 3.3 V coming from the pre-regulator can be combined with a power switch to supply the 3.3 V VDDSHVx IO domain. Buck1, Buck2, and LDO3 power the remaining core rails of the AM243x processor. Buck2 and Buck3 support the required voltages to power the DDR4 memory.

LDO1, LDO2, and LDO4 are free power resources that can be used for external peripherals, such as 3.3-V rail required for I/Os and an additional 2.5-V rail for the Ethernet PHYs. LDO1 and LD04 are enabled by default in the power up and down sequence, which LD02 is disabled by default. LDO1, configured as bypass, allows dynamic changes between 3.3 V and 1.8 V. This voltage change on LDO1 can be triggered by I2C or by setting the VSEL_SD pin high (LDO1=3.3 V) or low (LDO1=1.8 V). GPIO and GPO1 are free digital resources that are disabled by default but could be enabled through I2C if needed. GPO2 is pre-programmed to be enabled in the second slot of the power-up sequence with a duration of 6ms. It can be used to enable the external power switch and meet the processor sequence requirements. The switch must be selected with the right electrical spec to ramp and provide a stable output voltage within the 6ms duration of the second slot (before the PMIC starts the next slot in the power-up sequence). TPS6521908 comes pre-programmed, but maintains user-programmable functionality as a NVM device that allows full customization of the output voltages, sequencing, GPIO control, and more to best meet system needs.

Figure 4-8 and Figure 4-9 shows the power-up and power-down sequence programmed on TPS6521908.
Figure 4-7. TPS6521908 Powering AM243x
Figure 4-8. TPS6521908 Power-Up Sequence
Figure 4-9. TPS6521908 Power-Down Sequence
5 References

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated