TEXAS INSTRUMENTS

APPLICATION NOTE

GC2011-AN9802

Simultaneous Real -to -Complex Down Conversion of Four Signals Using a Single GC2011 Digital Filter Chip

April 14, 1998

Revision 0.0

This application note describes how to use a single GC2011 chip to perform the real-to-complex down conversion operation on four signals simultaneously. The input data is split into even and odd samples and then multiplexed into a time division multiplexed (TDM) format. The even sample TDM stream is input to the A-input of the chip and the odd sample TDM stream is input to the B-input. The I-half of the complex output will come out the A-output and the Q-half will come out on the B-output in the same TDM format as the input.

This app note also describes how two GC2011 chips can be used to perform the operations on 16 bit input data.

1.0 Quad Real to Complex Down Conversion

This mode takes advantage of the TDM mode described in application note GC2011-AN9801 to implement the real-to- complex down conversion operation described in Section 3.8 of the GC2011 data sheet. This mode allows four real signals to be down converted and filtered simultaneously by the chip. The sample rate of each signal is half the clock rate of the chip. The output signals will be complex I/Q pairs at one-fourth the chip's clock rate.

The user must divide the input samples into even and odd samples, and then format them as two TDM data streams. If the four input signals are identified as a(i), b(i), c(i) and d(i), then the even TDM stream will be the samples [a(0), b(0), c(0), d(0), a(2), b(2), c(2), d(2), a(4), b(4), c(4), d(4), a(6), ...], and the odd TDM stream will be the samples [a(1), b(1), c(1), d(1), a(3), b(3), c(3), d(3), a(5), b(5), c(5), d(5), a(7), ...]. The even stream is input to the A-input of the GC2011 chip and the odd stream is input to the B input. The TDM rate for the odd and even streams will be twice the sample rate of the input data. For example, if the input rate of each signal is 20 MHz, then the TDM rate will be 40 MHz. The clock rate to the chip is the same as the TDM rate.

The real-to- complex down conversion mode splits the 63 tap odd-symmetry filter between the two paths within the chip. The A-path uses the even coefficients and the B-path uses the odd coefficients. The even coefficients will have even symmetry and the odd coefficients will have odd symmetry. This means that the A-path should be in the dual, even symmetry TDM mode and the B-path should be in the dual odd-symmetry mode. In addition the down conversion operation requires every other input to be negated with the negations out of phase between the two paths. The negations are enabled using the input negation modes of the chip. The 16 bit data is handled by putting the chips in the 24 bit mode as described in the data sheet.

The control settings which put the chips in the proper modes are shown in Table 1.

Table 1: Quad Real to Complex mode

Address	0	1	2	3	4	5	6	7	8	9	10
Value	2CD8	0211	1CD8	0284	2000	0000	0470[1]	0000	0000	0000	0000

1. Assumes sum of coefficients is 16384 and output is rounded to the upper 12 bits

The 63 coefficients are stored in coefficient register 1 of each filter cell using the formula:

```
Store h(2k)   in memory address 129+4*k for k=0 to 15
Store h(2k+1) in memory address 193+4*k for k=0 to 15
```

where h(0) is the first tap and h(31) is the center tap of the 63 tap filter.

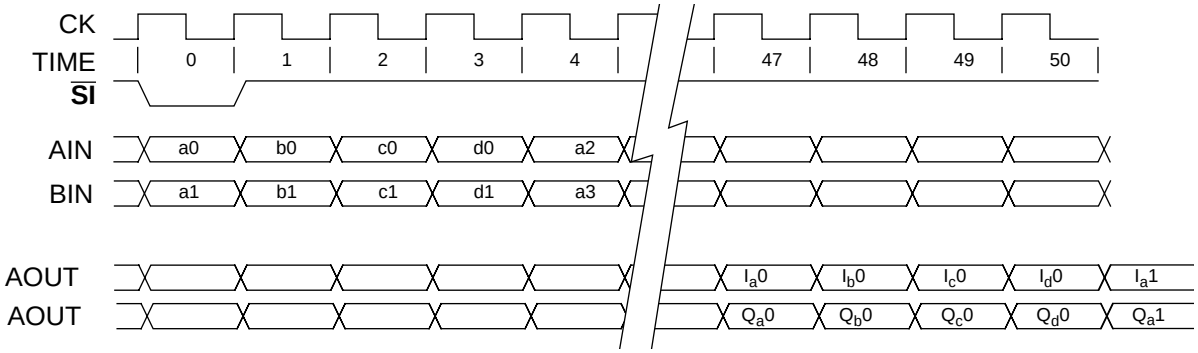

Figure 1. Quad Real to Complex Down Convert Mode I/O timing

2.0 16 bit Mode

The GC2011 chip can be operated in the 24 bit mode when the input data has more than 12 bits. The 24 bit mode combines both 12 bit paths within the chip into a single 24 bit data path. This means that two GC2011 chips are required to implement the quad down conversion operation. One chip will perform the A-path operations described in the previous section and the other chip will perform the B-path operations. As an example, this section describes how the quad down conversion can be performed on 16 bit data.

Two chips are required. Chip “I” will generate the I half of the complex output and chip “Q” will output the Q half of the complex output.

The 16 bit input data is split into the 12 MSBs and the 4 LSBs. The 12 MSBs are input into as the A input and the 4 LSBs are input as the 4 MSBs of the B input. The 8 LSBs of the B input should be grounded. The even data TDM stream is input into chip “I” and the odd data TDM stream is input to chip “Q”. The 16 bit I output will be the A output from chip “I”. The Q output will be the A output from chip “Q”.

The control settings which put the chips in the proper modes are shown in Table 2.

Table 2: Quad Real-to- Complex 16 bit mode

Address	0	1	2	3	4	5	6	7	8	9	10
chip-I	2CD8	0211	0CDC	0211	2000	0000	1070[1]	004C	0000	0000	0000
chip-Q	3CD8	0284	1CDC	0284	2000	0000	1070[1]	004C	0000	0000	0000

1. Assumes sum of coefficients is 16384 and output is rounded to the upper 16 bits

The 63 coefficients are stored in coefficient register 1 of each filter cell using the formula:

```
Store h(2k)   in memory address 129+4*k and address 193+4*k of chip “I” for k=0 to 15
Store h(2k+1) in memory address 129+4*k and address 193+4*k of chip “Q” for k=0 to 15
```

where h(0) is the first tap and h(31) is the center tap of the 63 tap filter.

3.0 Synchronization

Figure 1 shows how the TDM streams are synchronized relative to the $\overline{SI}$ input strobe. The $\overline{SI}$ strobe can be a one time sync pulse, or it can repeat every 8 clocks or any multiple of 8 clocks. It is assumed that the user will generate the TDM streams shown in Figure 1 using a simple programmable logic device[1]. This device will also need to be synchronized as shown in Figure 1. Three ways of synchronizing the chips are possible. First, an external device can generate the $\overline{SI}$ pulse. Second, the programmable logic device could generate the $\overline{SI}$ pulse, or third, the GC2011 can generate the $\overline{SI}$ pulse. The GC2011 can generate the pulse either as a one shot output on the $\overline{SO}$ pin, or as a periodic pulse on the $\overline{SO}$ pin using the chip’s internal counter. Bits 8 and 9 in the snapshot control register (address 10) are used to select the $\overline{SO}$ output source. See the datasheet for details. If the counter’s terminal count is selected, the $\overline{SO}$ output will pulse every 16 clocks. If the one shot is selected, then a pulse is generated when the user writes to address 11. In either case the $\overline{SO}$ output is used as the $\overline{SI}$ input to the GC2011 chips and to the programmable logic devices.

1. The user may note that this device will require lots of I/O pins to handle four 12 or 16 bit inputs and to output two 12 or 16 bit outputs. It may be cheaper and smaller to use two or more devices, each device handling a slice of the input words. For example, two devices could be used, one handling the upper 8 bits of each input word and another handling the 8 LSBs.

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