A Standardized Procedure for the Direct Measurement of Sub-Picosecond RMS jitter in High-Speed Analog-to-Digital Converters

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ABSTRACT

The advent of modern-day wireless communications systems as well as other high speed applications imposes exceedingly challenging demands on state-of-the-art Analog-to-Digital Converters (ADCs). The evolution of receiver architectures necessitates very high Signal-to-Noise Ratio (SNR) at intermediate frequencies that up until recently were impossible to achieve. Recent breakthroughs in converter architectures and silicon processes have however enabled the attainment of the required signal purity at input frequencies in excess of 100MHz. The predominant mechanism limiting high SNR at very high input frequencies in sampled systems is the timing (aperture) uncertainty of the sampling instant, commonly referred to as jitter. In order to achieve the required performance, today's best ADCs must feature jitter significantly below 1ps RMS. The ADS5420, a 14-bit 65MSps ADC from Texas Instruments, is specifically designed for high-IF sampling application and features industry-leading levels of jitter.

This application note proposes an innovative, reliable characterization technique that allows to measure ultra-low jitter levels while also discriminating noise contributions due to jitter from other phenomena (voltage reference and substrate noise, high-amplitude distortion) in ADCs. The jitter estimated with this method closely matches the one inferred from the SNR at high input frequencies, where noise is dominated by the aperture uncertainty. The document outlines therefore a standardized way for measuring and specifying jitter in ADCs, i.e. it proposes the unified test procedure that is notoriously absent in industry today.

Moreover, at the sub-picosecond resolution level required by the 14-bit high-IF ADC under test, any off-chip disturbances substantially affect the accuracy of the measurement also. In order to characterize the uncertainty, we show how the phase noise spectrum of the external clock source can be measured and converted into jitter by way of a rigorous formula.

INTRODUCTION

As the demand for high fidelity sampling of input frequencies in excess of 10MHz continues to increase, the aperture uncertainty (jitter) of the ADC itself is becoming the limiting factor of the achievable SNR of the whole signal-conditioning chain. Numerous methodologies have been proposed and discussed, since jitter performance still is one of the most challenging issues in state-of-the-art sampled systems [1-3]. The simplest and most widely adopted one infers the jitter value from the SNR measurements at high input frequency, where the random deviation s_T of the occurrence of the sampling edge translates into a random voltage error $s_{Vjitter}$ that dominates the noise deviation s_V. The retro-fitting is usually accomplished according to the formula [4]:

$$SNR = \frac{P_{IN}}{\sigma_V^2} \approx \frac{P_{IN}}{\sigma_{Vjitter}^2} = \frac{A_{IN}^2 / 2}{\sigma_T^2 \frac{(A_{IN}\omega_{IN})^2}{2}} \quad (1)$$

as applied to a sinusoidal input of amplitude A_{IN} and angular frequency ω_{IN} (= $2\pi f_{IN}$):

$$V_{IN}(t) = A_{IN} \sin(\omega_{IN} t) \quad (2)$$

Previous methods of estimating the jitter from the ADC's SNR were hampered by the imperfect knowledge of the real values of thermal noise, random non-linearity contributions [5], and any additional noise effects entering Eq. (1). Determining a f_{IN} high enough for the formula to be applied was somewhat of an arbitrary process. At very high input frequencies lots of dynamic effects such as substrate noise, signal leakage, complex device behavior, and many more, affect the noise term of the equation thus making the jitter estimation harder.
This application note describes a precise yet easy method of measuring the jitter of an ADC, and of any sampled-signal system. The description of an innovative technique for the determination of the jitter in sampled-input systems is first provided. The extraction of the period jitter from the SNR data collected on a 14b 65MSps ADC is then presented. Finally, the application note outlines the operative procedure to determine the jitter of the clock source.

CALCULATING JITTER THROUGH INPUT COHERENT SAMPLING

Coherent sampling (or locked-histogram) techniques have been successfully employed in the past [1,3,6,7] in order to estimate an ADC's jitter. However, this note presents a parametric analysis of the correlation between the jitter and the phase of the input at which noise is measured. The main advantage of the proposed technique is that the measurements obtained from the ADC under test are parametrically fitted to the true profile of the jitter in such a system, thus providing for the first time a true numerical solution to the problem. In addition, since the experimental results are fitted to the expected shape of the jitter vs. phase theoretical dependence, the ADC jitter can be measured down to levels lower than the ones allowed by the noise floor of the converter. Moreover, the technique eliminates the need to guessing what frequency is to be used for the analog input, in order to applying equations like the (1).

1. JITTER FORMULA DERIVATION

The theoretical RMS voltage error $\sigma_{Vjitter}$ induced by the clock cycle jitter (defined as the standard deviation of the Gaussian distribution of the periods, σ_T) is calculated through the input slope via the formula:

$$\sigma_{Vjitter} = \sigma_T \cdot \left|\frac{\partial V_{IN}(t)}{\partial t}\right| = \sigma_T \cdot A_{IN}\omega_{IN} \cdot \left|\cos(\omega_{IN} t)\right| \quad (3)$$

Equation (3) quantifies the well-known concept that when an ADC is sampling a sinusoidal input, the contribution of its jitter is much more pronounced when the sampling instant coincides with the zero crossing of the input, and has very little impact on the output noise when the sampling instant coincides with the top or bottom of the input sinewave. Fig.1 illustrates this concept: the Gaussian distributions shown on the right represent the histogram of the captured output samples of the ADC under test, in the two cases described.

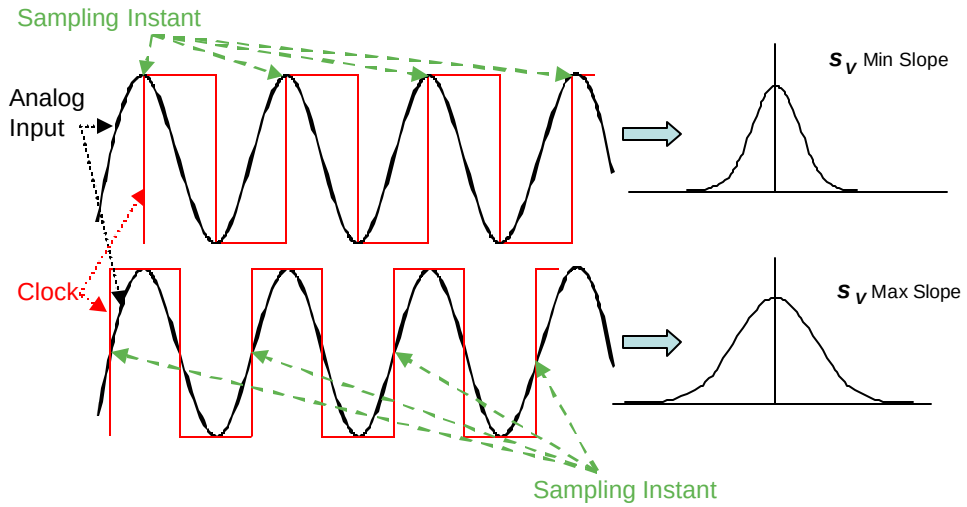

Fig. 1. Sinusoid sampling at different phases: sampling at the top of the input sinewave yields a much tighter output code distribution than sampling the input at its maximum slope (zero-crossing).

2. LOCKED-HISTOGRAM SAMPLING BASICS

Ideally, in order to remove any dynamic and non-linear effects and isolate the random contribution of the jitter, the best possible condition is to feed the quantizer of the ADC with *dc* input. Obviously, no real information could be derived from providing a signal to the input of the ADC at 0 Hz, other than the theoretical maximum attainable SNR and the converter's noise floor. However, a careful choice of input and clock frequencies and their relative phase makes the input of the ADC appear as *dc*. Experimentally this can be accomplished by coherently sampling the input; i.e., adopting a sampling rate $f_S=f_{IN}/N$ (N integer) to sample the same voltage in every period, or every few periods [6]. For a sinusoidal input, the sampling instant can be set to occur always at the V_{IN} peak (90° phase of the input waveform), always at the zero crossing (0° phase), or so forth at any intermediate point. After the SHA the signal to be quantized is indeed a *dc*, at different levels. This way, it is possible to obtain a distribution of the noise for each ADC code, as shown in Figure 2 where the differential input to the ADC V_{IN} equals 0V. In this case, the ADC output should be at its midscale value, 2^{13} = 8192 for the 14-bit ADC under test. Fig.2 exemplifies the experimental outcome of the procedure used to collect the code histograms at every *dc* level. If jitter is present, the Gaussian curve will be wider for samples taken close to the zero-crossings, and narrower when sampling near the peaks. In this latter case, the standard deviation of the noise represents only the thermal noise contribution, plus injections from substrate and any other terms not related to jitter. The adoption of "locked histogram" methods [6,7] guarantees a distinctive advantage over time-beat techniques [5] where the samples still change with time during the measurement, since dynamic non-idealities in the quantizer (reference bounce, hysteresis effects in the stages, etc.) are completely removed.

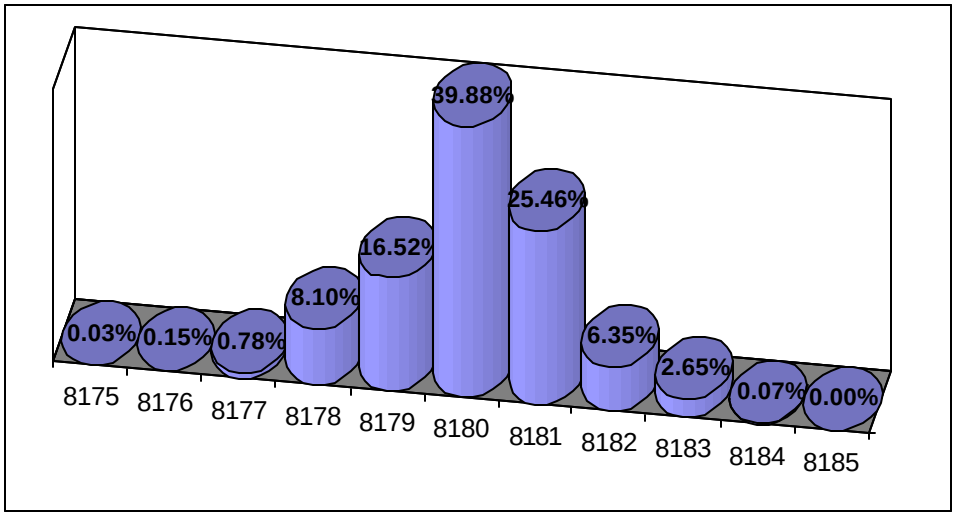

Fig. 2. Histogram of ADC under test with DC input applied (common-mode). The *x*-axis represents the ADC output code in LSBs, and the height of the barrels the percent hit count for each code in a run of 16384 sample points. The mean of the distribution is 8180 LSBs, indicating an offset of approximately 12 LSBs.

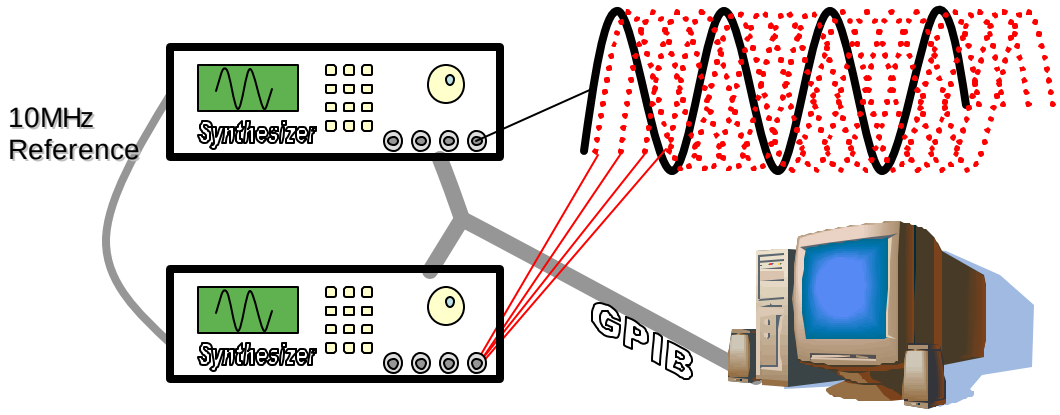

Fig. 3. Typical experimental setup used in order to apply the jitter measurement technique to an ADC. The two synthesizers are connected to the same 10MHz reference for coherency, and through GPIB synchronization commands the relative phase of one synthesizer's output can be incremented in 1° steps.

3. EXPERIMENTAL RESULTS

The setup used in the lab to implement the proposed technique is illustrated in Fig.3. Two synthesizers are referenced to the same 10MHz reference, ensuring coherency. These two instruments are used to provide the analog input and clock signals for the ADC under test. The two instruments are controlled remotely through a GPIB interface, and a PC running LabVIEW™ is used to control the test bed and automate the test process. Contrary to the typical implementations of such techniques, the relative phase of the clock and the analog input is controlled through the Phase-Frequency-Detector (PFD) of the synthesizer's PLL. This allows the two waveforms to be skewed from each other in phase by step increments as granular as permitted by the instrumentation - in this case, 1°. It is noteworthy to mention that this is a standard option offered by high-end instrumentation, hence no extra hardware is required. Through this technique, the main issue raised in [5] is then alleviated. Alternate methodologies employing tunable delay lines are much less convenient, do not offer the same level of automation, and can

introduce extra uncertainty. In order to prevent any high frequency effects from inhibiting the validation of our methodology, a sampling rate f_s = 30MSps was chosen for the following tests.

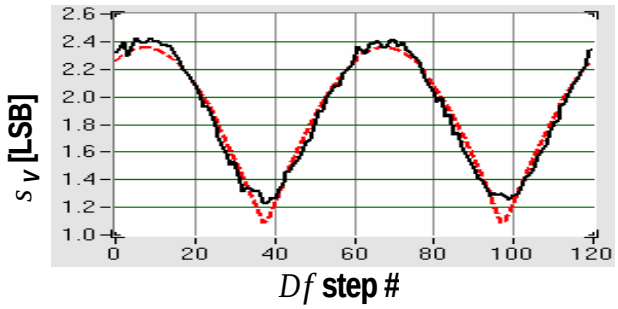

Fig. 4. Total s_V vs. number of Df steps at 30MSps clock rate, 30MHz coherent input: the s_V due to jitter amounts to 2.08LSB. The step between each phase sample is 3°, for a total of 360°.

The data collected at different relative phases Df of input vs. clock are represented in Fig.4. The statistic population (i.e., number of ADC samples collected) for every s_V measured was 4096 points. Although it is virtually impossible to control the absolute value of the phase of the input, the proposed technique does not require such control. In fact, the starting phase is irrelevant to the measurement, provided the entire cycle is covered. Once collected, the data can be fitted to the theoretical noise vs. phase dependency (pulsed cosine, Eq.(3)) through an LMS algorithm that identifies the correct starting phase as well. This method enables the extraction of the RMS jitter from the best-fit function found, providing an extremely accurate and robust measurement.

The dashed curve in Fig.4 has been obtained from the fitting algorithm. The analog input was chosen to be 30MHz, exactly the same frequency as the clock. Once a complete cycle of phase steps has been taken (corresponding to a complete cycle of 'sliding' the clock over the analog input), the data is parametrically fitted to the pulsed cosine shape as mentioned above. A Levenberg-Marquardt algorithm in LabVIEW ™ environment has been used to optimize baseline level, cosine amplitude, and starting phase of the experimental data. The striking resemblance of the theoretical behavior to the data across the whole phase range in Fig.4 provides a significantly enhanced level of precision than the traditional re-ordering of the measured points [1,6].

The same principle can be extended to undersampled inputs, yielding even stronger evidence. Figure 5 shows the measurement results and parametric fit for the case where the analog input f_{IN} =*90MHz* , with the ADC still sampling at 30 MSps. A key point to note here is the difference in the minima between the measured data and the fitted curve. The solid line (measured data) reaches a minimum higher than the theoretical one, since effects other than jitter contribute to the overall noise measured. The ultimate limitation in the minimum measurement therefore is not given by jitter, but is rather the thermal noise floor of the ADC. In this way, the fitted curve yields a very powerful point, which in the past was impossible to attain: it allows discriminating between jitter and other noise contributors (such as thermal noise). Finally, the technique was applied once more in the case where f_{IN} =150 MHz. This means only 1 sample was taken out of every 5 input periods. Figure 6 shows the results for this case. Obviously, the maxima observed are now significantly higher, as expected by the increased effect of jitter on higher analog inputs. As a consequence, the adherence of the experimental curves to the theoretical, jitter-dominated ones becomes closer and closer for higher values of the input frequency f_{IN}.

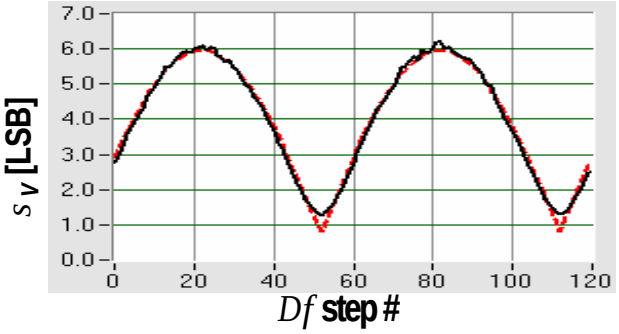

Fig. 5. Total s_V vs. Df steps at 30MSps rate, 90MHz coherent input. The s_V RMS difference is now 5.86LSB.

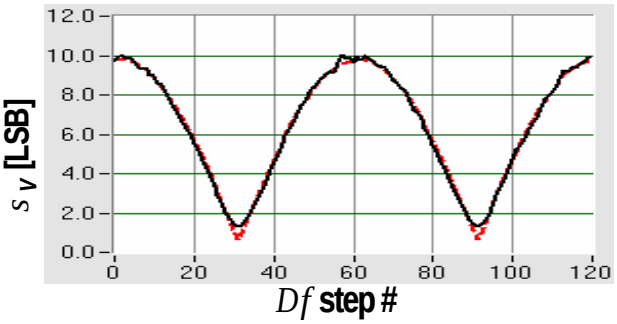

Fig. 6. Total s_V vs. Df steps at 30MSps rate, 150MHz coherent input. The jitter-related s_V is 9.91LSB.

In order to extract the cycle jitter from the fitted curves above, it is now sufficient to reverse (3) where $cos(w_{IN}t) = 1$. The value extracted from the best fit of 2.08LSB noise observed at 30MHz input is $s_T = 1.51$ps; 5.86LSB at 90MHz give $s_T = 1.42$ps; finally, 9.91LSB at 150MHz are fitted by $s_T = 1.44$ps. It is important here to note the virtual congruence of the results between the different cases. As stated earlier and as expressed by (3), $s_{Vjitter}$ is directly proportional to f_{IN} (for constant s_T). Therefore an added advantage of the technique is that noise contributors that do not scale with analog input frequency can be isolated. This constitutes a notable advantage of the technique over the complexity of alternative approaches aimed at discriminating the jitter from other noise sources ([5]). The above measured results, however, indicate a significant problem with jitter in the overall system. Since this is a sampled system, jitter in any part of the external or internal to the ADC clock sources can adversely impact overall performance.

JITTER ESTIMATION FROM SNR

In order to assess the internal clock jitter in a data converter without carrying out dedicated measurements, designers usually resort to the classical derivation of the parameter by fitting the SNR at high input frequency. The series of SNR vs. f_{IN} collected at 30MSps is represented in Fig.7, along with the theoretical SNR limitation set by the jitter, and calculated as per (1).

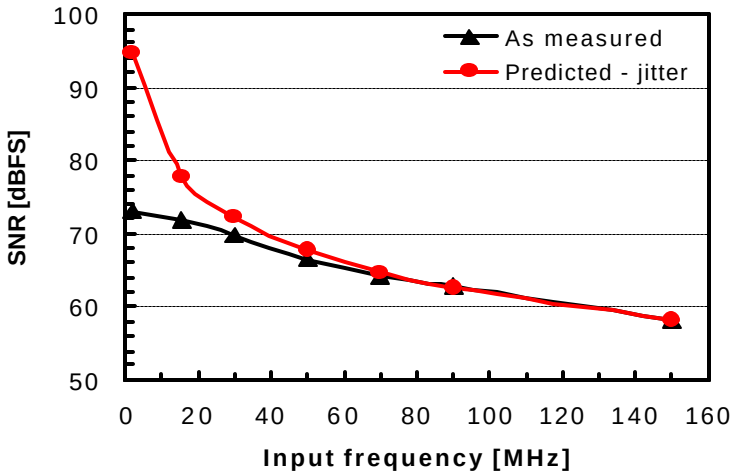

Fig. 7. SNR vs. f_{IN} of a 14b switched-capacitor pipelined ADC, measured at 30MSps, -1dBFS. The SNR is thermal-noise-limited at low f_{IN}, jitter-limited at f_{IN} >60MHz (external clock source jitter >1ps).

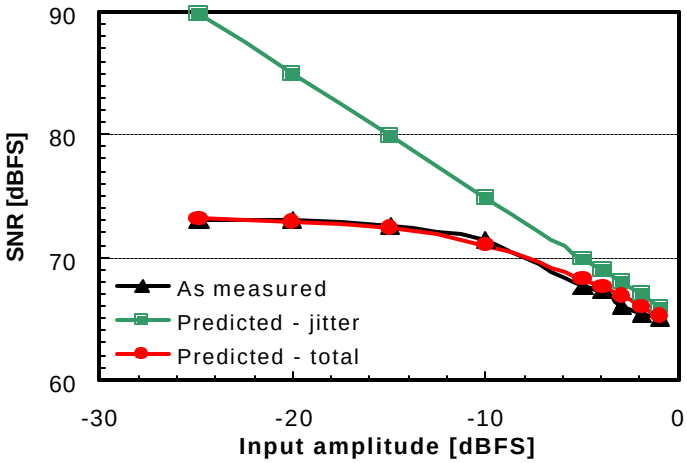

Fig. 8. Measured and predicted SNR vs. A_{IN} at f_{IN} = 150MHz. The high jitter level overwhelms any other effect, limiting SNR at high A_{IN}.

The period jitter used to fit the ADC performance at high IF projects a one-cycle s_T = 1.48ps, in very good accordance with the value previously obtained, which validates the method proposed. Fig.8 shows the SNR matching against A_{IN} when the same s_T is used, and the thermal noise - dominant at low amplitudes, per (3) - is assumed to fit the plateau observed on the experimental data. However, it is important to remark that this happens for high jitter values only. In our case, once the noise of the external clock is filtered out the total jitter estimated through this technique decreases to 580fs, whereas the SNR only improves by 1.3dB at f_{IN} = 150MHz and A_{IN} = -1dBFS, which would still project a pessimistic s_T = 1.27ps. This uncovers the presence of additional limitations to the ADC noise other than sheer jitter. The amplitude-dependent nature of this effect actually constitutes a precious input for the designer, pointing to the need for improvement of the SHA behavior at the signal peaks.

EXTERNAL CLOCK SOURCE JITTER

Final target of the designer's analysis is to improve the clock circuit in order to reduce the jitter figure. This entails the discrimination of the jitter components due to the external clock source, and to the internal clock conditioning and distribution integrated circuitry. The first task has been accomplished through a phase noise measurement system operated in phase-lock configuration, and fed with the clock source at frequency f_s. The phase noise vs. offset frequency f_n function, $L(fn)$, detected by the instrument, is a.k.a. Single-Sideband to Carrier Ratio or SSCR. The SSCR profile of a high-end time reference source is typical of a stabilized quartz precision source, with extremely reduced levels of close-in phase noise and a low white frequency noise component as low as -150dBc/Hz. The phase noise is then processed by means of the formula [8]:

$$s_T = \frac{1}{f_s^2}\sqrt{\int_{f_1}^{f_2} 2 f_n^2 \cdot SSCR(f_n) \cdot sinc^2\left(\frac{f_n}{f_s}\right) df_n} \qquad (4)$$

In practice, the expression converts the phase- into frequency-noise spectrum (according to the Laplace transform rule $S_f = jwS_f$) and weighs it through the *sinc* function, to account for the uniform jitter accumulation in the time span $0 \rightarrow T$ [8]. The integral of the noise spectral density is extended from the reciprocal of the total observation time $f_1 = 1/T_{obs}$ (about 4kHz) to the maximum frequency allowed by the instrument f_2 (40MHz in our setup). By applying (4) to the SSCR spectrum as observed from a phase noise analyzer available from Agilent, or Aeroflex Comstron, the jitter of the external 30MHz source is calculated to be about 1.36ps, dramatically decreasing to 25fs after bandpass-filtering the source. These state-of-the-art numbers emphasize the accuracy of the measurement, together with the impervious difficulty of it. The contribution just figured out is to be discounted from the aperture jitter determined previously in this document, to isolate the additional jitter introduced by the on-chip regeneration/distribution circuitry. The RMS subtraction returns 580fs, to be minimized in the design of the integrated preamplifier/tapered buffer chain. Utilizing the new, ultra-low jitter external clock signal available and this jitter measurement technique, the designer is able to accurately measure the magnitude of the jitter improvement needed, fine-tune the simulation tools to match simulated and experimental data, and accordingly redesign the circuit with heightened degree of confidence. The

application of the same technique to the enhanced clock design yielded the profile of Figure 9, where the overall jitter measured was in the order of 250fs RMS. This state-of-the-art figure enables the attainment of very high SNR readings over input frequency, as can be seen in Figure 10. An SNR of 70.5dBFS was measured at a very high 150MHz input frequency, which fully validates the efficacy of this measurement technique for design optimization.

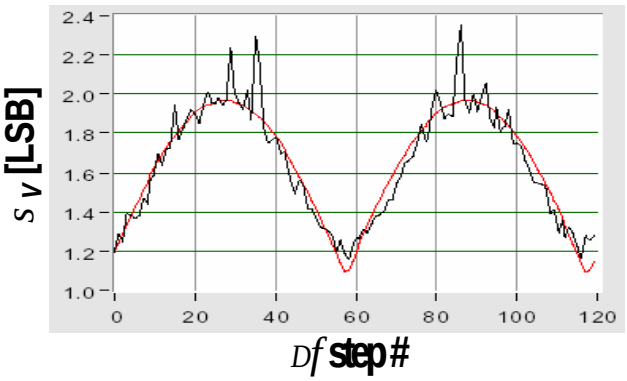

Fig. 9. Final jitter test run on the optimized clock decoupling ADS5420 version, with external filtered clock. The measured value for the jitter is 250fs RMS. This dramatically reduced jitter value exposes statistical effects of many noise sources which were hidden in Fig. 3, but are effectively averaged out by the coherent sampling algorithm proposed.

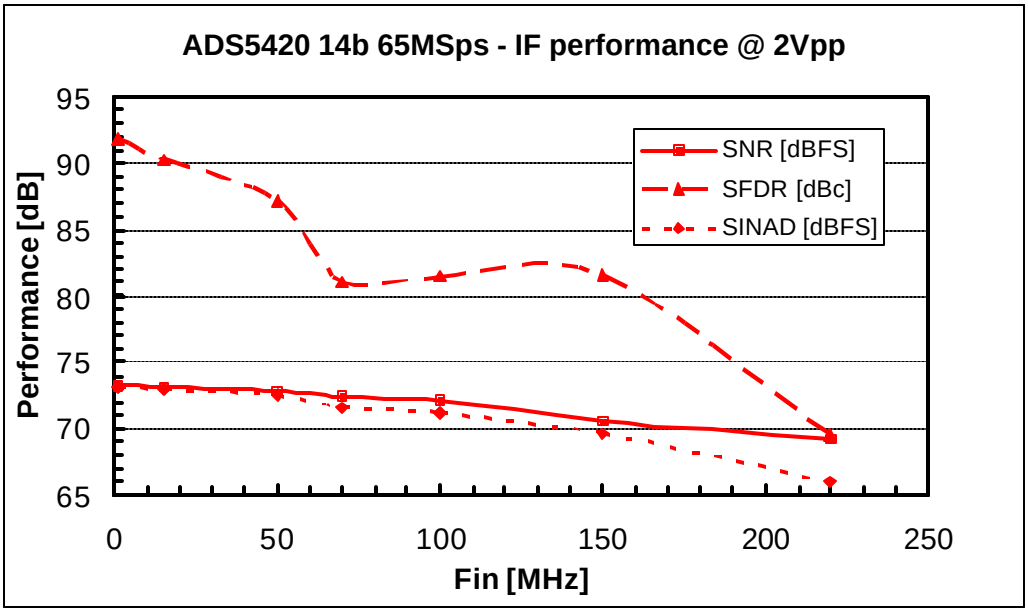

Fig. 10. f_{IN} sweep at 65MSps sampling rate on TI's ADS5420 14 bit 65MSps A-to-D converter for wireless infrastructure applications. The design changes implemented as a result of the application of the jitter measurement technique enabled a dramatic improvement in the ADC's IF performance.

The measured value of 250fs RMS synthesized in the new silicon was then used to construct a theoretical SNR vs f_{in} curve as shown in Figure 11. The theoretical line is of course unbounded as the input frequency to the ADC approaches DC, but converges to the measured numbers as the frequency increases. Since the SNR contribution yielded by jitter is so much lower than before, other noise effects manage to limit the SNR plot before jitter becomes the ultimate performance-setting phenomenon, right until 200MHz. This circumstance points to further margins of improvement to be pursued in the circuit before the best possible performance is reached for this pipeline architecture.

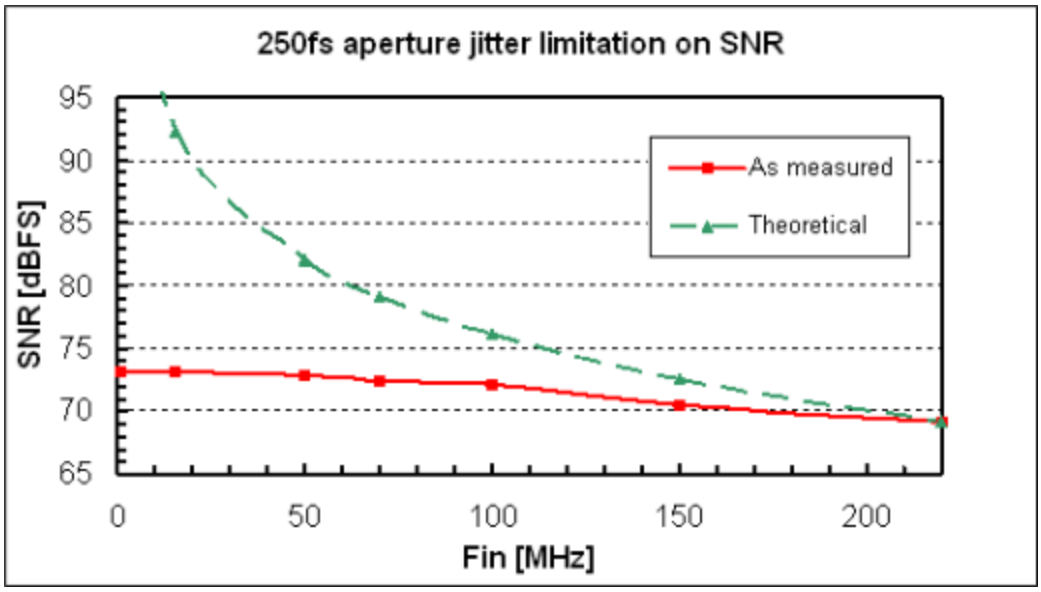

Figure 11 . Theoretical and measured SNR readings for a given aperture jitter of 250fs.

SUMMARY AND CONCLUSIONS

This application note presented a convenient and accurate method for measuring sub-picosecond RMS jitter of sampled systems using an application of the locked histogram coherent sampling method. The technique presented enables a direct, parametric measurement of the sampling instant uncertainty, and has found full confirmation in the SNR performance of the converter under test. Applied to the ADS5420, a state-of-the-art high speed 14-bit ADC by Texas Instruments, this technique measured an RMS jitter value of 250fs. This ultra-low jitter value of the ADC allows a dynamic performance in excess of 70dBFS SNR at 150MHz input frequency. The application of the proposed technique can lead to a standardized way of measuring the aperture uncertainty of high-speed ADCs, and can be a valuable tool in the design of such devices for high input frequency applications. The technique presented was also used to discriminate the timing uncertainty caused by the internal ADC clock circuitry from the one caused by the external synthesizer used as an input clock to the ADC. This methodology can easily be extended to any sampled system, allowing the system designer the flexibility to directly measure the system's jitter performance and accordingly improve the system design.

TO PROBE FURTHER

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