Analog and Mixed-Signal Products

Analog Applications Journal

November 2000

TEXAS INSTRUMENTS

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI's product-specific websites listed at the end of each article.

Smallest DSP-compatible ADC provides simplest DSP interface

By Joe Purvis
Application Specialist

Introduction

This article features TI's new TLV2541 12-bit data converter and highlights the ease with which analog signals can be converted.

Family features

The TLV2541 is one of six related devices, presented in Table 1.

Table 1. TLV25xx family features

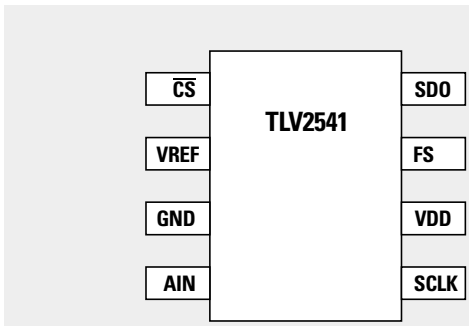
DEVICE NUMBER	DESCRIPTION
TLV2541	1-channel, unipolar input, 200-KSPS*, 8-pin MSOP
TLV2542	2-channel, unipolar input, 200-KSPS*, 8-pin MSOP
TLV2545	1-channel pseudo-differential, 200-KSPS*, 8-pin MSOP
TLC2551	1-channel, unipolar input, 400-KSPS*, 8-pin MSOP
TLC2552	2-channel, unipolar input, 400-KSPS*, 8-pin MSOP
TLC2555	1-channel pseudo-differential, 400-KSPS*, 8-pin MSOP

*DSP interface

TLV2541

The pin-out for this device is shown in Figure 1. A significant feature is that the TLV2541 will support a typical digital signal processor (DSP) with no glue logic. It will also support a typical serial port protocol, such as can be found in 8- and 16-bit microprocessors. The device does not support interrupts or end-of-conversion (EOC) flags.

Figure 1. TLV2541 device pinout



Timing diagram

The TLV2541 does not contain any user-configuration registers. Therefore, it is not possible to write to the device. After power-up, the ADC will power up in a known state.

There are two ways to trigger a conversion:

1. *Microprocessor mode*
   If the frame sync (FS) signal is **HIGH** during the falling edge of $\overline{CS}$, the ADC is considered to be in microprocessor mode. In this mode the sample/convert cycle occurs on every falling edge of $\overline{ADC\_CS}$. The user must ensure that $\overline{CS}$ remains active (LOW) for the entire sample/convert cycle (Figure 2).
   In this example, when $\overline{CS}$ is asserted LOW, the data from the previous sample/convert cycle is available on the falling edges of SCLK. The data received by the host system is B720 (h).
2. *DSP mode*
   If the FS signal is **LOW** during the falling edge of $\overline{CS}$, the ADC is said to be in DSP mode. In this mode, sample/convert cycles occur after FS has transitioned from HIGH to LOW (Figure 3).
   In this example, when $\overline{CS}$ is asserted LOW, the FS signal is LOW; therefore, the MSB of data output from the ADC will be held until the ADC detects FS↓. At that time, data from the previous sample/convert cycle is available on the falling edges of SCLK. The data received by the host system is 1640 (h).
   As can be seen in Figures 2 and 3, the serial data transmitted from the ADC in both instances follows a big endian data model (MSB to LSB).

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Figure 2. Conversion trigger timing in microprocessor mode

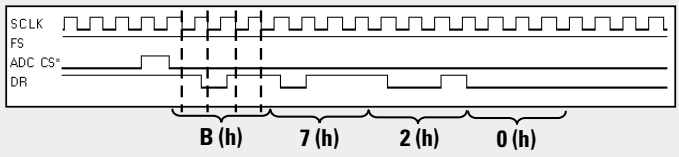
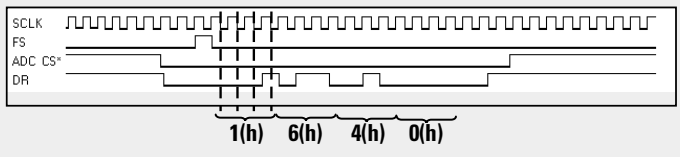


Figure 3. Conversion trigger timing in DSP mode



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Device evaluation

The device previously described is supported in an evaluation kit (Multi-Converter EVM). This kit contains:

- 0309 assembly, including socket support for all ADCs in this family, in addition to various digital-to-analog converters (DACs);
- samples of all available ADCs—TLV2541, TLV2542, TLV2545, TLC2551, TLC2552, and TLC2555; and
- samples of all available DACs—TLV5606, TLV5616, TLV5617A, TLV5618A, TLV5623, TLV5624, TLV5625, TLV5626, TLV5636, TLV5637, and TLV5638.

The EVM can be set up very quickly. Just follow these steps:

1. Apply power to the EVM.
2. Press the RESET button momentarily.
3. Press the START button momentarily.

Check that conversions are occurring by inspecting TP7 and TP20 (see Figure 4) via an oscilloscope. TP7 displays the input signal; TP20 displays the output signal.

Programming the TLV2541 ADC

Programming the TLV2541 can be achieved with a minimum of effort, since there are no registers to set up. The converter begins a sample/convert cycle every time the $\overline{CS}$ signal falls (microprocessor mode) or FS falls (DSP mode).

For clarity, sample code for both the microprocessor and the DSP is presented. The code written in these examples is referenced to the EVM system previously discussed and includes a TLV5636 DAC as a partner device for the TLV2541.

TLV2541 ADC flow

The goal of this code is to demonstrate the fundamental operation of the device. Several operations need to be completed successfully to achieve this goal, regardless of whether the platform is a DSP's serial port or a microprocessor's serial port:

- The host system (DSP or microprocessor) must be set up.
- The analog input signal must be sampled and converted.

Figure 4. EVM functional diagram

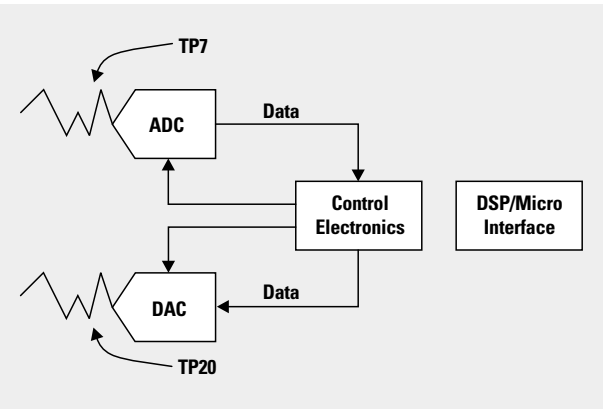
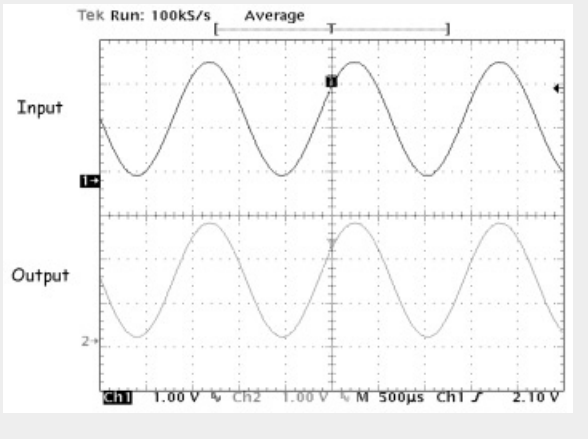


Figure 5. TLV2541 input/output comparison



- Converted data must be read into the host system as a serial bitstream.
- Some processing of the data word is necessary in preparation for writing the data to the DAC.
- The processed data is written to the DAC.

If these steps are completed successfully, the output signal from the on-board DAC will approximate the input signal from the ADC, as shown in Figure 5.

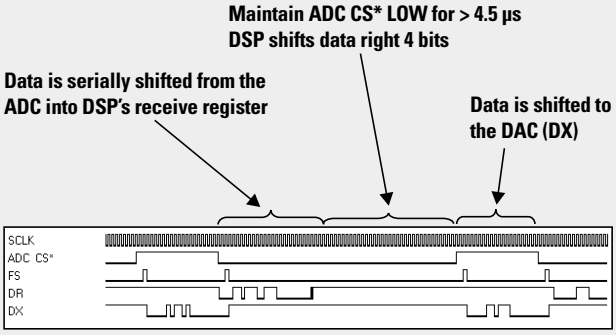
The only limit to this is the speed with which the DSP/microprocessor can read, process, and output the data.

Now that the general points have been discussed, example DSP code and microprocessor code are presented.

DSP code

The following code example in assembly language shows serial port access of a Texas Instruments TMS320C31 DSP using the DSP Starter Kit (DSK). Figure 6 shows a typical example of the serial port data transfer timing.

Figure 6. Serial port timing example



Serial port setup

The TMS320C31 contains one serial port. This article does not discuss the details of the serial port. See the references for more details. Table 2 lists the registers that must be set up and the data that should be written to the register in order to set up the serial port properly.

Table 2. DSP serial port setup

REGISTER NAME	ADDRESS (HEX)	DATA (HEX)
Serial-port Global Control	808040	0C140044
FSX/DX/CLKX Port Control	808042	00000111
FSR/DR/CLKR Port Control	808043	00000111
R/X Timer Control	808044	01CF
R/X Timer Counter	808045	00100010
R/X Timer Period	808046	00000000
Data Transmit	808048	Variable
Data Receive	80804C	Variable

Initiate a sample/convert

Refer to Figure 3 for assistance.

- Drive $\overline{\text{ADC CS}}$ LOW.

```
ldi       2,iof
```

- Generate an FS signal.

```
sti       r0,@xdata
```

Read the data from the previous conversion into the host system

- Because $\overline{\text{ADC CS}}$ was held LOW and FS was generated in the previous cycle, the serial data was automatically received by the DSP's receive register (DR) and assembled into a 16-bit word. This data can now be read into the DSP.

```
ldi       @rdata, r0
```

- The user must maintain $\overline{\text{ADC CS}}$ LOW for the complete sample/convert cycle. If $\overline{\text{ADC CS}}$ is de-asserted too early, the conversion cycle will be lost. There are a number of ways to achieve this delay; however, the simplest, without any knowledge of the DSP's serial port, is to include a decrement loop, timed for about 4.5 µs.

```
          ldi     0x10,r1
delay1    subi    1,r1
          bnz     delay1
```

The register is loaded with a value of 16 (10h) and is successively decremented until the register contains 0. The Z-flag in the DSP's status register is set, and the delay time is complete. It's clear that the number loaded is arbitrary and, depending upon the speed of the DSP, may not be optimal.

Maintaining $\overline{\text{ADC CS}}$ LOW for at least 4.5 µs achieves two objectives: It allows the ADC time to convert the analog input, and it also lets the ADC transmit the previously converted data to the DSP.

Data process

It's clear from the data formats of the ADC (Figure 7) and the DAC (Figure 8) that the host system cannot simply write the ADC data to the DAC. The ADC data first must be shifted right by 4 bits as shown in Figure 9.

The control nibble sent to the DAC is defaulted to 0000(b). Other control nibbles may be written to the DAC; these are at the user's discretion. However, 0000(b) is interpreted by the DAC (TLV5636) as:

- Write to the DAC latch.
- DAC is in slow mode.
- Normal operation.

```
lsh       -4,r0
```

See Reference 2 for further information.

Continued on next page

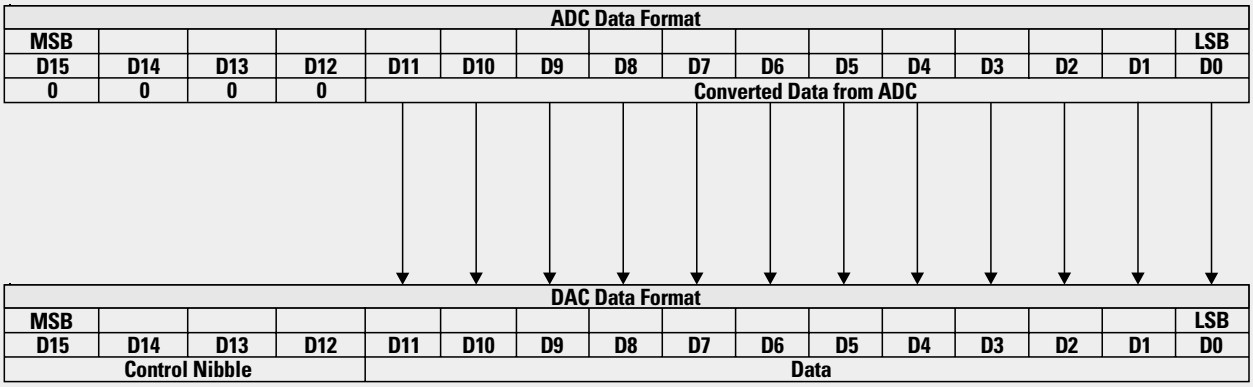
Figure 7. Data received from the ADC

ADC Data Format															
MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Converted Data from ADC												0	0	0	0

Figure 8. The DAC requires a 16-bit word that is composed of 2 parts

DAC Data Format															
MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Control Nibble				Data											

Figure 9. ADC data is shifted right 4 bits before it is written to the DAC



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Processed data is written to the DAC

The data is written to the DAC bit by bit upon successive falling edges of SCLK. This process is initiated after $\overline{\text{DAC}}$ $\overline{\text{CS}}$ is asserted LOW and FS falls. After the 16th falling SCLK edge, the data in the DAC latch will be sent to the DAC for conversion.

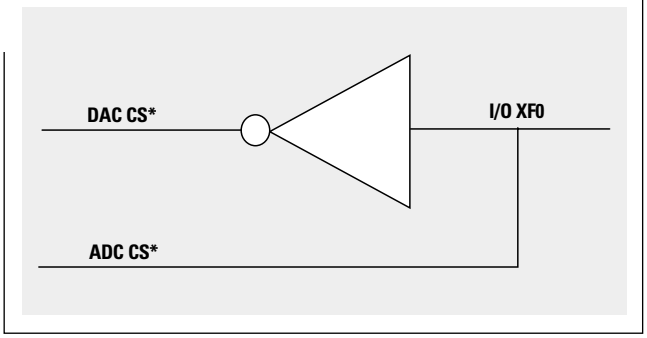
The ADC and the DAC share the same general-purpose I/O signal, I/O XF0. Selection of either device is mutually exclusive; i.e., if the ADC is selected the DAC is not selected, and if the DAC is selected the ADC is not selected. The ADC is selected by asserting I/O XF0 LOW; thus the DAC is selected by de-asserting I/O XF0 HIGH (see Figure 10).

```
ldi     6,iof
sti     r0, @xdata
```

Wait until all 16 bits have been transferred serially to the DAC.

```
        ldi     0x10,r1
delay2  subi    1,r1
        bnz     delay2
```

Figure 10. Simple inverter allows ADC and DAC to share the same I/O signal



The code portions just discussed can be assembled into the DSP program as given below:

Program code sample

```
.start  "SPORT", 0x809802
       .sect "SPORT"
       .entry BEGIN

                                ;Serial Port 0 registers
sport       .set 0x808040       ;Serial Port 0 global control register
xpctrl      .set 0x808042       ;FSX/DX/CLKX port control
rpctrl      .set 0x808043       ;FSR/DR/CLKR port control
rxtctrl     .set 0x808044       ;R/X timer control register
rxtcnt      .set 0x808045       ;R/X timer counter register
rxtprd      .set 0x808046       ;R/X period register
xdata       .set 0x808048       ;R/X Data transmit register
rdata       .set 0x80804C       ;R/X Data receive register
t0_GO       .set 001cfh         ;Timer cfg to GO

sp0_cfg     .word   0x0c140044
s0_rxcntr   .word   0x00100010
s0_rxprd    .word   0x00000000
```

Program code sample (Continued)

```
************************************************
* Main Program
************************************************
BEGIN    ldi    6,iof            ;Make sure ADC is not selected
         ldi    0x00000111,r0    ;Setup Serial Port:-
         sti    r0,@xpctrl           ;FSX is a serial port pin
                                     ;DX is a serial port pin
                                     ;CLKX is a serial port pin
         sti    r0,@rpctrl           ;FSR is a serial port pin
                                     ;DR is a serial port pin
                                     ;CLKR is a serial port pin
         ldi    @s0_rxcntr,r0    ;Counter value
         sti    r0,@rxtcnt       ;Load the counter with 15 for receive and transmit
         ldi    @s0_rxprd,r0     ;period value

         sti    r0,@rxtprd       ;Load the period with 3e for receive and transmit
         ldi    t0_GO,r0         ;Start timer0 config
         sti    r0,@rxtctrl      ;Start the counter
         ldi    @sp0_cfg,r0      ;0x0c140044 config for SP0 GCR
         sti    r0,@sport        ;configure sp0 GCR

*********************************************************************
* Sample and convert here
*********************************************************************

loop     ldi    2,iof            ;Assert CS* to select ADC
         sti    r0,@xdata        ;Generate an FS pulse

         ldi    @rdata,r0        ;Read ADC from the receive register

         ldi    0x10,r1          ;Wait for the ADC to complete a sample/convert cycle.
delay1   subi   1,r1             ;Wait for previous data to be received by DRR.
         bz     delay1           ;First conversion will be garbage.

          lsh   -4,r0            ;Shift the ADC data right 4 bits

         ldi    6,iof            ;Assert DAC CS*
         sti    r0,@xdata        ;Write data to the DAC

         ldi    0x10,r1          ;Wait for the serial data to be loaded into the DAC
delay2   subi   1,r1             ;before beginning another sample convert cycle.
         bz     delay2

         b      loop

         .end
```

Microprocessor code

The following code example in assembly language shows the SPI interface of the Motorola MC68HC912B32 microprocessor. General-purpose IO PS3 is used to generate frame sync (FS).

Since SPI is an 8-bit protocol, the communication to the ADC and DAC is achieved over two cycles. Figure 11 shows the converted data being read from the ADC and the processed data (4-bit shift) being written to the DAC.

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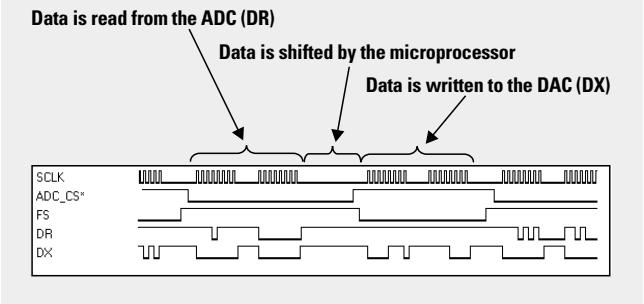
Figure 11. Code transfer timing example



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Serial port setup

This article does not discuss the details of the serial port. See Reference 4 for more details. Table 3 lists the registers that must be set up and the data that should be written to the register in order to set up the serial port properly.

Table 3. Microprocessor serial port setup

REGISTER NAME	ADDRESS (HEX)	DATA (HEX)
SPI Control Register 1	00D0	0054
SPI Control Register 2	00D1	0000
SPI Baud Rate Register	00D2	0001
SPI Status Register	00D3	0080 (to clear)
SPI Data Register	00D5	Variable
Port S	00D6	Variable
Data Direction Register for Port S	00D7	00EC

Initiate a sample/convert: Read data into host system

Refer to Figure 2 for the timing diagram, FS = 1.

- Drive ADC CS* LOW.
  `MOVB #$80, PORTS`
- Generate 8 SCLKs to ADC by initiating a dummy data transfer.
  `MOVB #$00, SP0DR`
- Load the first 8 bits of sampled data in accumulator A.
  `LDAA SP0DR`
- Generate 8 SCLKs to ADC by initiating a dummy data transfer.
  `MOVB #$00, SP0DR`
- Load the second 8 bits of sampled data in accumulator B.
  `LDAB SP0DR`
- Store 16 bits of sampled data (accumulator D) in DATA.
  `STD DATA`

Process data

As in the DSP example, the control nibble sent to the DAC is defaulted to 0000(b). Other control nibbles may be written to the DAC; these are at the user's discretion. There are various ways to right shift the ADC data by 4 bits; in this example a simple loop is used.

- Load index register X with the value 4.
  `LDX #$0004`
- Loop four times, shifting right once on each iteration of the loop, then store the shifted values from accumulators A and B.

```
LOOP:   LSRD
        DBNE X,LOOP
        STAA UPPER_BYTE
        STAB LOWER_BYTE
```

Processed data is written to the DAC

Since the MC68HC912 operates on an 8-bit data word, the upper and lower bytes must be sent individually. This is done on a bit-by-bit basis, with MSB first. The ADC must be deselected, which will select the DAC as described in the DSP example given previously.

- Disable the ADC while enabling the DAC.
  `MOVB #$88, PORTS`
- Send DAC FS LOW by clearing the PS3 bit.
  `BCLR PORTS, #%00001000`
- Send upper and lower data bytes to the DAC.

```
MOVB UPPER_BYTE, SP0DR
BSR FLAG
MOVB LOWER_BYTE, SP0DR
BSR FLAG
```

- Branch back to sample routine.

The code portions just discussed can be assembled into the microprocessor program as given below:

BRA sample program code

```
SP0CR1:      equ $D0      ;SPI 0 Control Register 1
SP0CR2:      equ $D1      ;SPI 0 Control Register 2
SP0BR:       equ $D2      ;SPI 0 Baud Rate Register
SP0SR:       equ $D3      ;SPI 0 Status Register
SP0DR:       equ $D5      ;SPI 0 Data Register
PORTS:       equ $D6      ;Port S Data Register
DDRS:        equ $D7      ;Port S Data Direction Register
Upper_Byte:  equ $0B00
Lower_Byte:  equ $0B01

*************************************************
* Main Program
*************************************************
ORG     $0800             ;User code data area, start main program at $0800
DATA    FCB  00,01        ;Set up 16 bit DATA variable format
MAIN:
        BSR INIT          ;Subroutine to initialize SPI registers
        BSR SAMPLE        ;Subroutine to start transmission
```

BRA sample program code (Continued)

```
INIT:
       BSET DDRS, #%11101100      ;Configure PORT S inputs/outputs:
                                  ;SS/CS, SCK, MOSI, MISO, PS3, PS2, TXD,
                                  ;RXD
       BSET SP0BR, #%00000001     ;Set Baud Rate
       BSET SP0CR1, #%01010100    ;SPI Configuration Register 1(SP0CR1):
                                  ;SPIE, SPE, SWOM, MSTR, CPOL, CPHA, SSOE,
                                  ;LSBF
       BSET SP0CR2, #%00000000    ;SPI Configuration Register 2 (SP0CR2):
                                  ;-,-,-,-,-,-,SSWAI, SPCO
       MOVB #$00, UPPER_BYTE      ;Set upper byte to zero
       MOVB #$00, LOWER_BYTE      ;Set lower byte to zero
       RTS                        ;Return from initialization subroutine

*********************************************************************
* Sample and convert here
*********************************************************************
SAMPLE:
       MOVB #$08, PORTS           ;Sets ADC CS* LOW, DAC CS* HIGH, FS HIGH
       MOVB #$00, SP0DR           ;Write zero value to data register
                                  ;to generate SCLK for ADC
       BSR FLAG                   ;Clear SPIF
       LDAA SP0DR                 ;Load first ADC Sample (Upper Byte)
       MOVB #$00, SP0DR           ;Write zero value to data register
                                  ;to generate SCLK for ADC
       BSR FLAG                   ;Clear SPIF
       LDAB SP0DR                 ;Load second ADC Sample (Lower Byte)
       STD DATA                   ;Store ACCA and ACCB in Data

       LDX #$0004                 ;Load value 4 in X
LOOP:                             ;Start loop to shift right by four
       LSRD                       ;Right Shift ACCD
       DBNE X,LOOP                ;Loop "X" times
       STAA UPPER_BYTE            ;Store accumulator A in Upper Byte
       STAB LOWER_BYTE            ;Store accumulator B in Lower Byte

       MOVB #$88, PORTS           ;Set DAC CS* LOW, ADC CS* HIGH, FS HIGH
       BCLR PORTS, #%00001000     ;Set FS to DAC(PS3) LOW
       MOVB UPPER_BYTE, SP0DR     ;Load Data Register with Upper Byte
       BSR FLAG                   ;Clear SPIF
       MOVB LOWER_BYTE, SP0DR     ;Load Data Register with Upper Byte
       BSR FLAG                   ;Clear SPIF

       BSET PORTS, #%00001000     ;Set FS for the DAC HIGH
       BRA SAMPLE                 ;Go back and take another sample

FLAG:
       BRCLR SP0SR,#$80,FLAG      ;Wait for flag to clear.
       RTS
```

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. TLV2541 Data Sheet	slas245
2. TLV5636 Data Sheet	slas223
3. TMS320C31 Data Sheet	sprs035
4. Motorola, MC68HC912B32 Technical Summary	—

Related Web sites

www.dataconverter.com

http://dspvillage.ti.com/docs/ccstudio/ccstudiohome.jhtml

www.ti.com/sc/docs/products/analog/*device***.html**
Replace *device* with tlc2551, tlc2552, tlc2555, tlv2541, tlv2542, tlv2545, tlv5606, tlv5616, tlv5617a, tlv5618a, tlv5623, tlv5624, tlv5625, tlv5626, tlv5636, tlv5637, or tlv5638

www.ti.com/sc/docs/products/dsp/tms320c31.html

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Hardware auto-identification and software auto-configuration for the TLV320AIC10 DSP Codec—a "plug-and-play" algorithm

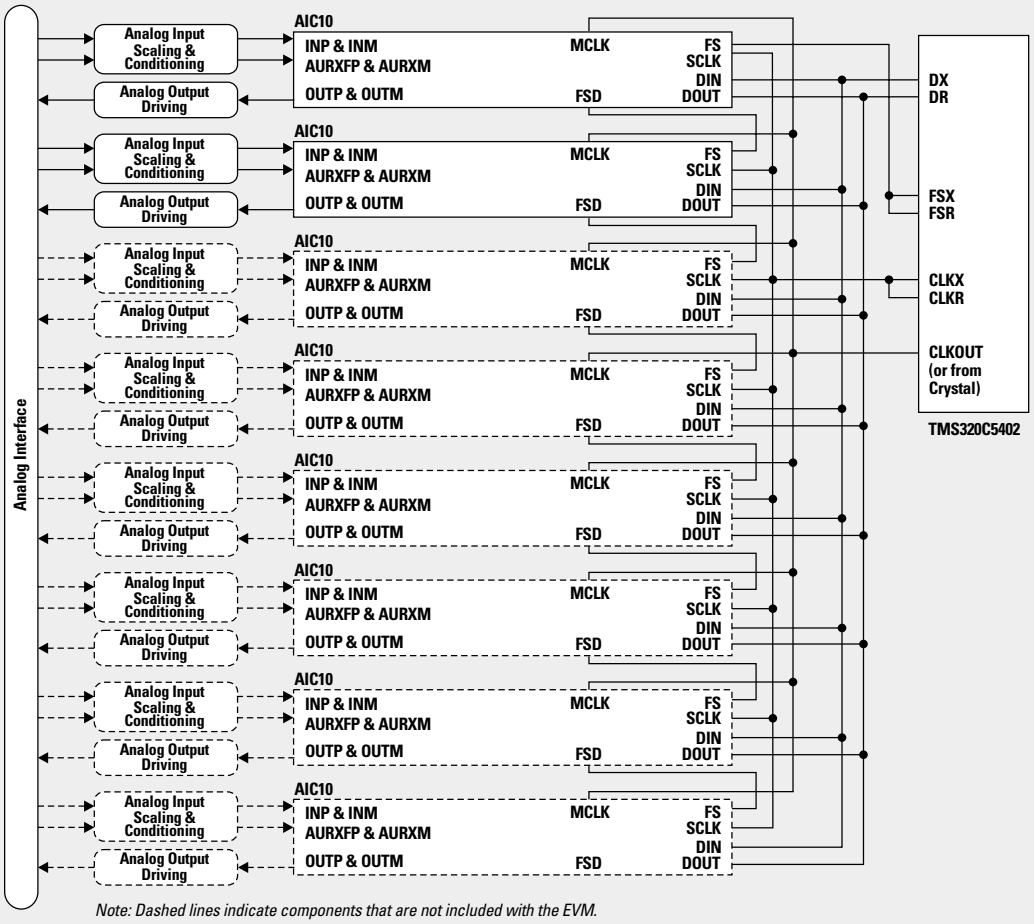
By Wendy X. Fang, *Application Specialist, Advanced Analog Products,*
and Perry Miller, *Application Specialist, Advanced Analog Products*

Introduction

The analog interface circuit (AIC), also called a modem Codec, is a complete data acquisition system on a chip for general-purpose telephony/speech applications such as: modem analog interface, voice-band audio processing, noise cancellation/suppression, hands-free communication, security voice systems, tone generation, echo cancellation, voice-over-internet protocol (VoIP), and industrial process control. The AIC is normally interfaced to a digital signal processor (DSP). This approach has a number of advantages and cost-saving benefits that cannot be realized with traditional Codec analog interfacing. The benefits include:

- lower cost,
- simple interface design and fewer components,
- greater system reliability due to fewer components,
- lower power consumption,
- higher performance, and
- high programmability.

Figure 1. Block diagram of the TLV320AIC10/11 EVM



Note: Dashed lines indicate components that are not included with the EVM.

The TLV320AIC10 is a high-resolution, high-speed device that contains both ADC/DAC data paths. The ADC data path includes signal conditioning op amps, a multiplexer, an anti-aliasing filter, a programmable gain amplifier, a Sigma-Delta ADC, and a decimation filter. The DAC data path is composed of a glueless DSP interface to an interpolation filter, a Sigma-Delta DAC, a low-pass reconstruction filter, a programmable gain amplifier, and a transmit amplifier.

An internal band-gap voltage reference is used to provide a stable V_{REF} both to the ADC and the DAC. The chip contains a clock divider circuit for dividing down the MCLK from the DSP or other clock source. Two analog inputs can be multiplexed to the ADC. In practice, more than one 'AIC10 is connected in parallel to form the multiple inputs/multiple outputs solution required for today's real-world telecommunication applications. Up to 8 TLV320AIC10 devices can be paralleled, in a cascade format, to communicate with a single DSP.

Figure 2. McBSP block diagram

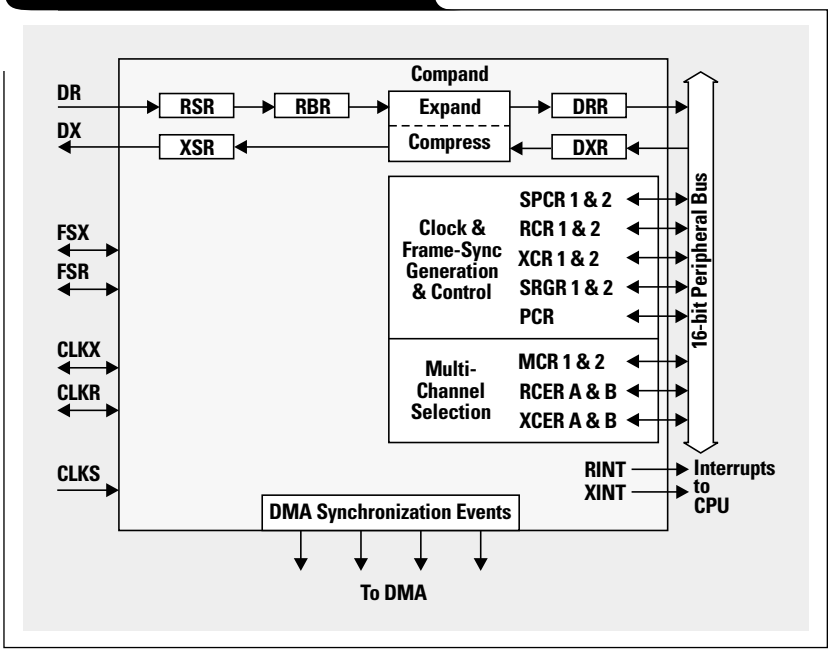


Figure 1 shows the block diagram of the TLV320AIC10/11 evaluation module (EVM), where a possible maximum of 16 analog inputs and 8 analog outputs could interface with a TMS320C54x DSP through 'AIC10s, providing a practical platform for various voice-band communication applications. There are many different working structures while multiple 'AIC10s work in parallel. In the one most widely applied, an 'AIC10 is assigned as the master and the rest of the 'AIC10 devices are assigned as slaves. Detailed information and various options are outlined in Reference 1.

The software program used to initialize and configure the AICs depends very much on the individual device hardware configuration and often needs to be modified for every hardware change or reconfiguration. Besides, human hardware configuration mistakes also can occur and affect the working reliability of the system.

In this article we present an algorithm that automatically identifies the number of on-board functional 'AIC10 devices and their positions (as a master or a slave) and indicates hardware configuring errors if they exist. Consequently, all control registers for the master and slave 'AIC10 devices are programmed automatically. With this algorithm, a faulty master AIC will *not* jeopardize the functioning of the whole system; and hardware reconfiguration or AIC master/slave reassignment will *not* require any software changes or rewriting. This "plug-and-play" software algorithm supports the TLV320AIC10/11 EVM for various customized applications, improving the DSP/'AIC10 system's reliability, flexibility, software reusability, and troubleshooting options.

McBSP and 'AIC10 interface

The algorithm developed in this article can be considered a generic "plug-and-play" communication method that handles the initialization and interface between a multichannel buffered serial port (McBSP) and a bank of TLV320AIC10 devices. Before the auto-identification and auto-configuration method is presented, a review of the McBSP and 'AIC10 interface is vital.

The multichannel buffered serial port

The McBSP is the full-duplex, multichannel buffered serial port in the TMS320C54x and C6x DSP families that allows direct interface among DSPs and between a DSP and other devices in a system, such as 'AIC10s.

A McBSP consists of 7 pins used to interface an external device (as shown in Figure 2):

Communication Data Lines

Data IN (from 'AIC10 to DSP):	DR (data receive)
Data OUT (from DSP to 'AIC10):	DX (data transmit)

Communication Clock and Control

DR Shift Clock:	CLKR
DX Shift Clock:	CLKX
DR Frame Sync:	FSR
DX Frame Sync:	FSX

McBSP System Clock

System Clock:	CLKS

A 16-bit external peripheral bus forms a bridge between the DSP's CPU and the McBSP. The triple-buffered DR and double-buffered DX can be read/written by the CPU. The CPU also reads the McBSP's status bits located in the serial port control registers, which are part of the sub-address register. See Reference 2 for more details.

'AIC10

The TLV320AIC10 is a general-purpose, 3- to 5.5-V, 16-bit, 22-ksps DSP Codec, mounted in a 48-pin surface-mount TFQP. The 'AIC10 contains signal conditioning op amps, filtering on both input and output, DSP interface to receive or transmit digital data to and from an external

Continued on next page

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host processor, programmable gain amplifier, an ADC, and a DAC. Figure 3 shows a simplified ’AIC10 block diagram.

The interface to the analog interface pins is defined as follows:

Analog Input #1
- Positive IN: INP
- Negative IN: INM

Analog Input #2
- Positive IN: AURXFP or AURXCP (if receive-path amplifier is used)
- Negative IN: AURXM

Analog Output
- Positive OUT: OUTP or DTXOP (if transmit-path amplifiers are used)
- Negative OUT: OUTM or DTXOM (if transmit-path amplifiers are used)

There are two digital pins on an ’AIC10 that can be considered as a pair of digital input/output ports:

- Digital IN: ALTIN
- Digital OUT: FLAG

For methods of interconnecting these analog and digital interface signals, please see References 1 and 3. This article concentrates on the software interface between DSP and ’AIC10. There are 11 pins provided on an ’AIC10 device to communicate with the C54x and C6x DSPs:

Main Communication Data Lines
- Data IN (from DSP to ’AIC10): DIN
- Data OUT (from ’AIC10 to DSP): DOUT

Communication Clock and Control
- Data Shift Clock: SCLK
- Frame Sync: FS
- Frame Sync Delay: FSD (output to next slave AIC as its FS)

Control Register Configuring
- Data IN: DCSI (direct configuration serial input)
- Hardware Secondary Comm Request: FC (force configuration)

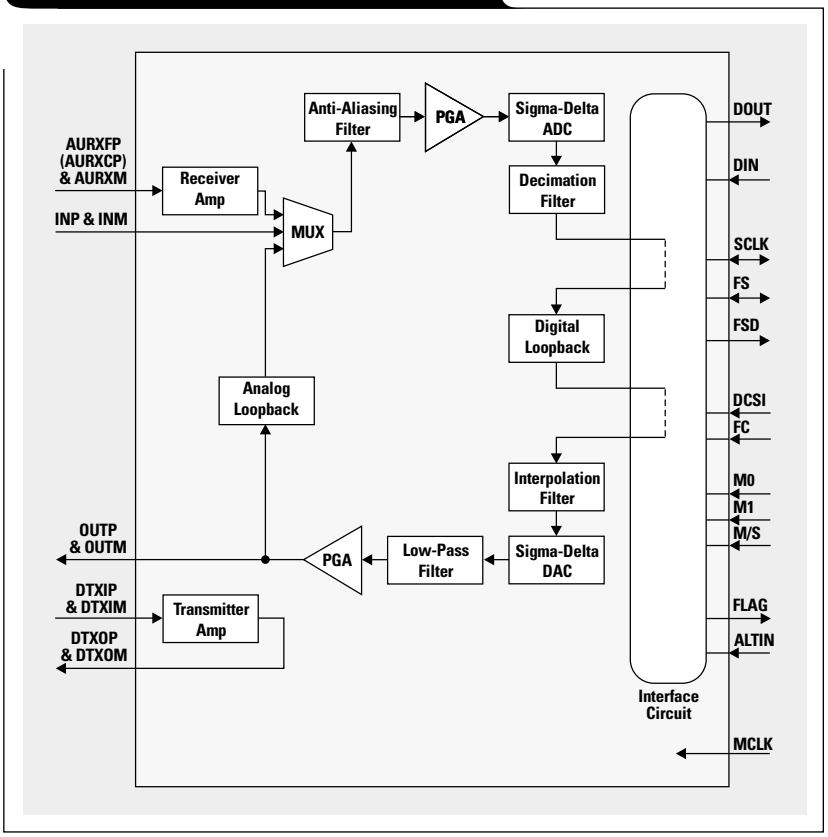
Communication Mode Setups
(configured by a jumper; will *not* change after power-up)
- Frame Sync (FS) Format: M0, M1
- Master/Slave Mode: M/S

AIC Device Master Clock
- Master Clock: MCLK

Each AIC device’s major link to the system DSP consists of 4 lines connected to its DIN, DOUT, SCLK, and FS pins, which are the hardware interface to the SPI port or the McBSP of a DSP.

Prior to power-up of the ’AIC10s, the communication mode is established by hardware configuration and usually involves setting a number of jumpers on the ’AIC10 EVM.

Figure 3. TLV320AIC10 block diagram



Interface

Figure 1 shows the hardware connection between the McBSP and the ’AIC10s. The MCLK at each ’AIC10 is connected to the same master clock source, such as a crystal or the CLKOUT pin of the system DSP. Each of the AICs is cascaded from its FSD pin to the next slave device FS pin. The master ’AIC10 generates SCLK that goes to the SCLK pins of all other ’AIC10s.

The McBSP and ’AIC10 communication data formats at primary (or ADC/DAC data) frame and secondary (or ’AIC10 control register configuring) frame are given in Figure 4. The primary communication always occurs, but the secondary one happens only if bit 0 is set in DIN (15-bit data mode) or by hardware pin FC in the ’AIC10 device.

The McBSP DR signal comes from multiple AIC DOUT sources, and the DX signal from the McBSP goes to multiple ’AIC10 devices (Figure 1). To ensure correct data to/from the right device, the DRs and DXs in McBSP must be delivered in the order that matches the number of ’AIC10s and the position of each. This synchronization procedure is illustrated in Figure 5 and is supported by proper software configuration according to ’AIC10 hardware. This software configuration is highly hardware-dependent; every ’AIC10 hardware change or reconfiguration can require the software to be changed or rewritten. Chiefly for this reason, the “plug-and-play” algorithm is necessary.

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Figure 4. Interface data format

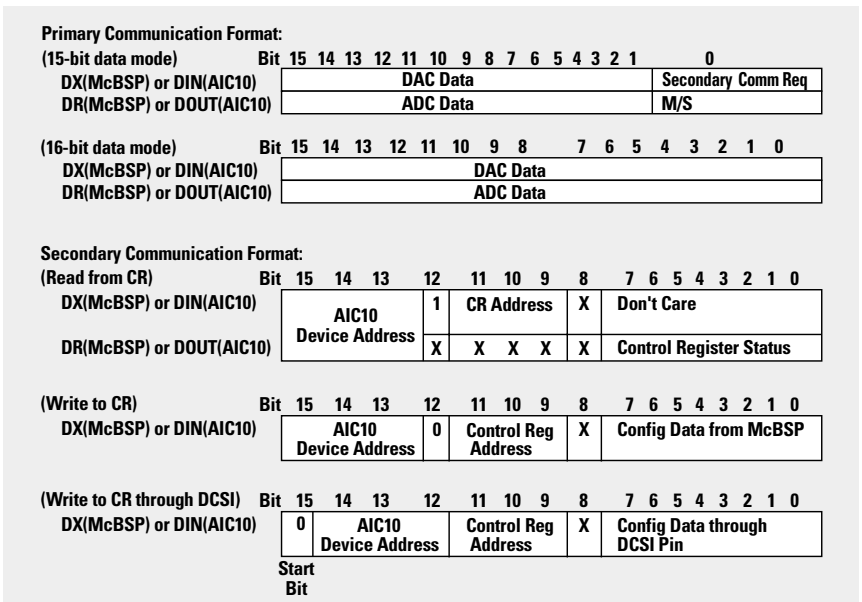
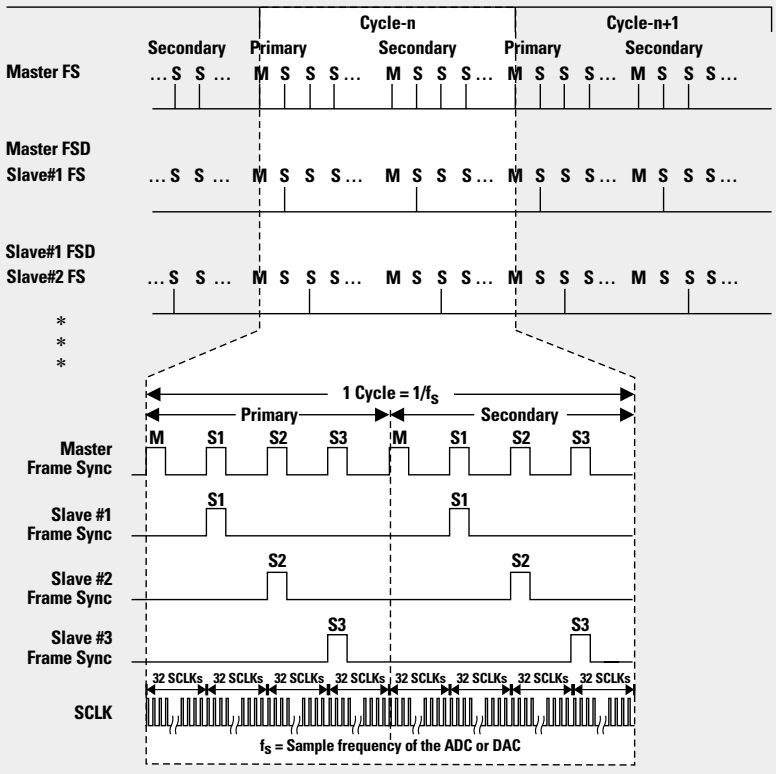


Figure 5. Paralleling 'AIC10 master/slave frame sync timing diagram



Notes:
1. In master FS there are 32 SCLKs between a master/slave frame and a slave/slave frame.
2. There are 256 (1 to 4 'AIC10s on board) or 512 (5 to 8 'AIC10s on board) SCLK pulses in each communication cycle (also called ADC/DAC sample interval), in which half (128 or 256) is for the primary phase and half is for the secondary phase.
3. The secondary communication phase occurs only if required in the primary one.

Continued from page 10

Algorithm

The developed algorithm consists of two phases: automatic 'AIC10 hardware identification, called auto-identification; and automatic 'AIC10 software initialization or configuration, called auto-configuration.

Auto-identification

A new routine is added to the normal software initialization procedure (see Figure 6) that automatically identifies the on-board 'AIC10 hardware configuration and supplies the following information:

- how many 'AIC10 devices are on-board;
- which device, if any, is configured as a master device; and
- whether there are any hardware configuration mistakes, such as the M/S pins of two 'AIC10s pulled high (more than one master is not allowed).

These configurations need to be known before the second phase, auto-configuration, can take place.

The new identification routine completes the following steps:

Step 1. At system power-up, all 'AIC10 control registers enter their default condition, which means that the interface data format is in 15-bit mode. At this stage the McBSP transmitter is *not* enabled to ensure that no secondary communication is requested. Only the receiver is enabled to read data from AIC devices.

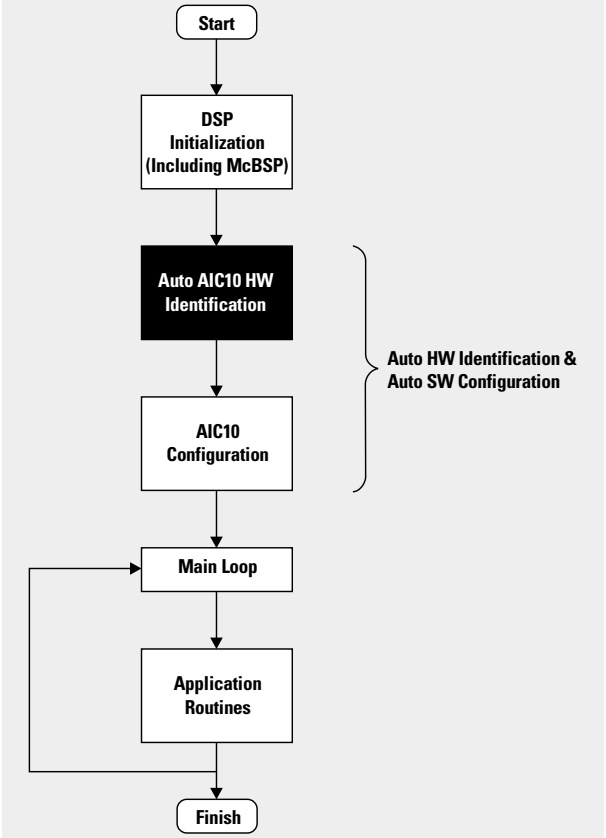
Step 2. To detect whether a master 'AIC10 is on board, the bit 0 of DR (called DOUT at 'AIC10) is checked for any data from a master 'AIC10 (refer to Figure 4).

Step 3. The communication frame number is counted before the first master 'AIC10 occurs. If the number is more than 8 (since a maximum of 8 'AIC10s can be paralleled in a system), a warning indication is displayed for "no master AIC devices."

Step 4. Otherwise, a master frame is detected at Step 3 before the frame counter reaches 8. Therefore, there is at least a master 'AIC10 on board, so the corresponding flag is set; for example, the MasterOnFlag.

Step 5. To identify the total number of 'AIC10s, the communication frames are counted, starting from the first time a master frame occcurs to the next master frame (refer to Figure 5). The result, named AIC10Num, is saved. The range of the number can be from 1 to 8.

Figure 6. Top-level flow chart of the main software routine with auto-identification



Otherwise the auto-identification failure flag (IdentFail) is set, a warning message is displayed, or an alarm sounds, aborting the system to reset condition.

Step 6. The system waits for AIC10Num-1 frames before enabling the McBSP transmitter to the starting point of the next primary communication, and checks whether bit 0 is logic "0" at each DR during the (AIC10Num-1) frames. If the check fails, the IdentFail flag is set, a warning message is displayed, and the system aborts to reset condition.

Step 7. The system repeats the secondary communication request AIC10Num times by writing 0x0001 to McBSP's DX register and transmitting. It also reads bit 0 at the first DR to make sure it is logic "1" (master). Otherwise, it sets the IdentFail flag, displays a warning message, and aborts to reset condition.

Step 8. Once the first secondary communication arrives, the system reads the control register (CR1) of the master device to set DX, reads the DR register on the DSP (masking out the 'AIC10's device address), and saves it to

Figure 7. Timing diagram of the auto-identification procedure

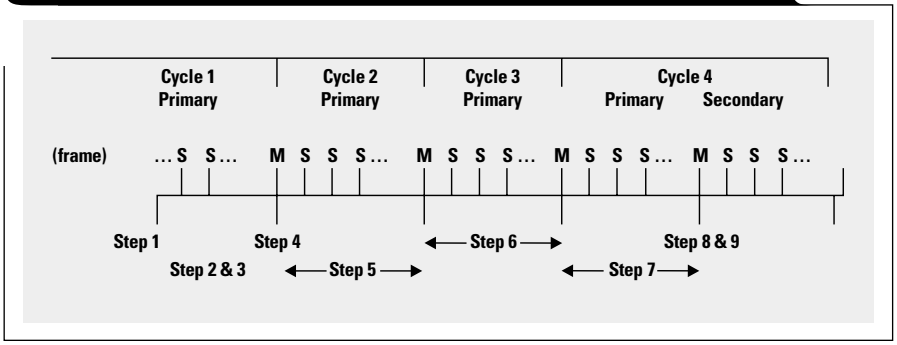
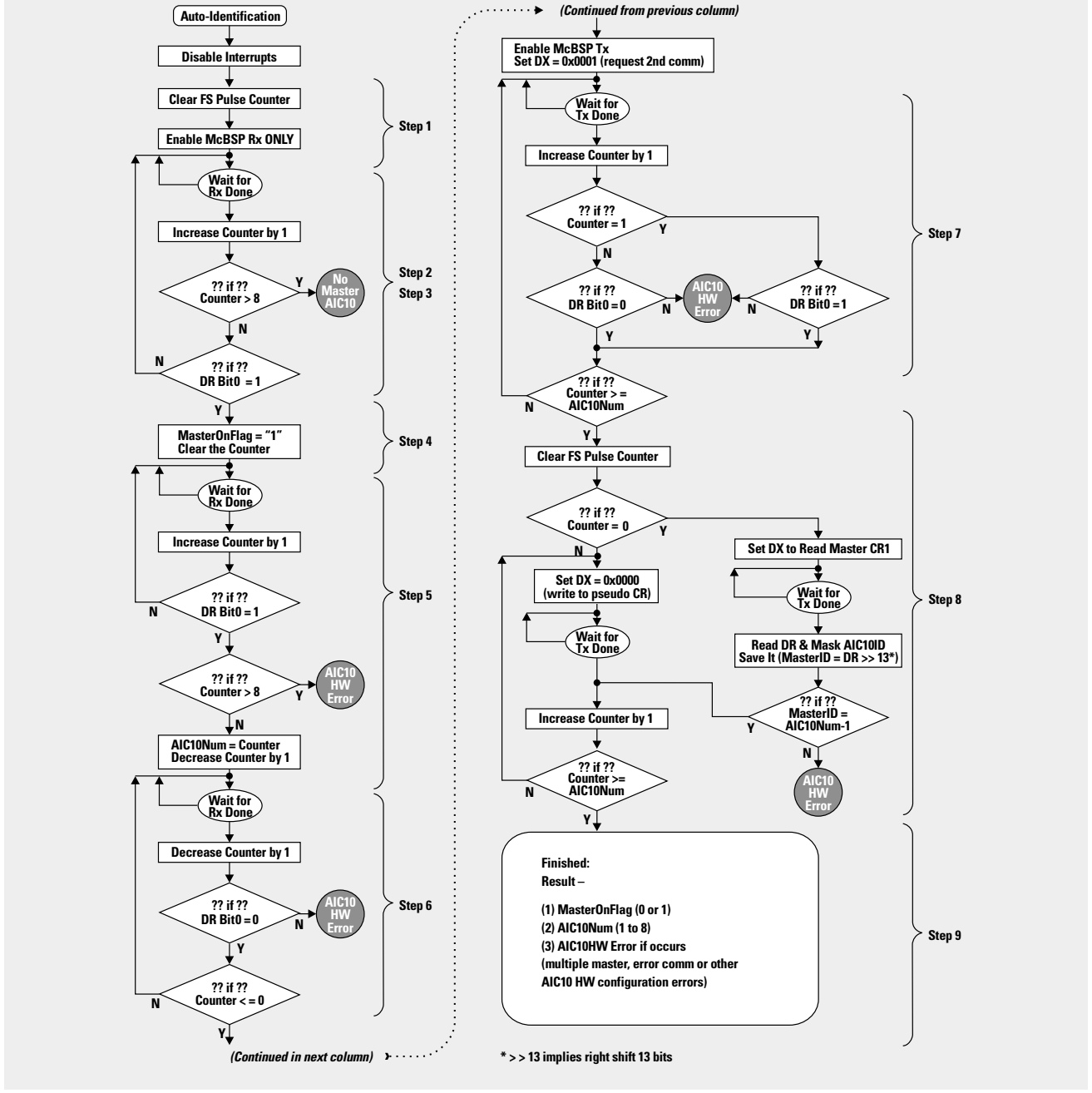


Figure 8. Automatic AIC hardware configuration and identification flow chart



MasterID. The MasterID is compared with AIC10Num-1. If they are not equal to each other, the IdentFail flag is set, an alarm sounds, and the system aborts to reset condition.

Step 9. The auto-identification of the hardware configuration is successfully completed. There is only one master 'AIC10 device on board (the IdentFail flag would be set if more than one master appeared), and there is a total of AIC10Num 'AIC10 devices.

Figure 7 shows the full timing diagram of the auto-identification procedure and indicates the task at each of the time intervals. It takes a maximum of 4 communication cycles to finish the auto-identification procedure. There are 256 (if there are 4 or less 'AIC10s) or 516 (if there are 5 to 8 'AIC10s) SCLKs within a communication cycle, and there are 32 SCLKs between each frame as illustrated in Figure 5.

The new auto-identification algorithm can be implemented by coding according to the flow chart in Figure 8.

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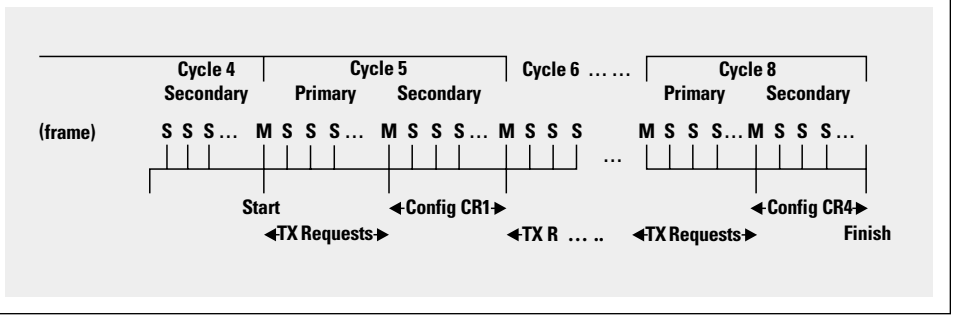
Auto-configuration

After the AIC hardware configuration is identified and the software establishes the number of 'AIC10s on board and that there is only one master, then the auto-configuration (software configuration) of the AIC control registers becomes a trivial task. Note that there are 4 control registers in an 'AIC10 device. Hence, 4 complete communication cycles are needed for the configuration. Each of the cycles includes a primary communication phase, which transmits the secondary communication requests; and a secondary communication phase, which programs the 'AIC10's control registers. Figure 9 shows the timing diagram of the auto-configuration that follows the auto-identification procedure.

Figure 9. Timing diagram for the auto-configuration procedure



Conclusion

This article presented a "plug-and-play" algorithm that uses the McBSP on the TMS320C5402 DSP to identify automatically the TLV320AIC10 EVM master/slave structure and the number of on-board TLV320AIC10 analog devices. The software automatically configures the 'AIC10s to initiate stable communication between the McBSP and 'AIC10s. The algorithm offers TLV320AIC10 users a handy and powerful tool for their applications.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. TLV320AIC10/11 EVM User's Guide	slwu003
2. *TMS320C54x DSP Reference Set*, Vol. 5: *Enhanced Peripherals*, Section 2	spru302
3. TLV320AIC10 Data Manual	slws093

Related Web sites

www.dataconverter.com

www.ti.com/sc/docs/products/analog/tlv320aic10.html

www.ti.com/sc/docs/products/dsp/index.htm

Using quad and octal ADCs in SPI mode

By Tom Hendrick
Data Acquisition Applications—Dallas

Introduction

This article describes the steps required to interface a microprocessor-based system using a serial peripheral interface (SPI) port of the quad and octal family of serial analog-to-digital converters (ADCs) listed in Table 1.

Table 1. TI ADC features

DEVICE	CHANNELS	SUPPLY VOLTAGE (V)	RESOLUTION (bits)	INTERNAL CONVERSION CLOCK
TLV1504	4	2.7 to 5.5	10	Yes
TLV1508	4	2.7 to 5.5	10	Yes
TLV1544	4	2.7 to 5.5	10	Yes
TLV1548	8	2.7 to 5.5	10	Yes
TLV2544	4	2.7 to 5.5	12	Yes
TLV2548	8	2.7 to 5.5	12	Yes
TLC1514	4	5.0	10	No
TLC1518	8	5.0	10	No
TLC2554	4	5.0	12	No
TLC2558	8	5.0	12	No

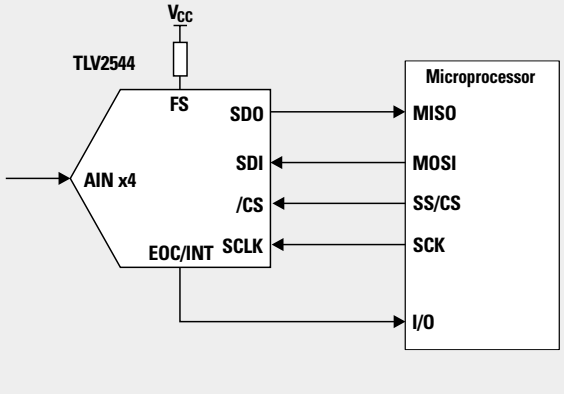
Serial ADC interface

Serial communication with this family of devices is accomplished through three serial inputs and a tri-state serial output: chip select (/CS), serial input clock (SCLK), serial data input (SDI), and serial data output (SDO). These 4 pins provide a direct 4-wire interface to most microprocessors. Figure 1 shows a typical ADC-to-microprocessor interface.

Frame sync and EOC/INT

A frame sync (FS) pin is provided for a typical DSP interface and is normally tied high when used in microprocessor applications. This family of devices also features a programmable end-of-conversion/interrupt (EOC/INT) pin. When programmed as EOC, the output goes from a high to low state at the falling edge of the 16th clock, indicating that the sampling process has been completed. EOC returns to a high state upon the completion of the conversion process. When programmed as /INT, it can act as an interrupt to the host processor. /INT goes from a high to low state at the end of the conversion process and is cleared automatically on the following /CS falling edge.

Figure 1. Four-wire microprocessor interface



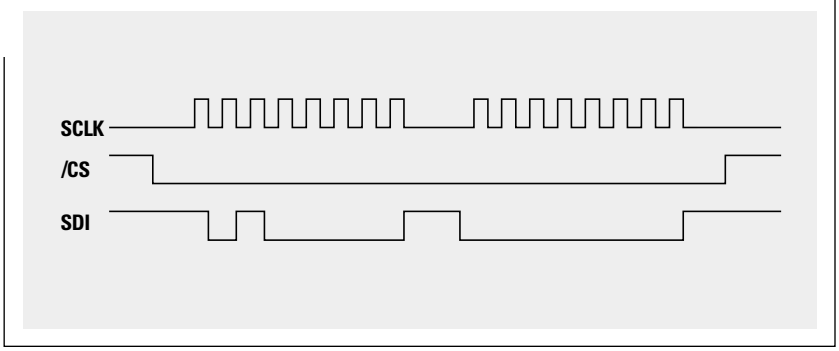
ADC read and write cycles

Many microprocessors offer an SPI port that transmits and receives data in 8-bit packets. The ADCs, however, use a 16-bit data string for configuration and provide serial data output in a 16-bit format.

Configuring the ADC requires the microprocessor to issue back-to-back data transfers while holding the SS/CS line low. The processor's transmit buffer is loaded first with the upper byte of configuration data, sending the SS/CS line low and starting the SCLK, which transmits the serial data to the ADC. The processor's SPI interrupt flag is then cleared, the transmit buffer is loaded with the lower byte of configuration data, and the transfer process begins again. Figure 2 shows the host mode configuration cycle (write 0xA000 to ADC).

The same sequence could be used to read the contents of the configuration register or the contents of the FIFO. The serial data output would simply be configured to perform the requested read operation (write 0x9000 or 0xE000).

Figure 2. The host mode configuration cycle



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ADC sample and convert cycles

Each sample/convert cycle requires the user to issue a valid channel select command in the upper nibble of the SDI string. The valid channel selection codes consist of the hex values 0x0000 through 0x9000. FIFO Read (0xE000) will also allow a conversion cycle to take place.

Hex commands 0xA000 through 0xD000 and 0xF000 are reserved for access to the configuration register and internal test modes. More information about these commands can be found in the respective device data sheets listed under References at the end of this article.

Another factor to consider when using these devices in the microprocessor mode is the sample and conversion time. When the TLV2544 is operated in short sampling with the internal conversion clock, for instance, sampling is not complete until the 16th falling edge of SCLK (see Figure 3). Another 3.5 µs are required for the conversion to take place. If chip select is asserted low before the conversion cycle is complete (EOC going Hi), the current conversion data will be lost.

If the microprocessor is set to clock polarity = 1 and clock phase = 1 as shown in Figure 4, the ADC requires the user to issue a third, or "null data," transfer to the SPI port. Since the ADC samples, converts, and shifts data out on the rising edge of the clock, the first falling edge is ignored. As shown in Figure 4, the EOC signal appears on the 16th falling clock edge after the *first* rising. The length of conversion time and number of dummy write transfers the processor has to make is dependent upon the mode in which the ADC is being used, and the clock phase and polarity settings of the SPI port.

The TLC series of devices does not contain an internal conversion clock and depends on SCLK throughout the entire sample/conversion process. This requires that additional "null data" SPI transfers be conducted. The total number of clock cycles is dependent upon the operating mode of the ADC being used. The TLC2544 (in single-shot mode), for example, would require 16 clocks for channel selection and sampling, plus an additional 16 clocks for conversion. A minimum of four 8-bit SPI blocks would be needed.

Figure 3. Sample/convert cycle

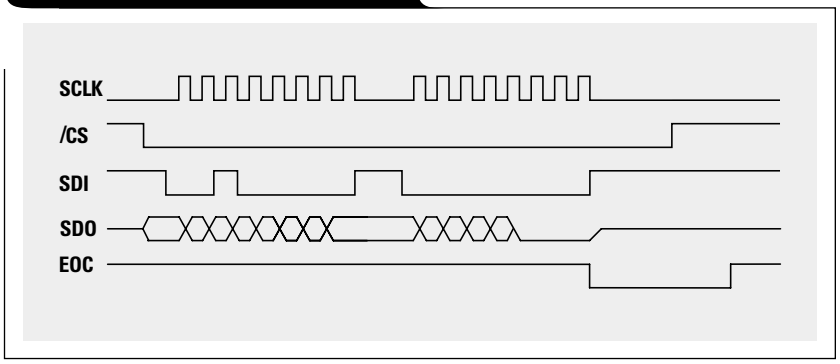
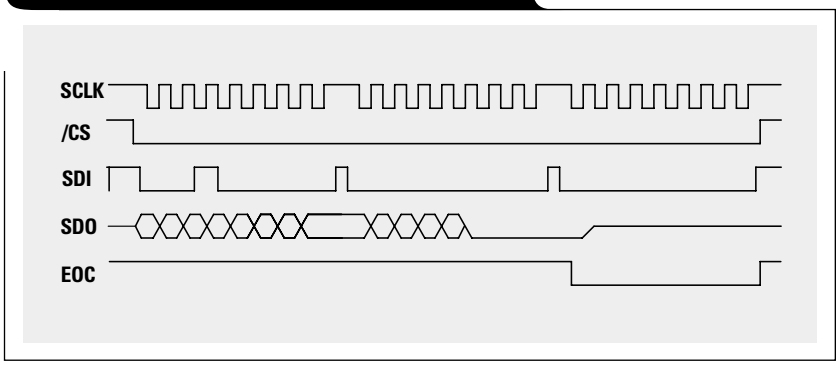


Figure 4. Alternate sample/convert cycle



Reading valid data

The serial data out from these devices is pre-released by 1/2 clock cycle, plus a delay. What this means is that while valid output data is available on the rising edge of SCLK, the rising edge also triggers the shifting out of the next data bit. With low clock speeds, it may appear as if data is changing when it should be valid. A processor's setup and hold time requirements may affect its ability to read correctly the data presented by the converter. Figures 5 and 6 show the relationship between SCLK, SDO, and SDI with a 4-MHz and 20-MHz clock, respectively.

The code example at the bottom of the next page was written for the Motorola 68HC912 and was assembled using ASM12.EXE. The code samples and stores data from channel 0 of a TLV2544.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. TLV1504/1508/1544/2544/2548, TLC1514/1518/2554/2558 10-Bit and 12-Bit ADC EVM User's Guide	slau029
2. TLV1504,TLV1508 Data Sheet	slas251
3. TLV1544,TLV1548 Data Sheet	slas139
4. TLV2544, TLV2548 Data Sheet	slas198
5. TLC1514,TLC1518 Data Sheet	slas252
6. TLC2554,TLC2558 Data Sheet	slas220

Related Web sites

www.dataconverter.com

www.ti.com/sc/docs/products/analog/*device***.html**
Replace *device* with tlc1514, tlc1518, tlc2554, tlc2558, tlv1504, tlv1508, tlv1544, tlv2544, or tlv2548

Figure 5. SCLK = 4 MHz

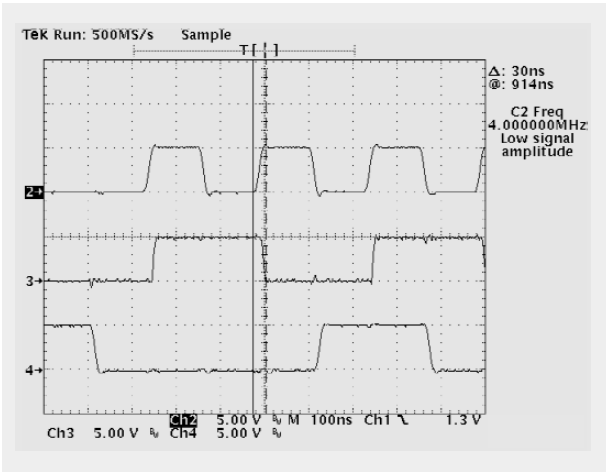
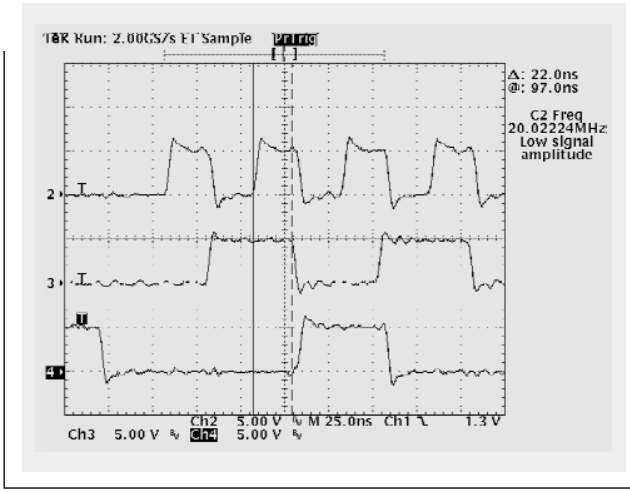


Figure 6. SCLK = 20 MHz



Code example

```
; SPI program using the 68HC912 uP and a TLV2544 ADC with Frame Sync hi via SP3
;* ------------------------------------------------;
;*             Equates and Variables
;* ------------------------------------------------

SP0CR1:     equ $D0      ;SPI 0 Control Register 1
SP0CR2:     equ $D1      ;SPI 0 Control Register 2
SP0BR:      equ $D2      ;SPI 0 Baud Rate Register
SP0SR:      equ $D3      ;SPI 0 Status Register
SP0DR:      equ $D5      ;SPI 0 Data Register
PORTS:      equ $D6      ;Port S Data Register
DDRS:       equ $D7      ;Port S Data Direction Register

; User Variables

Upper_Byte: EQU $0B00
Lower_Byte: EQU $0B01
Upper_CFIG: EQU $0B02
Lower_CFIG: EQU $0B03
;* ------------------------------------------------
;*             MAIN PROGRAM
;* ------------------------------------------------
       ORG      $0800    ; User code data area,
                         ; start main program at $0800
DATA   FCB      00,01    ; Set up 16 bit Output DATA
MAIN:
       BSR      INIT     ; Subroutine to initialize SPI registers
       JSR      SAMPLE   ; Subroutine to start transmission
;* ------------------------------------------------
;*             Initialization Subroutine
;* ------------------------------------------------
```

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Code example (Continued)

```
INIT:
       BSET DDRS, #%11101100    ; Configure PORT S input/ouput:
                                ; SS/CS, SCK, MOSI, MISO, PS3, PS2, TXD, RXD
       BSET SP0BR, #$00         ; Set Baud Rate
       MOVB #$50, SP0CR1        ; Configure SPI(SP0CR1)
                                ; SPIE, SPE, SWOM, MSTR, CPOL, CPHA, SSOE, LSBF
       MOVB #$00, SP0CR2        ; Configure SPI(SP0CR2):
                                ; -,-,-,-,-,-,SSWAI, SPCO
       MOVB #$88, PORTS         ; Sets ADC CS Hi, FS Hi
       BCLR PORTS, #%10000000   ; Select ADC
                                ; Configure ADC
       MOVB #$A0, Upper_CFIG    ; Write 0xA000 to set up Host Communication.
       MOVB Upper_CFIG, SP0DR   ; Put data in XMIT Buffer
       JSR FLAG                 ; Clear SPI Flag
       MOVB #$04, Lower_CFIG    ; Select EOC Mode
       MOVB Lower_CFIG, SP0DR   ;
       JSR FLAG                 ; Clear SPI Flag
       BSET PORTS, #$80         ; Sets ADC CS Hi
       MOVB #$00, UPPER_BYTE    ; Set initial values
       MOVB #$00, LOWER_BYTE    ; Set initial values
       RTS
;* ————————————————————-
;*     Sample / Convert
;* ————————————————————-
SAMPLE:
       MOVB #$08, PORTS         ; Sets ADC CS Low
       MOVB #$20, SP0DR         ; Tell ADC what channel to read and generate SCLK for ADC
       JSR FLAG                 ; Clear SPI Flag
                                ; Store received data
       LDAA SP0DR               ; Load first ADC Sample
       MOVB #$00, SP0DR         ; Write zero value to data register to generate SCLK for ADC
       JSR FLAG                 ; Clear SPI Flag
       LDAB SP0DR               ; Load second ADC Sample
       STD DATA                 ; Store ACCA and ACCB in Data

       nop                      ; Extra time for conversion nop
       MOVB #$88, PORTS         ; Sets ADC CS Lo
       JMP SAMPLE               ; Go back and do it again

;* ————————————————————-
;*         Clear SPI Flag Subroutine
;* ————————————————————-

FLAG:  BRCLR   SP0SR,#$80,FLAG  ; Wait for flag.
       RTS
.end
```

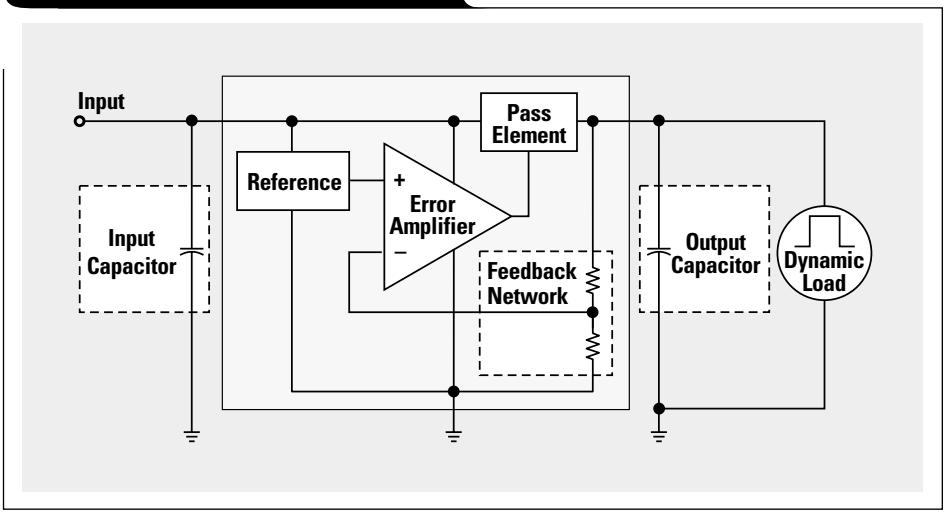
Understanding the load-transient response of LDOs

By Brian M. King
Advanced Analog Products

Introduction

Low-dropout linear regulators (LDOs) are commonly used to provide power to low-voltage digital circuits, where point-of-load regulation is important. In these applications, it is common for the digital circuit to have several different modes of operation. As the digital circuit switches from one mode of operation to another, the load demand on the LDO can change quickly. This quick change of load results in a temporary glitch of the LDO output voltage. Most digital circuits do not react favorably to large voltage transients. For the digital circuit designer, minimizing an LDO's transient response is an important task.

Figure 1. Typical LDO components



LDOs are available in a wide variety of output voltages and current capacities. Some LDOs are tailored to applications where a good response to a fast transient is important. The TPS751xx, TPS752xx, TPS753xx, and TPS754xx families of LDOs from Texas Instruments are examples of fast-transient-response LDOs. The TPS751xx and TPS753xx families are rated at 1.5 A of output current, while the TPS752xx and TPS754xx families can provide up to 2 A. All four families use PMOS pass elements to provide a low dropout voltage and low ground current. These devices come in a PowerPAD™ package that provides an effective way of managing the power dissipation in a TSSOP footprint.

Figure 1 shows the circuit elements of a typical LDO application. The main components within a monolithic LDO include a pass element, precision reference, feedback network, and error amplifier. The input and output capacitors are usually the only key elements of the LDO that are not contained in a monolithic LDO. There are a number of factors that affect the response of an LDO circuit to a load transient. These factors include the internal compensation of the LDO, the amount of output capacitance, and the parasitics of the output capacitor.

LDO compensation

The primary feedback loop of the LDO, consisting of the output capacitor, feedback network, error amplifier, and pass element, determines the LDO's frequency response. The unity gain crossover frequency and stability of the LDO circuit affect the overall transient response of the LDO.

The crossover frequency affects the settling time of the linear regulator circuit, where the settling time is the time elapsed from the initial onset of the load transient to the time where the output voltage returns to within a few percent of a steady-state value. A higher crossover frequency will decrease the duration of a transient condition. In most LDOs, the output capacitor and its associated equivalent series resistance (ESR) form a dominant pole in the loop response. Although larger output capacitors tend to decrease the magnitude of the transient response, they also tend to increase the settling time.

The stability of an LDO circuit can be assessed from the gain and phase margins of the loop response. A stable regulator will respond to a transient in a smooth, controlled manner, while an unstable or quasi-stable regulator will produce a more oscillatory transient response. Since the internal compensation of an LDO is fixed, only the output capacitor can be adjusted to insure stability. To assist in the proper selection of an output capacitor, LDO manufacturers typically provide limits on the acceptable values of capacitance and ESR.

Continued on next page

This article was adapted from "Optimized LDO Response to Load Transients Requires the Appropriate Output Capacitor and Device Performance" by Brian King in the September 2000 issue of *PCIM Power Electronics Systems* by permission of Primedia's Intertec Publishing Group.

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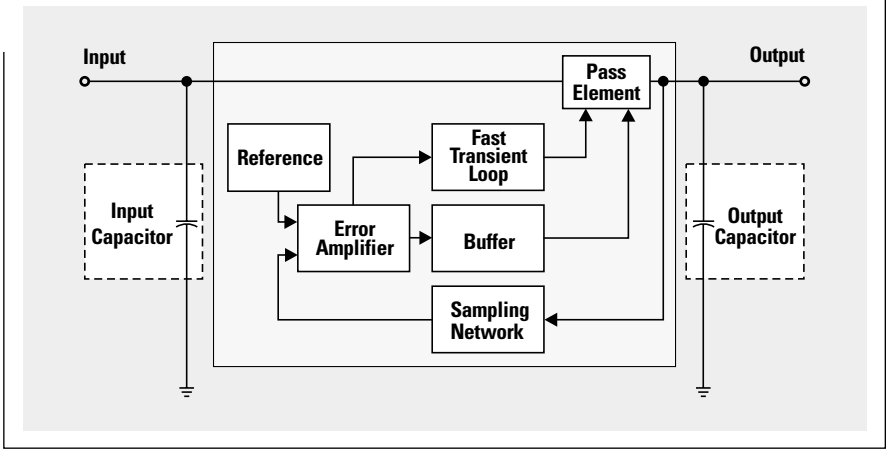
In addition to the main feedback loop, some LDOs contain a second feedback loop that allows the LDO to respond faster to large-output transients. This fast-transient loop basically bypasses the error amplifier stage and drives the pass element directly. A symbolic representation of an LDO with this secondary compensation is shown in Figure 2. By responding faster than the error amplifier compensation, LDOs that contain this loop are better able to minimize the effects of a load transient. The TPS751xx, TPS752xx, TPS753xx, and TPS754xx families of LDOs from Texas Instruments are examples of devices that contain this secondary loop.

Figure 2. LDO with secondary loop for fast-transient response



Figures 3 and 4 show the transient response of a TPS75433 with a 100-µF, 55-mΩ output capacitor to different load transients. The transient in Figure 3 transitions from no load to 250 mA, while the transient in Figure 4 steps from no load to 2 A. The 250-mA-load transient is not large enough to trigger the secondary loop. However, the response of the secondary feedback loop is clearly visible in the LDO response to the 2-A transient. If the secondary loop were not present, the voltage drop in Figure 4 would be much more severe.

Output capacitor

Since the LDO cannot respond instantaneously to a transient condition, there is some inherent delay time before the current through the pass element can be adjusted to accommodate the increased load current. During this delay time, the output capacitor is left to supply the entire transient current. Because of this, the amount of output capacitance and its associated parasitic elements greatly impact the transient response of the LDO circuit.

The equivalent model of a typical capacitor is shown in Figure 5. All capacitors have an equivalent series resistance (ESR) and an equivalent series inductance (ESL). A number of factors affect the ESR and ESL values, such as the package type, case size, dielectric material, temperature, and frequency. The amount of capacitance, ESR, and ESL each affect the transient response in a different way.

To demonstrate the effects of the parasitics of the output capacitor, a test circuit was built by using a TPS75433 and an adjustable output capacitor model. The capacitor model was built using discrete components to model the ESL, ESR, and capacitance so that the effects of each parasitic element could be evaluated independently. Small valued air-core inductors were used to model the ESL. Low-inductance metal film resistors were used to model the ESR. The capacitance was modeled by combining multiple 10-µF ceramic capacitors in parallel. The low ESL and low ESR of the ceramic capacitors make them good models of an ideal capacitor.

Figure 3. TPS75433 response to a 250-mA-load transient

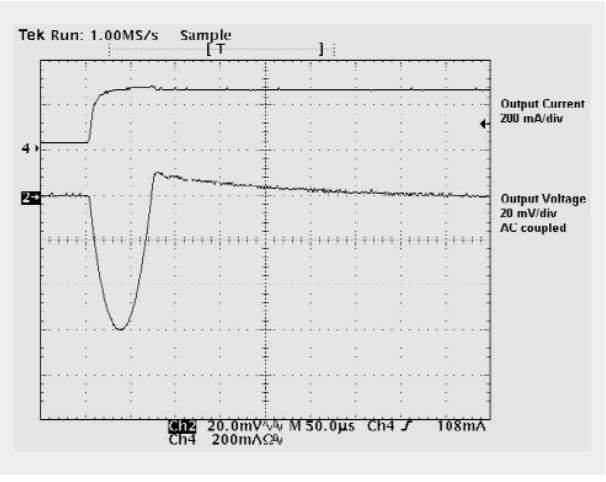
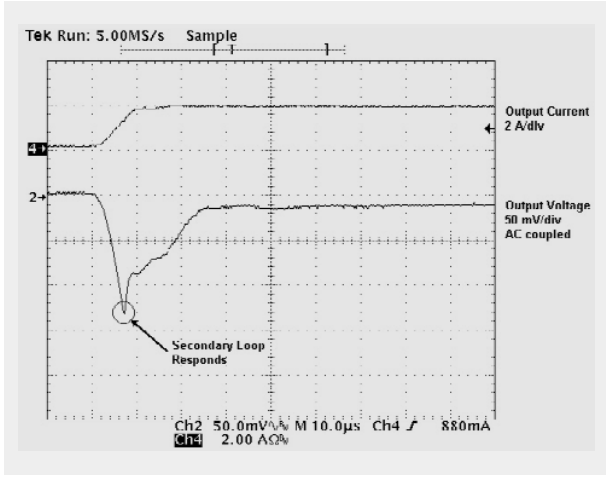


Figure 4. TPS75433 response to a 2-A-load transient



Equivalent series inductance

When a load transient occurs, the first factor that comes into play is the ESL. The transient response of various amounts of ESL is shown in Figure 6. The voltage across the ESL is equal to the product of the inductance and the rate of change of current. Initially, the ESL voltage is zero. During the rising edge of the current, a negative potential will appear across the ESL. Once the transient has reached its final value, the voltage across the ESL will return to zero. The net result is a negative voltage spike whose width is determined by the rise time of the transient and whose magnitude is determined by the slew rate of the transient step and the ESL value. The ESL value of capacitors is quite small. However, as the rate of change in current increases, the ESL-induced voltage may become bothersome. For this reason, it is a good idea to consider the ESL when selecting a capacitor for a fast-switching application, particularly if the load is sensitive to voltage spikes.

Since the parasitic inductance of PWB traces will add in series with the ESL, a good layout is key to minimizing the effects of ESL. The inductance of a trace is dependent upon the geometry of the layout. However, as a general rule, 10 nH to 15 nH are added for every inch of trace. Ideally, the input and output capacitors should be located as close as possible to the LDO. In addition, the entire LDO circuit should be located as close as possible to the load. Using planes for the LDO output and its return will also help to reduce the stray inductance.

Equivalent series resistance

The voltage across the ESR of a capacitor also adds to the transient response. The voltage across various amounts of ESR is shown in Figure 7. The ESR voltage is equal to the product of the capacitor current and the resistance. Before the transient, while there is no current flowing in the capacitor, the ESR voltage is zero. As the output capacitor begins to supply the transient current, the ESR voltage ramps down proportionally to the rise in load current. The voltage across the ESR remains at a steady value until the LDO begins to respond to the transient condition. After the LDO has responded to the transient, the entire load current is again supplied by the LDO, and the voltage drop across the ESR returns to zero. The resulting response is a negative pulse of voltage. The magnitude of the load transient and the amount of series resistance determine the magnitude of the ESR voltage pulse. The period of the voltage pulse is determined by the response time of the LDO and is significantly longer than the period of the ESL voltage spike. Because of the integrating nature of the LDO error amplifier, the LDO responds faster to larger dips in output voltage. Basically, a larger dip in output voltage generates a larger differential error voltage that causes the error amplifier to drive the pass element harder. Consequently, the LDO responds faster to larger voltage drops caused by larger ESR values. As a result, the period of the ESR-induced voltage droop decreases as the amount of ESR increases. From a transient point of view, it is desirable to minimize the amount of ESR. However, since the ESR and output capacitance form a dominant pole in the compensation of most LDOs, some finite amount of ESR is usually required to guarantee stability of the LDO.

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Figure 5. Equivalent capacitor model

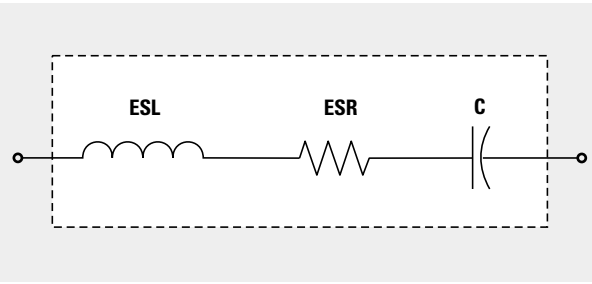


Figure 6. ESL load-transient response

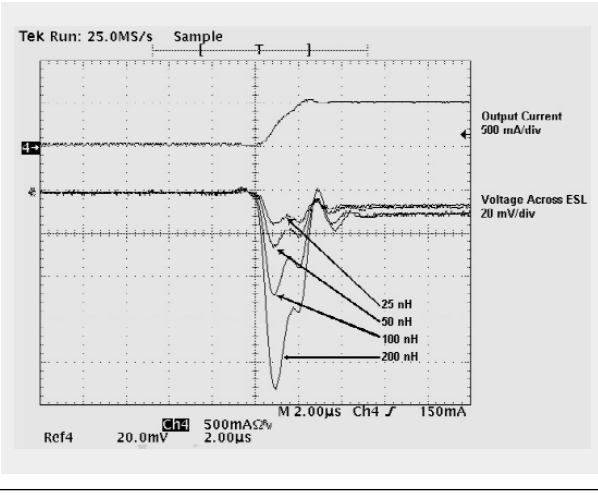
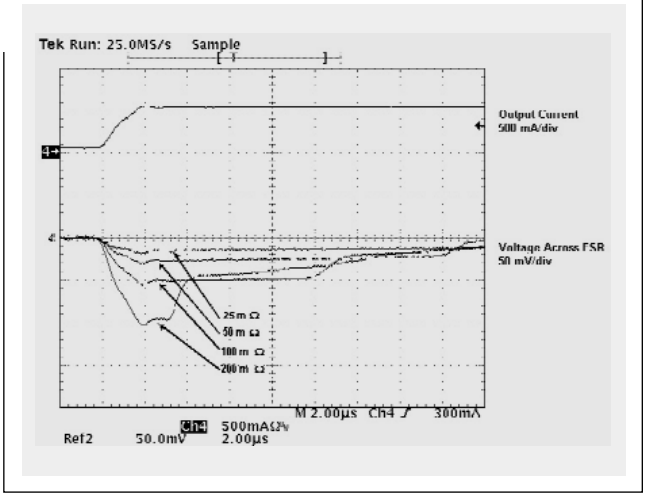


Figure 7. ESR load-transient response



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Bulk capacitance

The voltage across the actual output capacitance begins to decay as the capacitor supplies current to the transient load. The transient response of various amounts of output capacitance is shown in Figure 8. The rate of change of capacitor voltage is equal to the transient current divided by the capacitance. While the load is at its new value, the capacitor voltage decays at a constant rate until the LDO begins to respond. The larger voltage dip associated with a smaller capacitance value produces a larger error signal at the input of the error amplifier that causes the LDO to respond faster. Consequently, as the output capacitance is increased, the magnitude of the voltage dip decreases, while the period of the voltage dip increases. In order to minimize the output voltage dip, the amount of bulk capacitance must be increased.

The combined effect of the capacitance, ESL, and ESR is shown in Figure 9. In Figure 9, the capacitor consists of 200 µF of capacitance, 33 mΩ of ESR, and 100 nH of ESL. The actual response of a given capacitor will vary depending on the relative values of the ESR, ESL, and capacitance. The initial voltage spike during the rising slope of transient load will be less pronounced for capacitors with lower ESL values. Similarly, the voltage offset caused by the ESR will be smaller for smaller values of ESR, and the output voltage droop will be smaller for larger values of capacitance.

Capacitor technology

Although there are many types of capacitors, there are three that are most commonly used in LDO applications. These capacitor types include ceramic, aluminum electrolytic, and tantalum.

Ceramic capacitors offer a compact size, low cost, and very low ESR and ESL. Until recently, ceramics were limited to about 4.7 µF maximum. However, ceramics up to 22 µF recently have been introduced to the market. In situations where the low ESR of ceramics becomes a stability problem for the LDO, a low-value external resistor can be added in series with the capacitor.

Aluminum electrolytic capacitors are available in a wide range of capacitance values and case sizes. Because the loss of electrolyte over time limits the useful life of aluminum electrolytics, reliability can be a concern. The ESR of aluminum electrolytic capacitors is much higher than that of ceramic capacitors, but it decreases substantially as the voltage rating increases. In addition, aluminum electrolytic capacitors typically have more ESL than either ceramic or tantalum capacitors. However, the ESL of aluminum electrolytic capacitors usually is not large enough to cause concern. While the footprint areas of surface-mount electrolytics are comparable to ceramics, they tend to have taller profiles than their ceramic counterparts. However, since most LDO applications require a large amount of capacitance (more than 4.7 µF), aluminum electrolytics offer an attractive solution.

Tantalum capacitors offer a large capacitance in a compact size. The low ESR values of tantalums are well suited to LDO applications. The ESL of tantalum capacitors usually is higher than that of ceramic capacitors but less than that of aluminum electrolytic capacitors. As with aluminum electrolytic capacitors, the ESL usually is small enough not to cause concern in LDO applications. Most tantalum capacitors have an unsafe failure mode, which dictates that their operating voltage should be substantially less than their rated voltage (usually less than 50%.) Although tantalum capacitors are well suited to LDO applications, their popularity has skyrocketed in recent years, reducing availability and raising cost.

Design example

Consider a 3.3-V application that must be able to supply a load transient that transitions from no load to 1 A in 2 µs. Assume that the specifications do not allow the output voltage to drop below 3.0 V under any transient condition. First, an LDO must be selected that the designer feels can handle the output requirements. Given the high load rating and the transient requirements, a TPS75333 may be used, which provides 3.3 V at up to 1.5 A. From the TPS75333 data sheet, it can be seen that the minimum guaranteed output voltage is 3.234 V. Subtracting the 3.0-V output

Figure 8. Capacitance load-transient response

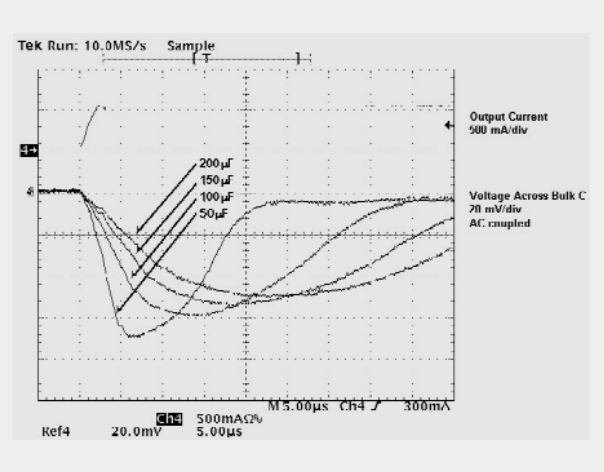
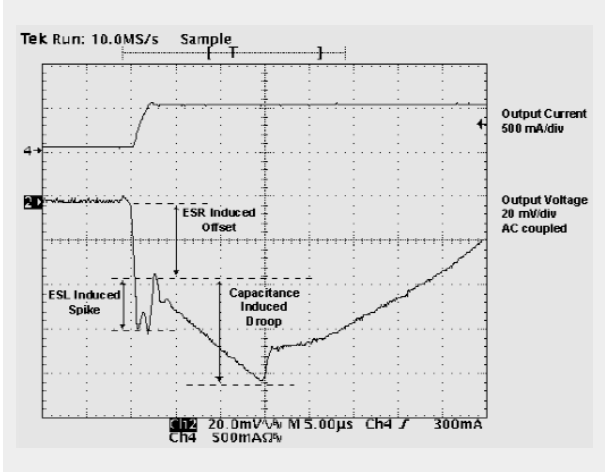


Figure 9. Total capacitor response



requirement from the minimum LDO voltage allows 234 mV for the transient.

Next, an output capacitor must be selected that, in conjunction with the TPS75333, will keep the output at an acceptable level. First, the ESL requirement must be checked. The maximum allowable ESL can be calculated as follows:

$$ESL_{max} = V_{dip,max} \times \frac{\Delta t_1}{\Delta I} = 234\,mV \times \frac{2\,\mu s}{1\,A} = 466\,nH, \quad \textbf{(1)}$$

where $V_{dip, max}$ is the maximum allowable voltage dip, Δt_1 is the current rise time, and ΔI is the stepped load change. In this example, as in most situations, the maximum allowable ESL is quite large and will not impact the capacitor selection.

Next, assume that the response time of the TPS75333 is going to be around 5 µs. Since LDO response times vary based on the ESR, capacitance, and the magnitude of the transient, this information typically is not published in the data sheets. Consequently, this assumption must be based on the evaluation or prior knowledge of the part. Having made this assumption, the voltage droop can be calculated for different capacitance values. The droop associated with the capacitance is given by

$$\Delta V_C = \frac{\Delta I \times \Delta t_2}{C} = \frac{1\,A \times 5\,\mu s}{100\,\mu F} = 50\,mV, \quad \textbf{(2)}$$

where C is the output capacitance and Δt_2 is the response time of the LDO. Assuming that 100 µF of output capacitance is needed, the associated voltage drop will be about 50 mV. Subtracting this 50 mV from the 234-mV allowable drop leaves 184 mV for the ESR voltage drop.

The maximum allowable ESR can now be calculated:

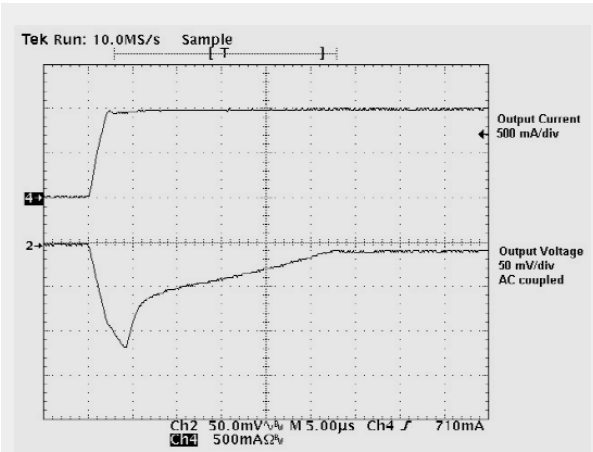
$$ESR_{max} = \frac{\Delta V_{ESR,max}}{\Delta I} = \frac{184\,mV}{1\,A} = 184\,m\Omega. \quad \textbf{(3)}$$

For the assumed 5-µs response time and 100-µF capacitance, the ESR should be less than 184 mΩ. There are numerous electrolytic and tantalum capacitors that meet this requirement. Selecting a 10-V, 100-µF tantalum with 55 mΩ of ESR should provide plenty of margin in meeting the specifications. The transient response for this example is shown in Figure 10. In fact, the output voltage droops about 120 mV, which is well within the specifications.

Summary

Selecting an LDO that is tailored to fast-transient loads is the first step in minimizing the effects of transients. Equally as important is the selection of the output capacitor. Understanding the load requirements and the behavior of the LDO and output capacitor can provide confidence in the design of a power distribution strategy. With this understanding, the designer can optimize a design for performance, board area, and cost.

Figure 10. Design example transient response



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For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Bang S. Lee, "Technical Review of Low Dropout Voltage Regulator Operation and Performance," Application Report	slva072
2. Bang S. Lee, "Understanding the Stable Range of Equivalent Series Resistance of an LDO Regulator," *Analog Applications Journal* (November 1999), pp. 14-16	slyt010
3. Bang S. Lee, "Understanding the Terms and Definitions of LDO Voltage Regulators," Application Report	slva079
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5. Everett Rogers, "Stability Analysis of Low-Dropout Linear Regulators with a PMOS Pass Element," *Analog Applications Journal* (August 1999), pp. 10-12	slyt005

Related Web sites

http://power.ti.com
www.ti.com/sc/docs/products/analog/tps75333.html
www.ti.com/sc/docs/products/analog/tps75433.html

Comparison of different power supplies for portable DSP solutions like an MP3 player working from a single-cell battery

By Juergen Neuhaeusler
Power Management Systems Engineer

Introduction

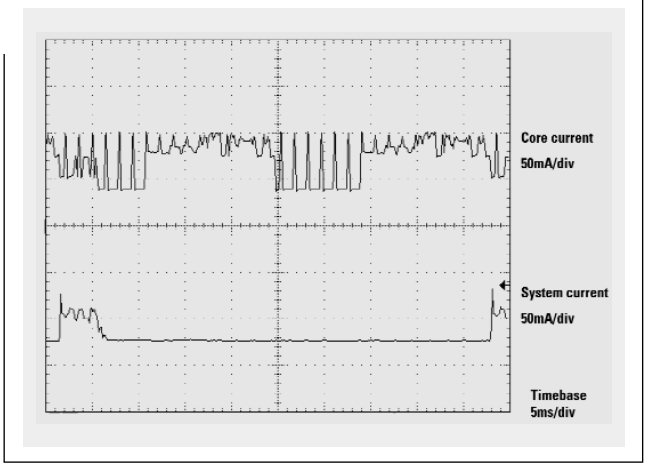
There are different ways to approach today´s requirements for power supplies in portable DSP solutions. Normally two system voltages are needed, one for the DSP core and the other for DSP I/O and the rest of the system. A major concern is that the power supply needs to be highly efficient to extend battery life. This article introduces different configurations of DC/DC converters that address these requirements. With an MP3 Internet audio player used as an example, the system designs are explained and analyzed for performance, total efficiency, and cost.

The problem

Because modern DSPs require dual supply voltages with restricted voltage tolerances, it is impossible to supply circuits directly from the batteries; so suitable DC/DC converter solutions have to be designed.

Another design challenge is the load behavior, as can be seen in the transients in the core and system supply current of an Internet audio evaluation module (EVM) shown in Figure 1. There are different tasks running in the software that are reflected as transients in core and system current, such as waking up the DSP to service DMA interrupt and performing decode and media access. Because both core and system have to be supplied by the same energy source, additional problems can occur through superimposition of these current pulses. Engineers are faced with a demand for designs that offer good performance at low cost—especially for battery-powered equipment, where good performance of the power supply circuit means the highest efficiency and long battery life.

Figure 1. DSP input currents (core and system) for an Internet audio EVM

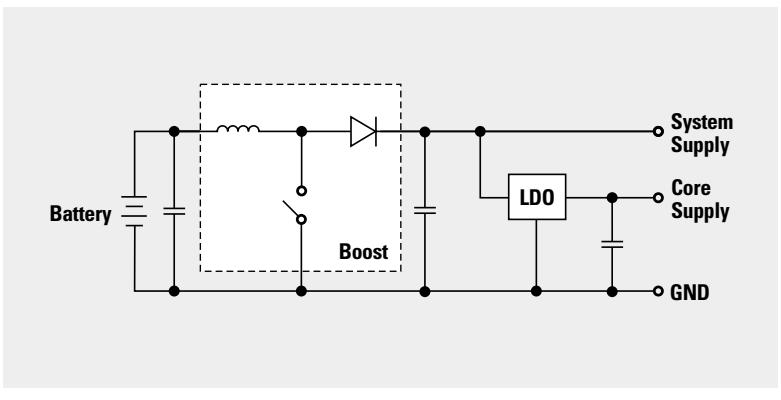


DC/DC converter solutions

In the following discussion, different designs of DC/DC converters are introduced that can be used to supply DSP core and system circuits with the typical two supply voltages. The designs are demonstrated on TI's Internet audio EVM, based on the TMS320VC5410 DSP, which requires 3.3 V for the system and 2.5 V for the core.

All of the DC/DC converters described are capable of operating from alkaline, NiCd, or NiMH batteries, so they must handle an input voltage range from 0.9 V up to 3.0 V. Because the system voltage is at 3.3 V and therefore higher than the maximum input voltage, a boost-based solution always must be used. Three different circuits are discussed. The first configuration is a boost converter with a cascaded LDO, the second is a dual-output flyback converter, and the third is a boost converter with a cascaded buck converter.

Figure 2. Boost converter with cascaded linear regulator



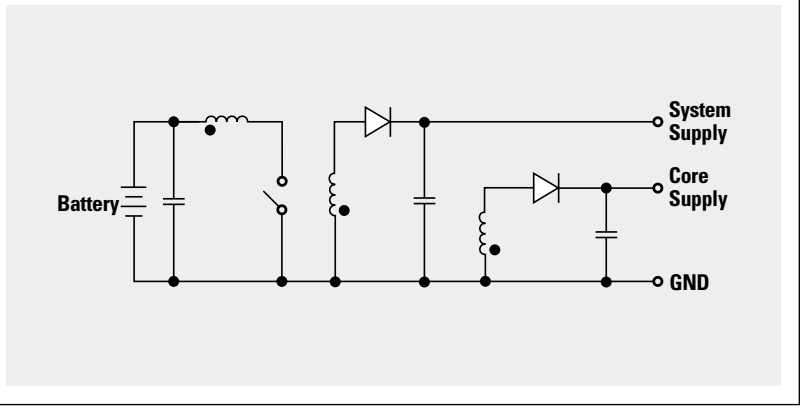
Boost converter with a cascaded linear regulator

The first and simplest solution is the boost converter with a cascaded linear regulator. As shown in Figure 2, the boost converter stage is connected directly to the battery with a blocking capacitor. At the output of the boost (which is also the system supply), the linear regulator is connected to generate the lower core voltage.

The standard boost converter shown in Figure 2 operates with one active switch, which is controlled by a pulse-width modulation (PWM) scheme. When the switch is closed, the inductor is charged by the battery. Opening the switch redirects the current through the rectifier to the output capacitor, which then is charged. The ratio between input and output voltages is determined by the duty cycle. Details about the design and operation of a boost converter can be found in References 1 and 2.

Due to the nature of boost converters, the input current is continuous and the output current is discontinuous. This is important to consider when choosing the capacitors around the converter and will be explained later in this article. To increase efficiency, use of a converter with synchronous rectification is highly recommended, because it uses a MOSFET switch instead of the diode to reduce the conduction losses. To generate the core voltage, a linear regulator is used. The nominal dropout in this design is 0.8 V (3.3 V to 2.5 V), so a linear regulator with low dropout (LDO) has to be chosen. For details of operation and design, refer to the appropriate LDO datasheets.

Figure 3. Dual-output flyback converter



Dual-output flyback converter

The second solution provided is a flyback converter with a dual output, shown in Figure 3. The input to the flyback stage is connected directly to the battery.

From a battery standpoint this input is similar to the boost input, except that the rectification is done differently. The inductor is divided into three windings. It is charged through the primary winding (similar to the boost) and discharged through the two secondary windings. Regulation is also achieved by a PWM scheme, but only one output can be regulated. The second output will follow this regulation indirectly through the winding ratio of the two secondary windings. The inductor discharge current will always flow into the output where the voltage is lowest. Under special operating conditions, the unregulated output can break down when it is under full load and the regulated output is under a light load or freewheeling. To avoid problems this must be taken into consideration when choosing the output that is regulated by the PWM controller that controls the flyback switch. When selecting the capacitors it is important to know that the input and output currents are discontinuous. Details about design and operation of flyback converters can be found in References 1 and 3.

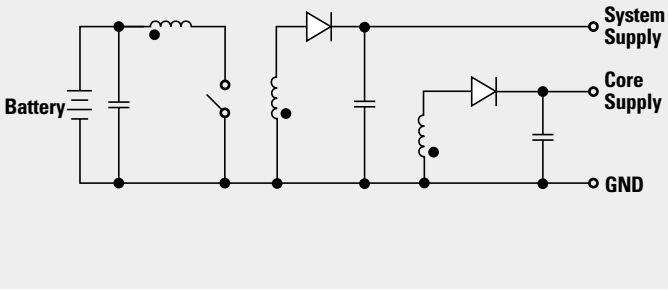
Because no converters for synchronous rectification of multiple-output flyback applications are available, it is not possible to design a small, highly efficient circuit. The voltages of the system and core supplies have a difference of only 0.8 V in our test circuits, so there is no gain in efficiency using the non-synchronous flyback solution compared to the synchronous boost + LDO solution. In addition, the design of the flyback solution is significantly more costly and requires more board space due to the customized inductor, which is larger and more expensive than a standard boost inductor. Therefore this solution is not considered in this article.

Boost converter with cascaded buck converter

The third solution, a boost converter with a cascaded buck converter, is the most costly but also the most efficient. It consists of the same boost converter as the solution with the LDO; but, instead of the LDO, a buck converter is added. The block diagram is shown in Figure 4. The standard buck converter also operates with one active PWM-controlled switch. When the switch is turned on, the inductor is charged. Turning off the switch leads to a freewheeling phase where the inductor current flows through the buck rectifier diode. The ratio between input and output voltage is also determined by the duty cycle. Details about the design and operation of buck converters can be found in References 1 and 4.

For defining the input and output capacitors, it is important to know that in a buck converter the input current is discontinuous and the output current is continuous. This also helps in design optimization. When the buck converter is controlled in a way that requires input current in the switching phase, where the boost converter delivers output current, the stress to the storage capacitors for the system voltage can be reduced by

Figure 4. Boost converter with cascaded buck converter



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trailing edge/leading edge synchronization. This means that the buck switch will be turned on after the boost switch is turned off. The efficiency of a buck converter also can be increased by using synchronous rectification with a MOSFET instead of using a diode.

The capacitors

The boost input capacitor serves to decouple the boost input from the battery and its connection (battery terminal, cables, and PCB traces). In general, it can be said that the more capacitance you add, the better it will be for the battery. But this will be effective only if the equivalent series resistance (ESR) of the capacitance is lower than the series resistance and impedance of the battery and its connection. Optimization can be done when these design parameters are known. Due to the continuous current at the boost converter input, the input capacitor is needed only for decoupling and lowering the current ripple of the input current. Therefore it will not affect power conversion efficiency to leave out this capacitor in very cost-sensitive designs. It is normal to use a 10-µF X7R or X5R ceramic capacitor, as in the designs described here.

The boost/flyback output capacitor is needed to supply the load during the charging phase of the inductor in normal operation. So its value and ESR are the main determining factors for the output ripple. Relevant parameters for the calculation of the minimum capacitance are the maximum output current and the desired voltage ripple on the output voltage, as well as the duty cycle and the operating frequency. The output capacitor also can be used to cover a current transient impulse with a corner frequency above the crossover frequency of the boost converter. Because of this, high-performance capacitors such as ceramic capacitors or low-ESR/ESL tantalum capacitors are a good choice.

The LDO output capacitor is used to stabilize the control loop of the LDO. Due to the high loop-gain bandwidth, the LDO normally requires no additional output capacitance to cover current transient impulses. Energy storage is better done at the input of the LDO. The buck input capacitor also has a storage function because of the discontinuous current of the buck converter input. It dampens the input current impulses and so reduces the stress on the supplying components. In this design the buck input is connected to the boost output, where the same considerations on the capacitors have to be made. Due to the synchronization with the boost converter and the output capacitors of the boost converter already on the board, no additional capacitors are necessary for the buck input.

The output current of the buck converter is continuous. Ideally, no capacitor is necessary, but stabilizing the control loop and covering fast-transient current pulses with a corner frequency above the crossover frequency of the buck converter requires capacitance. For this task, a high-performance capacitor is recommended. Storing energy to cover current pulses with a corner frequency below the crossover frequency is better done at the input of the buck converter. Due to the higher operating voltage at the input, more energy will be stored in the same capacitance and volume, assuming that the voltage ratings of the capacitors are the same.

Final designs and measurement results

Power supply needs

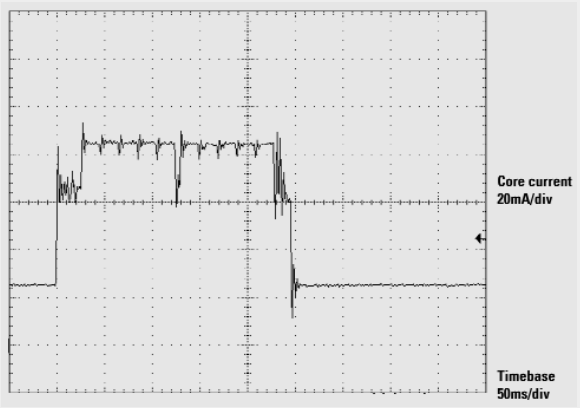
The Internet audio EVM used for this article requires 2.5-V core voltage with a maximum current of 120 mA. The average is in the range of 90 mA. The system supply is 3.3 V and requires a maximum current of 90 mA, with an average of 70 mA.

Identifying the corner frequencies of core and system current

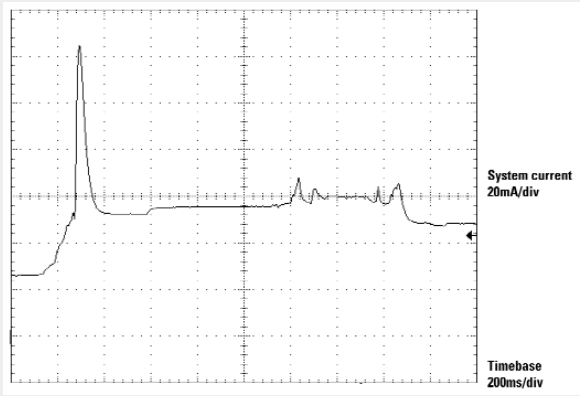
The oscilloscope plots in Figure 5 show the rising edge of the fastest current pulses of core (a) and system (b) supply current.

With the rise time of the rising edges, the corner frequency can be calculated ($f_c = 0.35/t_r$). The result for core current is in the range of 230 kHz. Because DC/DC converters usually have crossover frequencies in the range

Figure 5. Fastest load transients of core and system supply



(a)



(b)

of 10 kHz, this corner frequency must be lowered by using additional storage/blocking capacitance. An additional 10-µF tantalum capacitor with an ESR lower than 3 ohms would reduce this corner frequency to the range of 1 kHz, well within the acceptable range. The same is done for the system supply. A corner frequency of 20 kHz is calculated with the data of the shown pulse. To ensure proper operation, this frequency should be lowered to a value of 1 kHz by using additional output capacitance in the range of 10 µF.

Identifying the maximum current pulses for system supply

The worst case of the total system current is shown in the oscilloscope plot in Figure 6. Because the peak of this current pulse lies above the maximum operating current, the pulse was covered by increasing the storage capacitance of the system supply (boost output). With the parameters from this pulse it is possible to calculate the required capacitance by allowing a maximum voltage decrease of 0.1 V caused by this current pulse. A minimum storage capacitance of 225 µF with a total ESR lower than 0.1 ohms can be calculated. To achieve this, two additional 120-µF tantalum capacitors with low ESR of 0.85 ohms were added in parallel to the output of the boost in both configurations previously discussed. Another way to cover this kind of pulse is to oversize the basic DC/DC converter, which usually is more costly and requires more board space.

Description of boost + LDO circuit

Figure 7 shows a test circuit that uses a boost converter with a cascaded LDO. For this design the TI TPS61016 boost converter is used. It is a synchronous boost converter with integrated switches and a fixed output voltage of 3.3 V. This device is capable of covering the whole input voltage range from 0.9 V up to 3.0 V. As shown in the figure, it requires a small number of external components to operate. Input and output capacitors (defined earlier) are added. The TPS76925 is used as the LDO. A small tantalum capacitor is added at the output for stable operation.

Table 1 shows the parts list for this circuit with the cost added for each component.

Continued on next page

Figure 6. Worst-case total system current

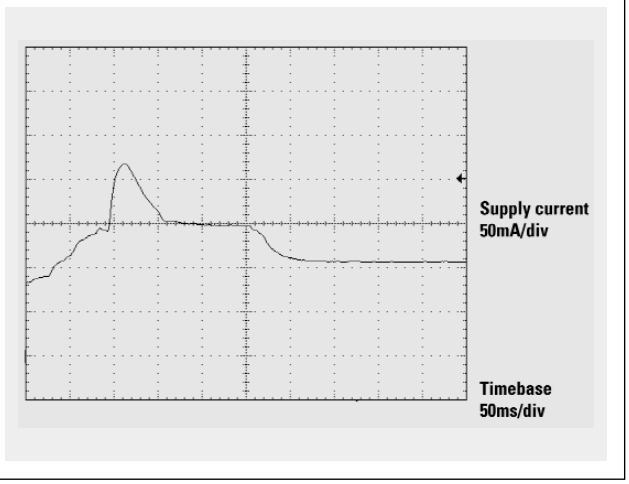


Table 1. Parts and cost of boost + LDO circuit

COMPONENT	DESCRIPTION	COST (%)
Input capacitor	10 µF X5R 6.3 V	10
Boost output capacitors	2 x 120 µF 594D 6.3 V	34
LDO input capacitor	1 µF X5R 6.3 V	1
LDO output capacitor	10 µF 293D 10 V	7
Boost inductor	CDR63	7
Boost converter	TPS61016DGS	30
LDO	TPS76925DBV	10
Various passive components		1
	TOTAL	100

Figure 7. Complete schematic of boost + LDO solution

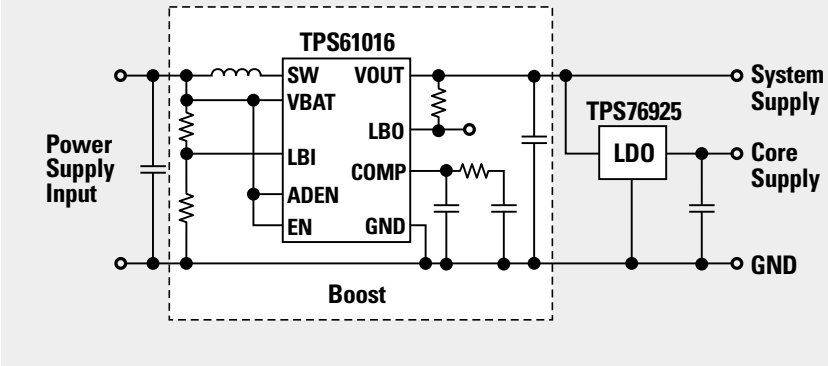


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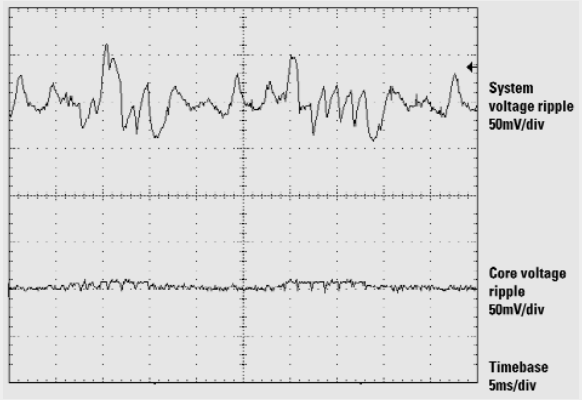
Figure 8 shows the ripple of core and system voltage during operation at an input voltage of 1.2 V (single battery NiXX).

It can be seen that the ripple is lower as designed. Figure 9 shows, in the upper trace (100-mV ripple), the power consumption of the Internet audio EVM under normal operation (playing music) versus the input voltage. The power losses in the boost input circuit increase due to the higher current at lower voltages.

Figure 8. Ripple of core and system voltage of a boost + LDO solution during operation



Description of a boost + buck circuit

Figure 10 shows a test circuit that uses a boost converter with a cascaded buck converter. The boost circuit is the same as in the boost + LDO solution, and the buck circuit is based on the TPS62006*, a synchronous buck converter IC with integrated switches. It offers a fixed output voltage of 2.5 V and is easiest to synchronize with the boost converter. There are only a few external components required for operation. Input and output capacitors also are added as suggested before.

Table 2 shows the cost calculation based on the parts list for the total circuit.

*Future product. Contact TI for availability.

Table 2. Parts and cost of boost + buck circuit

COMPONENT	DESCRIPTION	COST (%)
Input capacitor	10 µF X5R 6.3 V	10
Boost output capacitors	2 x 120 µF 594D 6.3 V	34
Buck input capacitor	1 µF X5R 6.3 V	1
Buck output capacitor	22 µF X5R 6.3 V	17
Boost inductor	CDR63	7
Buck inductor	LQH4C	3
Boost converter	TPS61016DGS	30
Buck converter	TPS62006DGS	30
Various passive components		1
	TOTAL	133

Figure 9. Power consumption of boost + LDO and boost + buck solutions

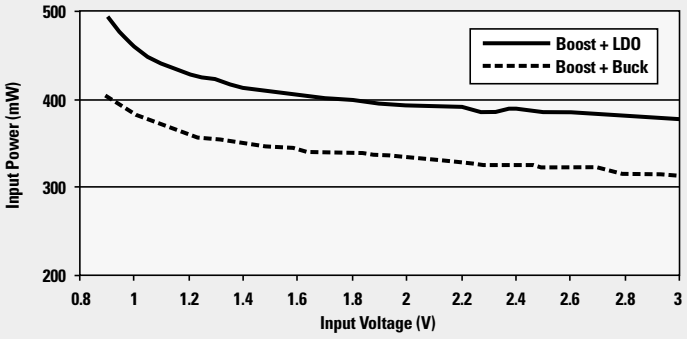
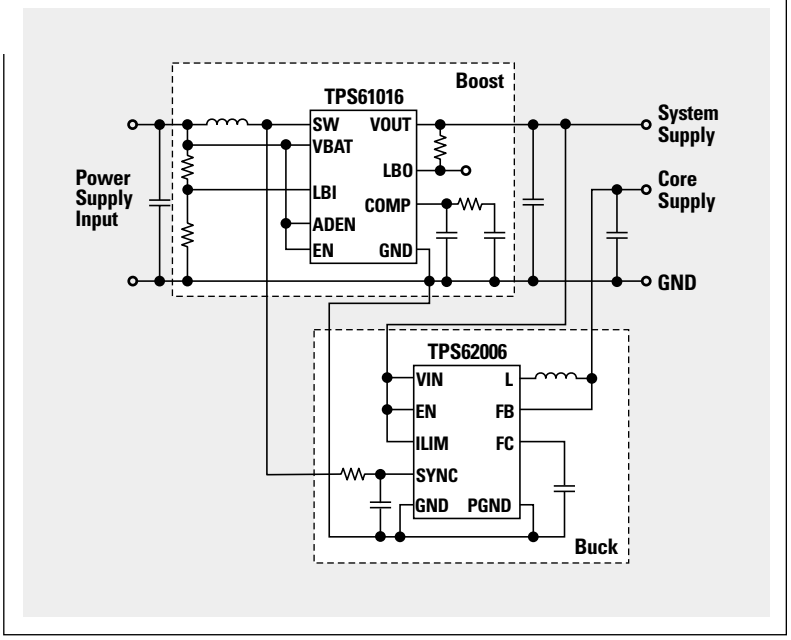


Figure 11 (voltage waveforms) and Figure 9 (power consumption, lower trace) show the results of the measurements.

Conclusion

From comparing the results of the power consumption measurements, it is clear that the boost + buck configuration is significantly more efficient. A single battery supply provides about 4.2 hours of operating time for the boost + LDO solution and 5 hours for the boost + buck solution, so the latter offers an improvement of about 20% in battery life. The trade-off is higher power supply system cost. The boost + buck solution is 33% more expensive and requires more board space. There is no doubt that the boost + LDO circuit is much easier to design. Fewer calculations have to be made to select the right components, and no synchronization has to be implemented. Regarding the future development of DSPs, the gap between core and I/O (system) voltage is increasing, leading to an increasing gap in power consumption between the two solutions. This could make the flyback solution more attractive. In the end, the designer has to decide whether he wants a simple and small solution or a more expensive, larger, but more efficient power supply.

Figure 10. Complete schematic of boost + buck solution

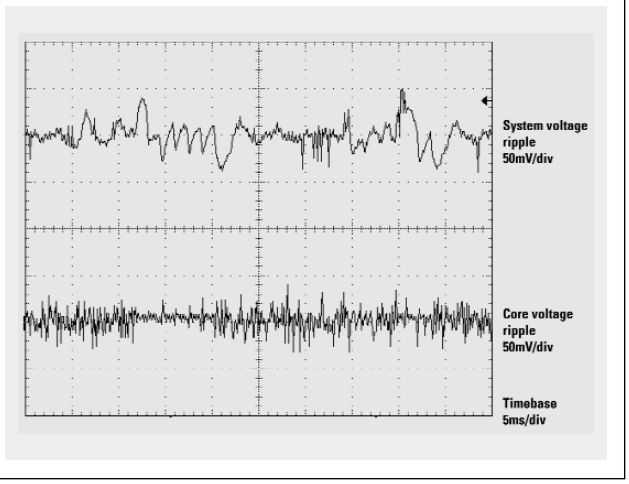


References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Robert W. Erickson, *Fundamentals of Power Electronics*, ISBN 0-412-08541-0.	—
2. "Understanding Boost Power Stages in Switchmode Power Supplies," Application Report	slva061
3. "Understanding Buck-Boost Power Stages in Switchmode Power Supplies," Application Report	slva059
4. "Understanding Buck Power Stages in Switchmode Power Supplies," Application Report	slva057

Figure 11. Ripple of system and core voltage of a boost + buck solution during operation



Related Web sites

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www.ti.com/sc/docs/products/analog/tps61006.html
www.ti.com/sc/docs/products/analog/tps76925.html
www.ti.com/sc/docs/products/dsp/tms320vc5410.html

A statistical survey of common-mode noise

By Jerry Gaboian
Characterization Engineer, High Performance Linear Department

Introduction

In today's high-tech world, one does not have to look very far to find some sort of noise generator, whether in the home or office. Knowing the many different sources of noise and its behavior in an electronic circuit is very valuable to the designer and user. The first part of this article defines some fundamental concepts of noise, while the latter part demonstrates the effect of noise induced on cables of different lengths.

Noise sources

EMI

Electromagnetic interference (EMI) is a signal that can cause undesirable performance in a device or system.

Electronic equipment can be divided into two main categories. The first consists of devices from which RF signals are deliberately emitted, such as radio and television transmitters, citizens' band and amateur radio transceivers, cellular telephones, radar and electronic navigation systems, etc. The second category is composed of devices that emit unintentional RF signals, such as computers, home television and stereo sets, fluorescent lights, power tools, power lines, and office equipment such as printers, copiers, fax machines, etc. It is this category that gives us the most grief.

There are, of course, natural sources of EMI such as lightning, cosmic radiation, solar radiation, and nuclear decay. These are unique and require special consideration that is beyond the scope of this article.

High-impedance circuits are most susceptible to capacitive coupling from nearby circuits with rapid and large voltage swings and to inductive coupling from nearby circuits with rapid changes in large currents. These transients are momentary changes in voltage and current that can be measured from milliseconds to nanoseconds. Often this transient is called a voltage or current spike.

Most respectable electronic equipment has an EMI filter on the front end of the power supply. The FCC requires this filter to stop most noise conducted from the power lines through the supply. Unfortunately, noise can find other paths into the device. EMI may be radiated and can couple into the system through the metallic enclosures or through the data lines. Unshielded twisted pair (UTP) is a likely candidate for coupled noise. This is especially true if there is an inadequate ground or the cable is routed close to a noise source.

Conducted noise still can enter the system through the ground. If the ground wire contains electrical signals, they will travel the path of least resistance and sometimes return to their point of origin—a device, ground, or even earth.

Many computer problems have electrical or magnetic origins. Monitor problems, for example, often are caused by nearby magnetic fields, neutral wire harmonics, or conducted/radiated electrical noise. Intermittent lockup of computers often is caused by ground loops. An electrical wall outlet improperly wired or grounded also causes many problems.

RFI

There are two modes of radio frequency interference (RFI): via radiation (electromagnetic waves in free space) and via conduction over signal lines and ac power distribution systems.

One of the most significant contributors to radiated RFI is the ac power cord. The power cord is often a very efficient antenna, since its length approaches a quarter wavelength for RFI frequencies present in digital equipment and switching power supplies.

Conducted RFI is induced over the ac power system in two ways. Common-mode (asymmetrical) RFI is present on both the line and the neutral current paths with reference to the ground or the earth path. Differential (symmetrical) RFI is present as a voltage between the line and neutral leads.

Ground loops

One of the most difficult types of power problems to understand, diagnose, and resolve is the ground loop. All types of equipment are susceptible to this type of problem, whether medical, industrial, or data processing. Ground loops can cause data errors, component failures, lockups, and even—in the worst case—safety hazards.

Grounding is used primarily to insure safety from fire and hazards. An important aspect of this protection is a reliance on multiple or redundant grounds. If one ground is accidentally removed or disconnected, the additional safety paths still exist. This redundancy has one major side effect—it can create ground loops.

Grounding is also used to terminate the shield on transmission lines and to prevent radiated emissions from getting in or out.

When ground loops are formed, the current that flows in the system ground is very unpredictable. This ground current can be caused by voltage differences, induction from other cables or devices, wiring errors, ground faults, or normal equipment leakage. The currents can be dc, 60 Hz, or very high-frequency.

Ground loops can cause specific equipment problems in three ways:

1. Low-energy currents in the grounds generate voltages that can cause data errors. These can be low-frequency, such as a 60-Hz hum, or high-frequency, classified as electrical noise.
2. High-energy transients choose data grounds instead of power grounds to clear to earth. These transients can

be caused internally by switching or inrush currents, such as the initial charge on the input capacitors in a switching power supply; or externally by the starting of a high-inductive motor or by lightning. These transients can cause equipment damage to drivers, receivers, microprocessors, and almost any electrical component if the surge is high enough.

3. Ground loops are one cause of common-mode noise between phases, neutral, and ground in a power distribution system. This noise is injected into the power supplies, which in turn pass it on to the electronic components.

Common-mode noise

The term “common-mode noise” is used in both ac power management and in circuit design considerations. Both environments will be discussed.

Common-mode noise in terms of ac power is the noise signal between the neutral and the ground conductor. This should not be confused with normal-mode noise, which is referenced between the line (hot) and the neutral conductor.

Common-mode noise impulses tend to be higher in frequency than the associated normal-mode noise signal. This is to be expected since the majority of the common-mode signals originate from capacitively coupled normal-mode signals. The higher the frequency, the greater the coupling among the conductors, line, neutral, and ground. Electronic equipment is 10 to 100 times more sensitive to common-mode noise than to normal-mode noise.

We would probably be surprised at the amount of noise present on the power line at any given time. The source of this noise is both the electrical distribution system outside the building and the one inside the building. The noise results from the power line’s dynamic nature of the ever-changing loads.

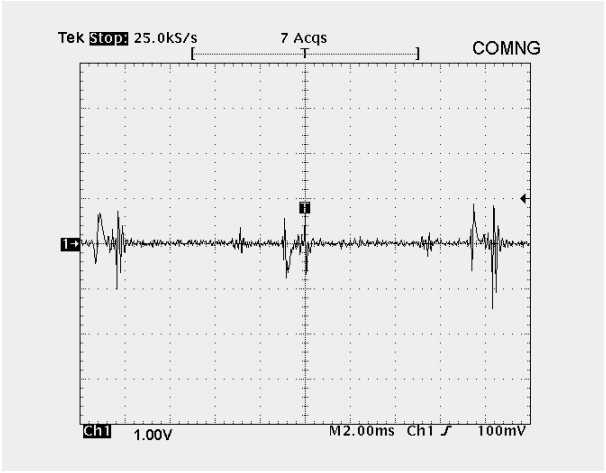
Figure 1 shows typical noise found on a power line. The noise was taken from unconditioned house power inside an IC characterization lab. Some of the signals occur at a regular repetition rate related to the 60-Hz power line frequency. This type of noise is common-mode signals found on the power line and is generally caused by some type of motor-driven device. If the oscilloscope were left in infinite persistence mode, we would see random or asynchronous noise from loads being switched on and off, power utility switching, or some natural phenomenon.

Conventional power transformers and isolation transformers will not block normal-mode noise impulses, but if the secondaries of these transformers have the neutral bonded to ground, they serve to convert normal-mode noise to common-mode noise. From the standpoint of microelectronic circuits, common-mode noise is even more potentially harmful than the normal-mode noise.

Common-mode voltage (CMV) identifies a voltage (noise) present on both input leads of an analog input with respect to analog ground (see Figure 2).

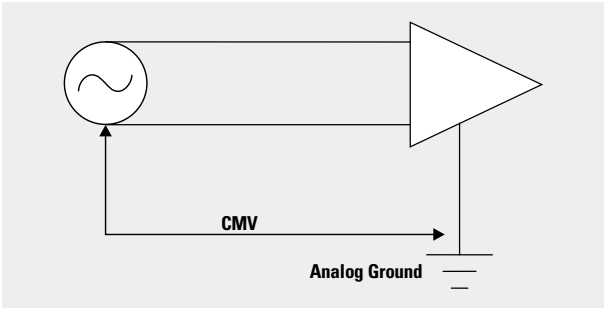
The biggest source of common-mode noise is the difference in potential between two physically remote grounds. This is often the case when dealing with networked computer equipment where ground loops can occur. Typical

Figure 1. Common-mode noise from neutral to ground



A line noise interface instrument from ONEAC was used.

Figure 2. Common-mode voltage



effects can be intermittent reboots, lockups, and bad data transfer. Network interface cards, serial ports, parallel ports, and modems are prime targets for some form of failure due to high CMV. If the CMV is high enough, component failure is possible.

The second most significant common-mode noise source is the potential due to ungrounded sources. Such problems can occur when a separate power supply is used to power the field device remotely and the remote power supply is left ungrounded.

RFI noise sources provide ample opportunity to induce common-mode noise. A poor ground system or an ungrounded analog signal cable can act as an antenna, gathering the induced voltage and applying it on the analog input. The most common methods of treating common-mode noise lose their effectiveness as the frequency of the common-mode noise increases.

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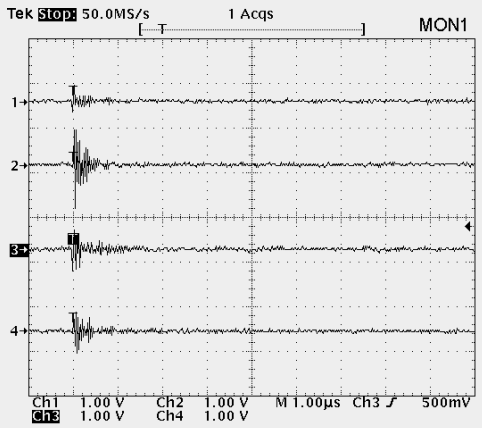
Common-mode rejection

Common-mode rejection (CMR) techniques exist to prevent common-mode noise from being converted to normal-mode voltage. These techniques relate to the ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. The CMR ratio (CMRR) is the ratio in dB of the differential voltage amplification to CMV amplification. CMR is often defined at an associated effective frequency with a maximum allowable input imbalance such as 120 dB @ 500 Hz 1000 ohms. A CMRR of 120 dB means that a 1-V CMV passes through the device as though it were a differential input signal of 1 µV. This implies that the higher the CMRR, the better.

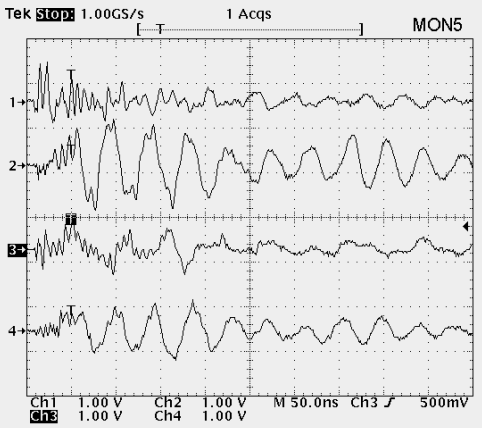
Experimental setups

There could be a big debate on which technique would provide the best data for measuring noise induced on a cable. Since the purpose of this article is to measure the effect of noise and not to characterize it, an oscilloscope was used to view the noise in a time/voltage domain

Figure 3. PC monitor power switched on/off with cables 6 inches from the monitor

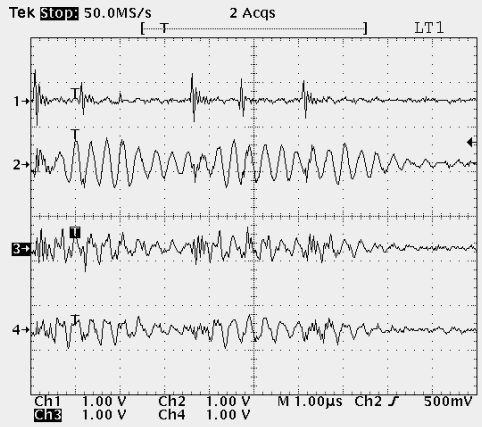


(a) Time scale: 1 µs/div

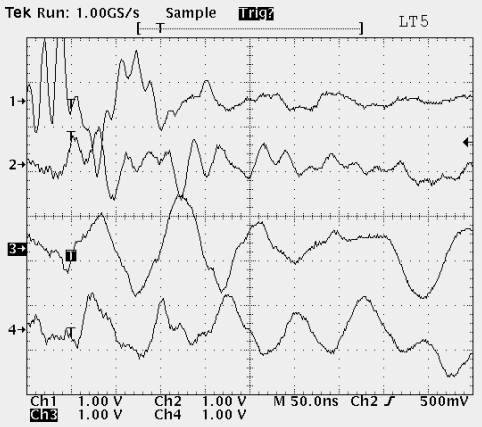


(b) Time scale: 50 ns/div

Figure 4. Fluorescent light switched on/off with cables 12 inches from the light



(a) Time scale: 1 µs/div



(b) Time scale: 50 ns/div

instead of using a spectrum analyzer to view the data in a frequency domain. The latter method could fill an application note by itself.

Figures 3–8 represent views of noise induced on cables of various lengths. The transmission line used in each case was an unshielded, 24-AWG, solid bare copper wire with polyolefin insulation, twisted pairs, and a PVC jacket. This line is Belden part #1588A, one of Belden's most-sold cables for data transmission. It is a standard category-5 cable. The lengths used on channels 1–4 of the oscilloscope were 3 ft., 30 ft., 100 ft., and 800 ft., respectively.

The cable mentioned has two pairs of conductors. In each case, the pair that was connected to the oscilloscope was terminated in 100 ohms at the load end of the cable. The oscilloscope used was a Tektronix TDS784C with termination on each channel set at 1 Mohm. The 30-, 100-, and 800-foot cables were coiled with the exception of a 6-foot length on each end. The coiled sections were placed 6 feet from the noise source.

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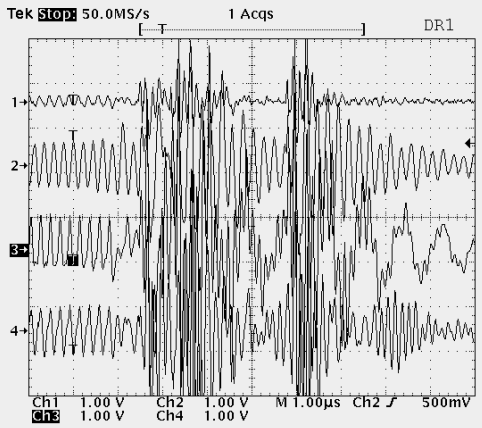
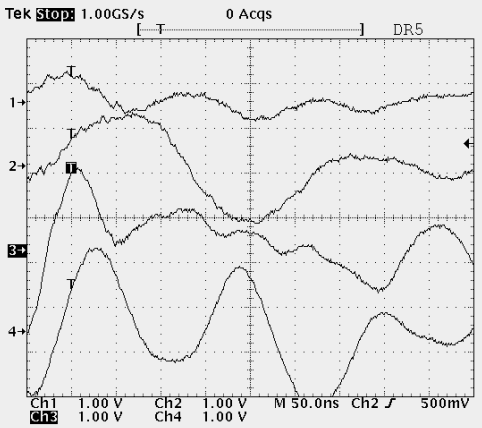
Figure 5. 110-V drill press motor with cables 10 inches from the motor

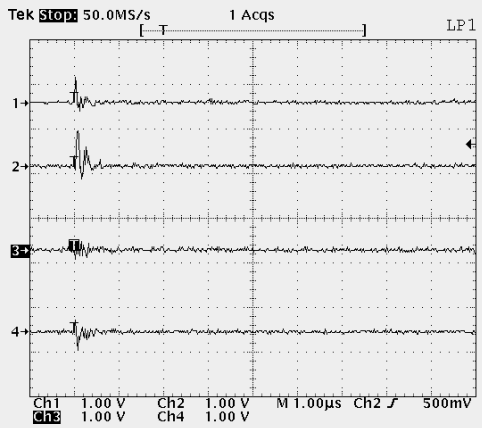


(a) Time scale: 1 µs/div

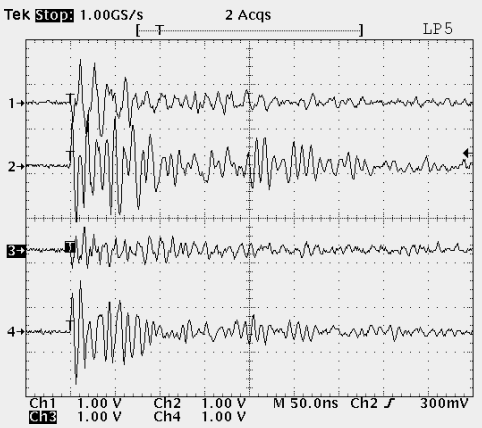


(b) Time scale: 50 ns/div

Figure 6. 208-V ac power line in conduit with cable insulation touching conduit



(a) Time scale: 1 µs/div



(b) Time scale: 50 ns/div

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Conclusion

It appears from Figures 3–8 that cable length made very little difference on the induction of noise in the environments described. There was some noticeable attenuation on the longer cables that could be attributed to the dc resistance of the cable and normal line loss factors. This was not always the case when the drill motor EMI was measured. The longer the cable, the greater the chance that high EMI fields will couple onto it. It should be pointed out that if the same test were done today, the results would be different because the noise level varies constantly. The noise was very unpredictable in all cases. We will never be able to eliminate all the noise in our environment. A good defense for common-mode noise would be to choose components that have a very high CMRR and a high common-mode operating range, such as the Texas Instruments LVDS and LVDM products.

Related Web site

www.ti.com/sc/docs/products/msp/intrface/default.htm

Figure 7. Cables tied to chassis ground on a VLSI logic tester and powered on/off

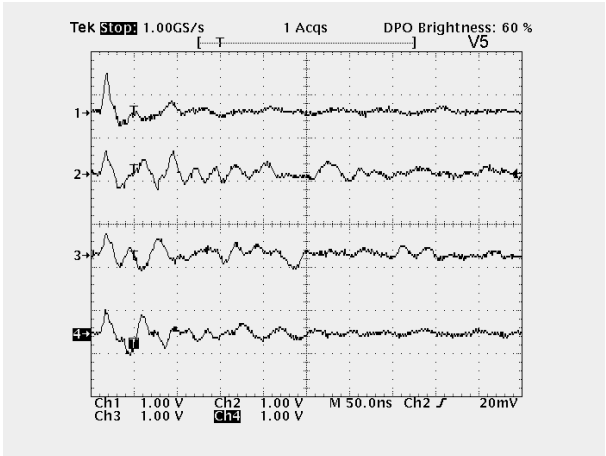
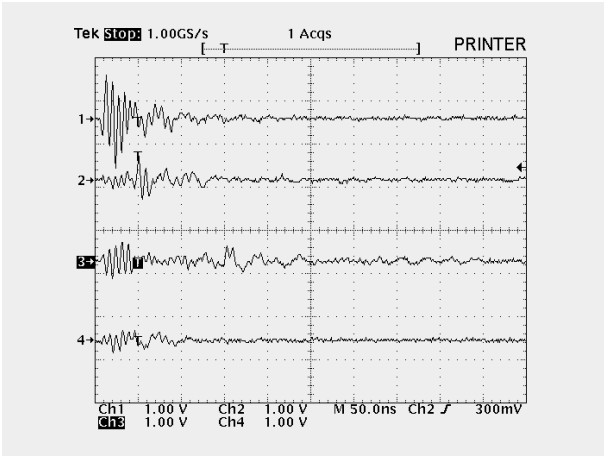


Figure 8. Cables connected to a networked laser printer ground during printing



The Active Fail-Safe feature of the SN65LVDS32A

By Mark Morgan, *Interface Design Manager, Data Transmission,*
and Bryan Smith, *Project Engineer, Data Transmission*

Introduction

Differential data line receivers can switch on noise in the absence of an input signal. This can occur when the bus driver is turned off or the interconnecting cable is damaged or disconnected. Generally, this problem is solved with an external resistor network applying a steady-state bias voltage to the undriven input pins. While this adds to the cost of external components, it lowers the input-signal magnitude and reduces the differential-noise margin.

The fail-safe function attempts to drive the output of the data receiver to a known state under floating or disconnected bus conditions. However, the fail-safe features of many existing differential receivers are limited to open-circuit conditions or restricted to only certain operating conditions. The SN65LVDS32A* (hereinafter referred to as the LVDS32A) Active Fail-Safe** function is not restricted to the limitations seen in existing solutions. This article explains some of the existing fail-safe solutions, the differences between them, and the advantages of using Active Fail-Safe.

What is Active Fail-Safe?

A fail-safe circuit provides a known receiver output when a valid input signal is not present. Receivers without fail-safe will oscillate in response to input differential noise. As previously mentioned, one technique to solve this problem is to bias the bus externally as shown in Figure 1. This maintains a dc offset in the absence of a valid signal. However, the presence of a bias network can unbalance the driver output loop currents. This can distort the output signal and possibly reduce the input signal amplitude to the receiver. When this happens, the possibility of switching on input noise is increased. Therefore, it is desirable to provide a fail-safe function with minimal impact on the input signal during normal operation.

Existing integrated fail-safe implementations rely on bias currents integrated internally into the receiver. As illustrated in Figure 2, the bias sources provide a current through the termination resistor. This ensures that a dc voltage is maintained across the termination resistor when a valid input signal is not present. The receiver in Figure 1 uses a pull-up and a pull-down current source to maintain a dc bias across the termination resistor. Other integrated solutions, such as in the non-A version of the LVDS32, use a pull-up on both input pins to bias each node up to V_{CC}. Logic detects this and drives the output to a known state.

The small bias currents used by existing integrated fail-safe solutions do not appreciably affect the input-signal magnitude. However, one disadvantage of the existing solutions is that the fail-safe bias currents are unable to generate the required differential with an external common-mode voltage applied. Increasing the bias currents to improve this would result in additional bus loading during normal operation. Additionally, the offset created when pulling the two differential signals apart increases the input-signal magnitude required by the receiver to switch. This offset also contributes to pulse skew, which is the difference between the time needed for the receiver to switch from LOW to HIGH and the time to switch from HIGH to LOW.

Figure 1. Input biasing

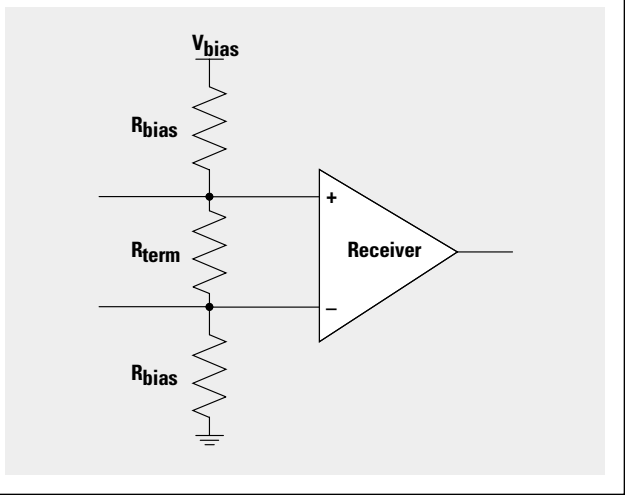
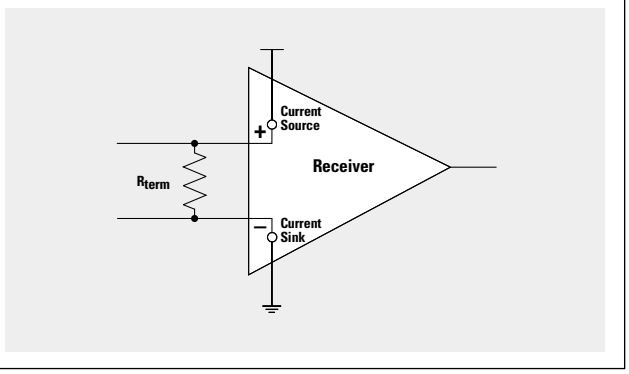


Figure 2. Receiver bias currents



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*The SN65LVDS32A Active Fail-Safe is also available in the following TI devices: SN65LVDT32A, SN65LVDS3486A, SN65LVDT3486A, SN65LVDS9637A, and SN65LVDT9637A.

**TI patent pending

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Fail-safe as implemented on the LVDS32A relies not on bias circuits but on a window-comparator circuit to monitor the differential voltage at the receiver input pins. The window comparator senses when the input differential is less than 80 mV and drives the output to a logic HIGH state. Because the new Active Fail-Safe requires no external resistor bias network or internal bias current to generate an offset, it neither affects the receiver input threshold nor adds any significant bus loading. The window comparator operates over the entire input common-mode range of the receiver. Therefore, Active Fail-Safe operates even when an external common-mode voltage is applied.

Active Fail-Safe operation

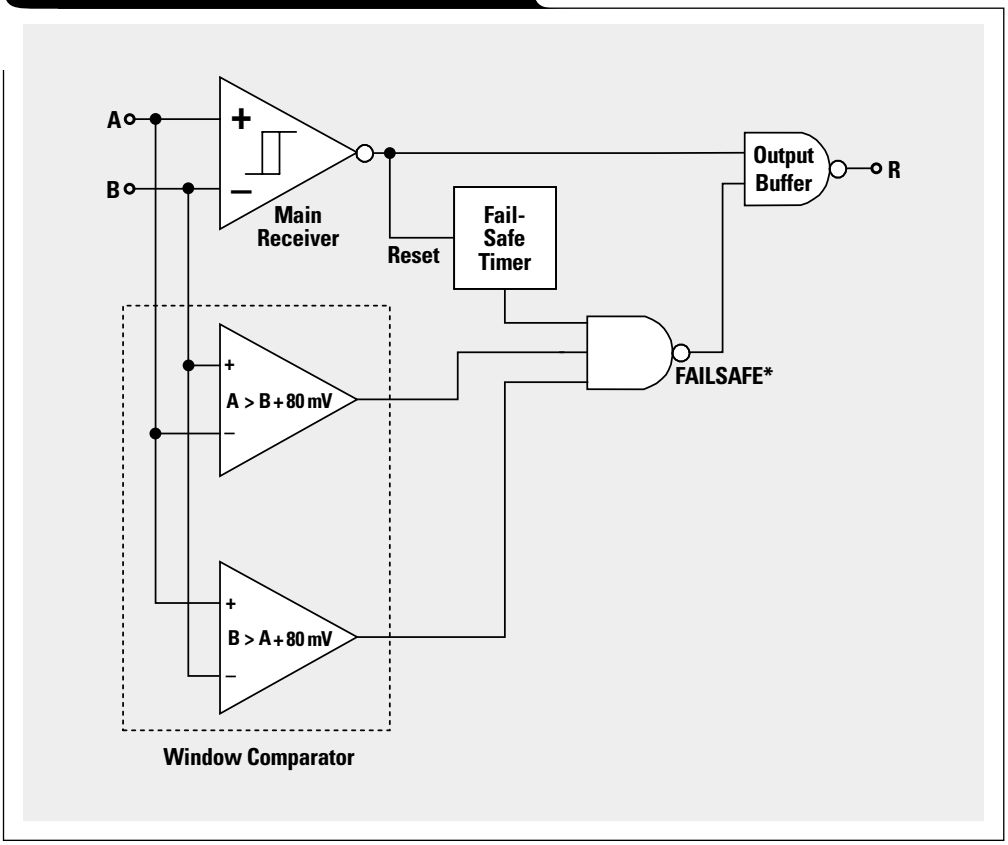
Figure 3 shows one of the LVDS32A receiver channels with Active Fail-Safe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two fail-safe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and detects when the input differential falls below 80 mV. A 600-ns fail-safe timer filters the window comparator outputs. When FAILSAFE* is asserted, the fail-safe logic drives the main receiver output to a logic HIGH.

During normal operation, the main receiver tracks the input signal. It switches when the input signal changes polarity and exceeds 50 mV of hysteresis. Each time the main receiver switches, the fail-safe timer resets and begins timing from zero.

The window comparator monitors both inputs on a continuous basis to detect a loss of input signal. If the two inputs are within 80 mV of each other, the window comparator outputs are driven HIGH. Then the window-comparator outputs are gated with the fail-safe timer. If the timer is allowed to reach its maximum value and the window comparator still detects a low differential input, the receiver output is driven to a logic HIGH state.

Under normal conditions and when the timer expires, the input differential signal is greater than 100 mV and, as illustrated in Figure 4, FAILSAFE* is not asserted. Here, the input signal begins with A greater than B by 400 mV. The input then switches polarity, and B is greater than A by 100 mV. When the input switches, the output of the receiver is driven LOW (upper trace of Figure 4) and the fail-safe timer begins timing. After approximately 600 ns, the timer output is set HIGH and enables the window comparator to drive the FAILSAFE* node. Since the difference between inputs is 100 mV (greater than the

Figure 3. Receiver with Active Fail-Safe



fail-safe threshold), FAILSAFE* is not asserted, and output node R remains at logic LOW, tracking the input signal.

If the fail-safe timer expires and the input differential is less than 80 mV, FAILSAFE* is asserted and output node R of the receiver is driven to logic HIGH. Figure 5 illustrates this condition. The input signal begins with A greater than B by 400 mV. The input then switches polarity with B greater than A by approximately 50 mV. When the input switches, the receiver output is driven LOW and the fail-safe timer is reset and begins timing. When the timer expires, since B is greater than A by only 50 mV, FAILSAFE* is asserted. Figure 5 illustrates the receiver output R being driven HIGH 600 ns after the switch, even though B is greater than A (normally a LOW output condition). This figure demonstrates how Active Fail-Safe functions when a valid input signal is lost.

After the fail-safe function has been asserted, the window comparator and logic continue to drive the output to a logic HIGH as long as the inputs remain within 80 mV of each other. If a valid differential signal is restored at the input, one window-comparator output is driven LOW, and the fail-safe signal is driven HIGH. The receiver then resumes tracking the input signal. Figure 6 illustrates this, starting with B greater than A by 50 mV and FAILSAFE* asserted (the fail-safe signal drives the output to logic HIGH). The input signal then increases in magnitude where B is greater than A by 400 mV. FAILSAFE* then is deasserted, and the receiver begins tracking the input signal, driving the output node R to a LOW state.

If the main receiver does not switch when the input is restored, the fail-safe timer does not reset. Thus, if the input signal subsequently is reduced in amplitude with no reversal of polarity, fail-safe will immediately resume control of the receiver output. If the application of the valid signal results in the main receiver switching, the fail-safe timer is reset, and any subsequent signal loss will not be detected until the timer is allowed to reach its maximum value.

Note that Active Fail-Safe relies on the main receiver hysteresis (50 mV) to keep FAILSAFE* asserted. If external noise is large enough to cause the main receiver to switch, the fail-safe timer is reset and the fail-safe function is disabled. FAILSAFE* will not be reasserted until the input noise is less than the receiver hysteresis for the entire fail-safe timer period.

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Figure 4. Receiver operation with valid inputs

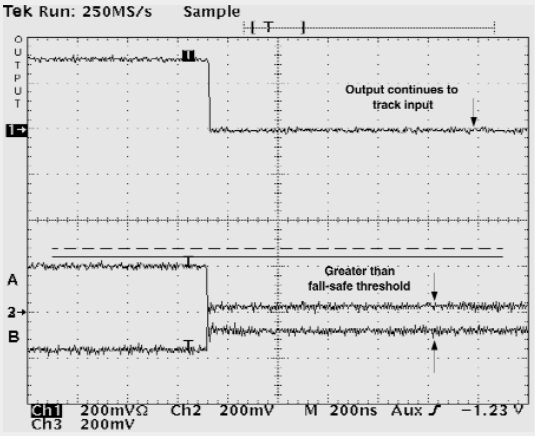


Figure 5. Receiver operation with invalid inputs

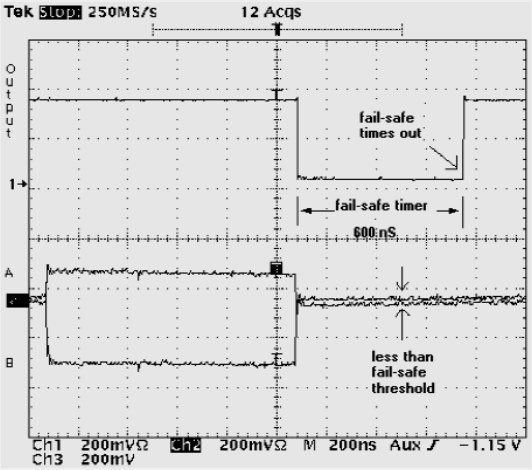
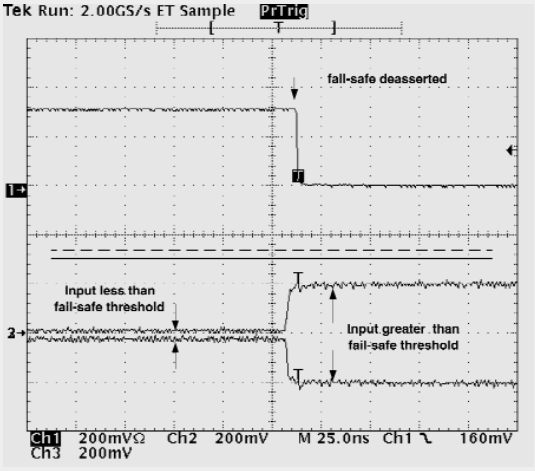


Figure 6. Restoration of valid input signal



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Active Fail-Safe-supported conditions

Active Fail-Safe guarantees that the output is driven to the fail-safe state when the input pins are shorted (from a crushed cable), left open (an unused receiver), or connected together through a termination resistor when the line driver is disabled or removed.

Following is a detailed summary of the supported fail-safe conditions.

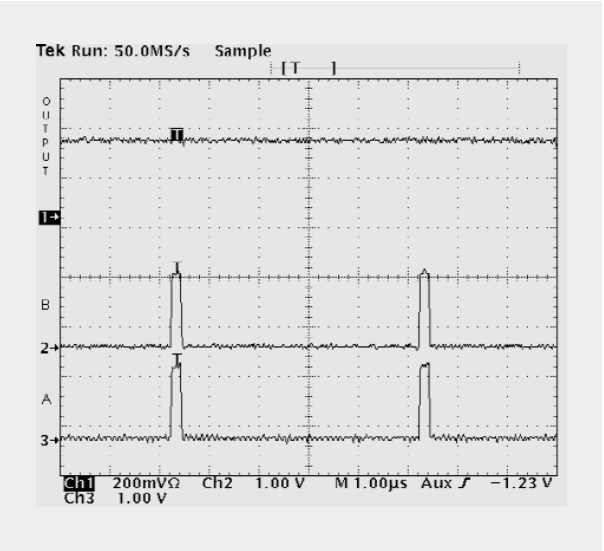
Open input pins—In a multipoint or multidrop configuration, unused nodes can be disconnected from the bus. It is also possible to have multichannel receivers with a portion of the channels used and with unused channels left open. If receiver inputs are left floating, both pins are pulled internally to the same potential. Active Fail-Safe detects this condition and drives the receiver output R to a logic HIGH.

Idle bus—If the receiver is connected to an idle bus with the driver in the high-impedance state (turned off), the receiver input pins are pulled to nearly the same voltage via the termination resistor. Normally this would be near the receiver's differential threshold, and any external noise would cause the receiver to switch. Active Fail-Safe detects the low differential input and provides a known output state.

Shorted input pins—Line-fault conditions (a crushed cable) can result in shorted inputs. Active Fail-Safe detects the input short and drives the output HIGH. Active Fail-Safe functions over the entire receiver input common-mode range, which is important in the presence of bus voltage biases, ground offsets, or common-mode noise.

Figure 7 illustrates the case when both receiver inputs are shorted together. Since FAILSAFE* is asserted, the output is HIGH. Both pins are held initially at ground potential. Common-mode voltage spikes are then coupled onto both inputs. The output remains at logic HIGH, demonstrating Active Fail-Safe functions over the entire input common-mode range.

Figure 7. Common-mode fluctuations on disconnected line



Conclusion

This article discussed a new type of fail-safe that overcomes the limitations seen in other fail-safe solutions. Active Fail-Safe presents minimal bus loading and therefore does not degrade the signal quality of the driver output as an external bias network would. Active Fail-Safe requires no internal offset in the signal path and therefore does not increase the input differential required for the receiver to switch, as do some integrated fail-safe solutions. Active Fail-Safe operates over the entire input common-mode range and assures a known state in the presence of common-mode noise, dc bias voltages, or system ground offsets.

Related Web sites

www.ti.com/sc/docs/products/analog/sn65lvds32a.html
www.ti.com/sc/docs/products/msp/intrface/default.htm

An audio circuit collection, Part 1

By Bruce Carter
Advanced Analog Products, Op Amp Applications

Introduction

This is the first of two articles on audio circuits. New operational amplifiers from Texas Instruments have excellent audio performance and can be used in high-performance applications.

There have been many collections of op amp audio circuits in the past, but all of them focus on split-supply circuits. Often, the designer who has to operate a circuit from a single supply does not know how to perform the conversion. Single-supply operation requires a little more care than split-supply circuits. The designer should read and understand the introductory material.

Split supply vs. single supply

All op amps have two power pins. In most cases they are labeled V_{CC}+ and V_{CC}–. Sometimes, however, they are labeled V_{CC} and GND. This is an attempt on the part of the data sheet author to categorize the part as split-supply or single-supply, but it does not mean that the op amp has to be operated with the split or single supply shown by the data sheet. It may or may not be able to operate from different voltage rails. Consult the data sheet, especially the absolute maximum ratings and voltage swing specifications, before operating at anything other than the recommended power supply voltage(s).

Most analog designers know how to use op amps with a split power supply. In a split-power-supply system, the input and output are referenced to ground. The power supply consists of a positive supply and an equal and opposite negative supply. The most common values are ±15 V, but ±12 V and ±5 V are also used. The input and output voltages are centered on ground and swing both positive and negative to V_{OM}±, the maximum peak output voltage swing.

A single-supply circuit connects the op amp power pins to a positive voltage and ground. The positive voltage is connected to V_{CC}+, and ground is connected to V_{CC}– or GND. A virtual ground, halfway between the positive supply voltage and ground, is the "ground" reference for the input and output voltages. Voltage swings above and below this virtual ground to V_{OM}±. Some newer op amps have different high- and low-voltage rails, which are specified in data sheets as V_{OH} and V_{OL}, respectively.

5 V is a common value for single supplies, but voltage rails are becoming lower, with 3 V and even lower voltages becoming common. Because of this, single-supply op amps are often "rail-to-rail" devices to avoid losing dynamic range. "Rail-to-rail" may or may not apply to both the input and output stages. Be aware that even though a device may be specified as "rail-to-rail," some specifications may degrade close to the rails. Be sure to consult the data sheet for complete specifications on both the inputs and the outputs. It is the designer's obligation to make sure that the voltage rails of the op amp do not degrade system performance.

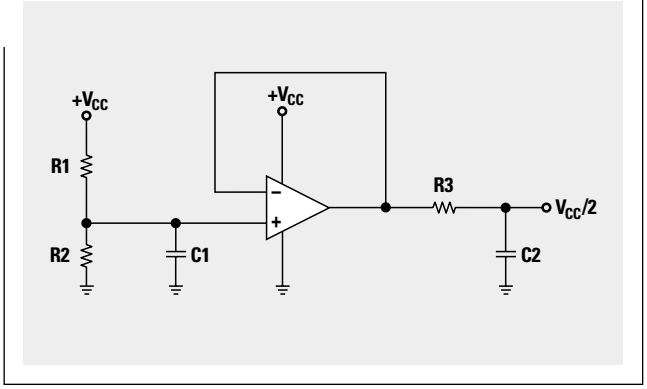
Virtual ground

Single-supply operation requires the generation of a "virtual ground" at a voltage equal to VCC/2. The external circuit can be a voltage divider bypassed by a capacitor, a voltage divider buffered by an op amp, or preferably a power-supply splitter such as the Texas Instruments TLE2426. Figure 1 shows how to generate a half-supply reference if the designer insists on using an op amp.

R1 and R2 are equal values selected with power consumption vs. allowable noise in mind. C1 forms a low-pass filter to eliminate conducted noise on the voltage rail. R3 is a small (47-Ω) resistor that forms a low-pass filter with C2, eliminating some of the internally generated op amp noise. The value of C2 is limited by the drive capability of the op amp.

In the circuits in the figures that follow, the virtual ground is labeled "VCC/2." This voltage comes from either the TLE2426 rail-splitter or the circuit in Figure 1. If the latter is used, the overall number of op amps in the design is increased by one.

Figure 1. Half-supply generator



Passive components

The majority of the circuits given in this series have been designed with standard capacitor values and 5% resistors. Capacitors should be of good quality with 5% tolerance wherever possible. Component variations will affect the operation of these circuits, usually causing some degree of ripple or increased roll-off as the balance of Chebyshev and Butterworth characteristics is disturbed. These should be slight—almost imperceptible.

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Speech filter

Human speech most frequently occupies an audio spectrum of 300 Hz to 3 kHz. There is a requirement, especially in phones, to limit the frequency response to this range. Frequently, this function is performed with a DSP chip. DSP chips, however, require an anti-aliasing filter to reject high-frequency components. The anti-aliasing filter requires an op amp. Since there is already an op amp anyway, why not consider adding a second and doing the entire function with analog components? An additional op amp (plus one for the half-supply reference) can perform the filtering with no aliasing problems, freeing the DSP for other tasks.

Figure 2 shows a single-supply phone speech filter in two op amps, five capacitors, and four resistors. This circuit is designed to be low-power and compact, and is scalable for even lower power consumption.

Figure 2. Single-supply phone speech filter

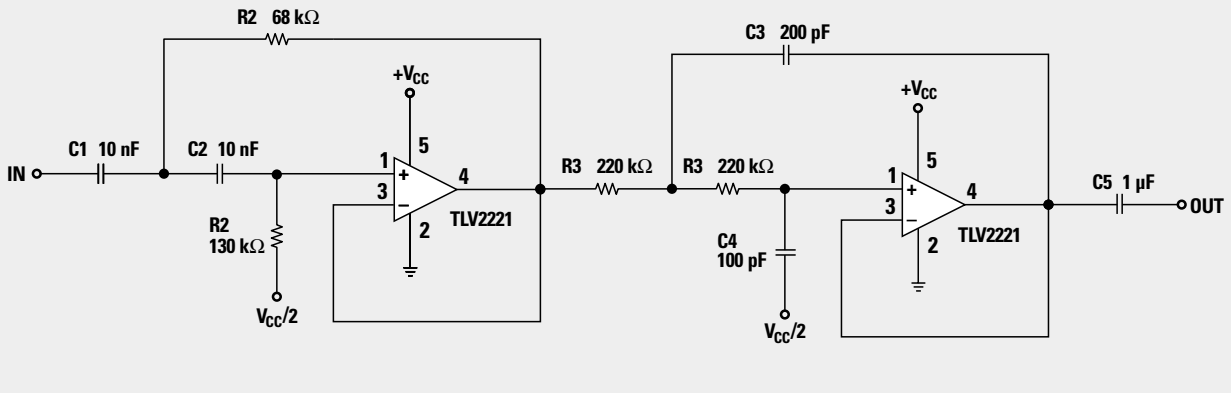


Figure 3. Second-order circuit

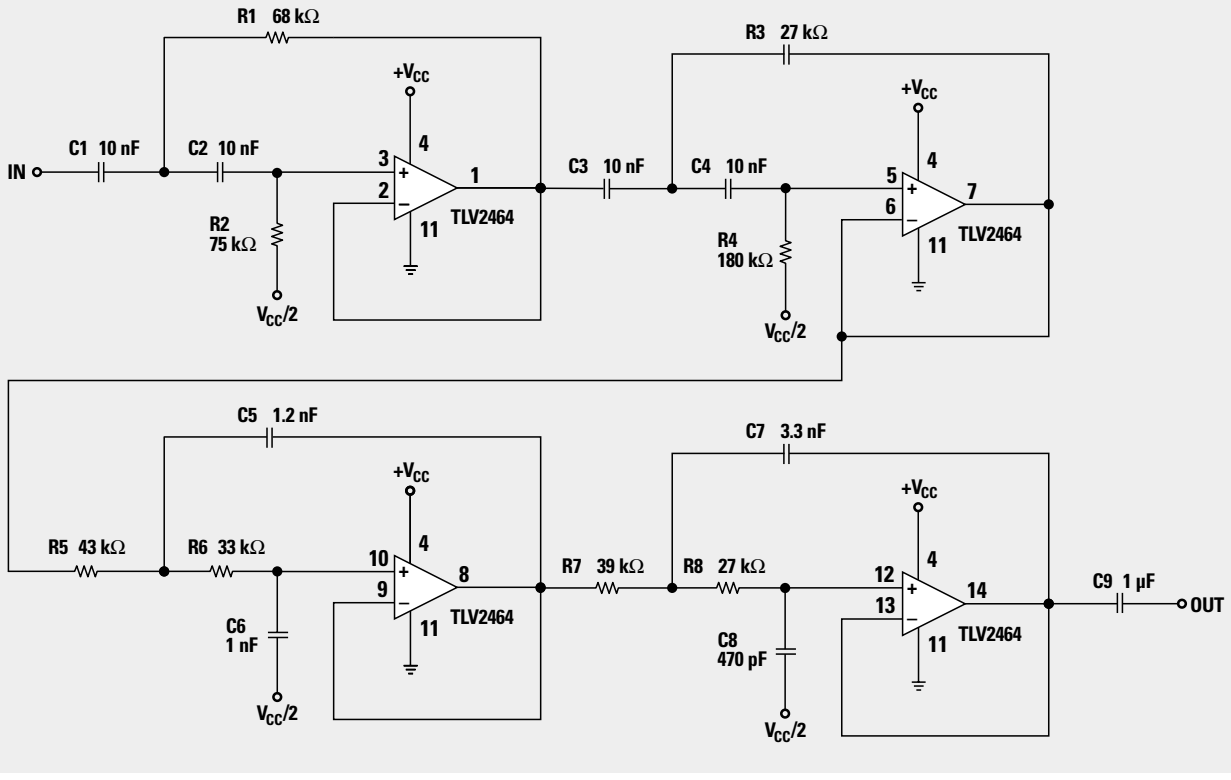
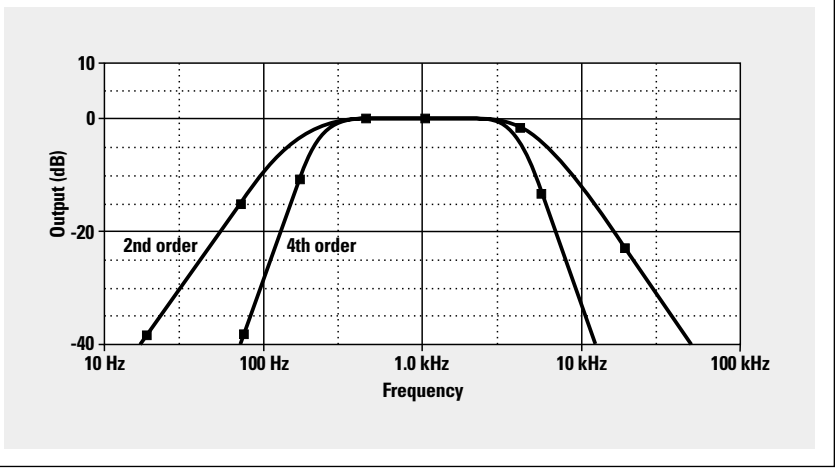


Figure 3 shows a second-order circuit. Nearby out-of-band signals, such as 60-Hz hum, are not rejected very well. This may be acceptable in cellular telephone headsets, but may not be for large switchboard consoles. A fourth-order speech filter, although more complex, can be implemented in a single quad op amp (with an external VCC/2 reference).

The response of the second- and fourth-order speech filters is shown in Figure 4. The 60-Hz rejection of the fourth-order filter is greater than 40 dB, while that of the second-order filter is about 15 dB. Both filters have been designed to have an imperceptible 0.5-dB roll-off at 300 Hz and 3 kHz.

Figure 4. Response of second- and fourth-order speech filters



Crossover filter

Inside any multiple-speaker cabinet is an array of inductors and capacitors that directs different frequency ranges to each speaker. The inductors and capacitors, however, have to handle the full output power of the power amplifier. Inductors for low frequencies in particular tend to be large, heavy, and expensive.

Another disadvantage of the inductor and capacitor crossover network is that it is a first-order network. At high volume, destructive levels of audio can be transferred to speakers not designed to handle a given frequency range. If a speaker is incapable of moving in response to stimulation, the only way the energy can be dissipated is in heat. The heat can build up and burn out the voice coil.

A number of audiophiles are beginning to talk about the virtues of bi-amplification, or even multiple amplification. In this technique, the crossover network is applied to the audio source before amplification instead of after it. Each speaker in the cabinet is then driven by a separate amplifier stage that is optimized for the speaker.

The primary reason for bi-amplification or multiple amplification is that human hearing is not equally sensitive to all frequencies. The human ear is relatively insensitive to low and high frequencies, but audio amplifiers are designed to have flat response (constant power) across

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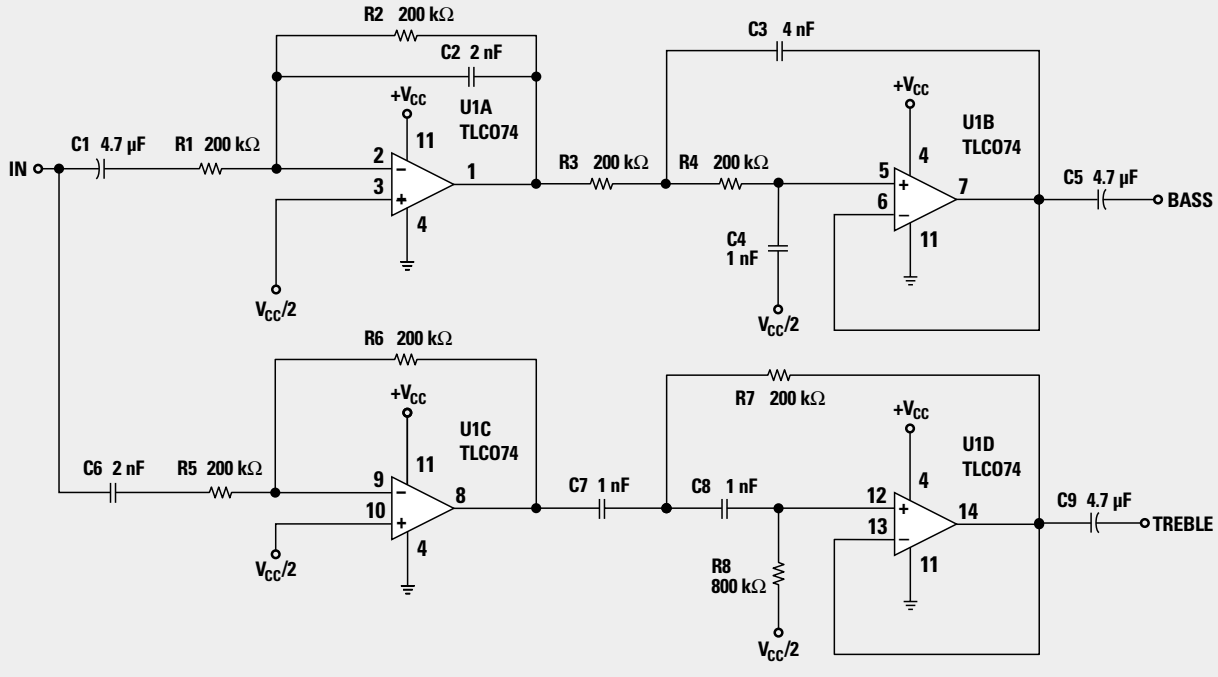
Figure 5. Crossover network



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the audio band. The result is that the listener uses tone controls or graphic equalizers to compensate for the human hearing curve to make the sound pleasing. This compensates to some degree for the differential power requirements, but most tone controls are limited to ±20 dB—not nearly enough to make up for human hearing sensitivity at really low or really high frequencies. Tone control characteristics are linear; even if they were devised with more gain, they still would not follow the human hearing curve. Graphic equalizers are limited to discrete frequency values and produce an unpleasant degree of ripple when several adjacent controls are turned up.

Human hearing is not sensitive to low frequencies, so more power is required to reproduce them at a level that can be heard. A high-power class "B" amplifier can drive a large bass woofer. Crossover notch distortion from the class "B" topology is inaudible at these frequencies, and the efficiency of the amplifier allows it to generate a lot of power with relatively little heat.

Hearing is most sensitive in the midrange frequencies, for which the best amplifier is a relatively low-power, very low-distortion, class "A" amplifier. As little as 10 watts can produce deafeningly loud audio in this frequency range.

But what about high frequencies? There are purists who would insist that high frequencies should be amplified the same way as low, so that the human ear could discern them as well. While this is technically true, there are some reasons why it is not desirable:

- The energy required to accelerate a speaker cone to a given displacement at 20 kHz is 1000 times that required to accelerate a speaker cone to that displacement at 20 Hz. There are some piezo- and ceramic-type tweeters that can produce high output levels, but they require correspondingly high amounts of energy to drive. These output levels are enough to shatter glass and eardrums.
- The spectral content of almost all music is weighted with a "pink" characteristic. Simply stated, there is much more middle- and low-frequency content than high-frequency content.
- Because there is not much high-frequency spectral content but a constant level of white noise throughout the spectrum, a lot of amplification in this range will increase audio perception of noise at high frequencies.

The crossover network shown in Figure 5 routes low (bass) frequencies to a woofer, and midrange and high frequencies (treble) to a tweeter. This is a very common application, because many speaker cabinets contain only a woofer and tweeter.

A crossover frequency of 400 Hz has been selected, which should suffice for the majority of applications. The filter sections are third-order, which will minimize energy to the wrong speakers.

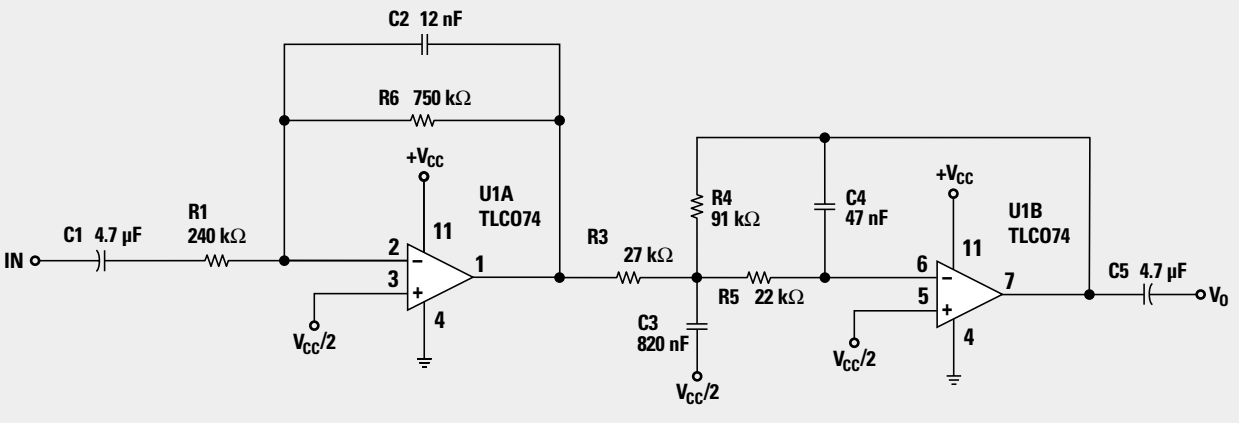
This circuit was designed to be very easy to build. The op amp sections can be interchanged, of course. There are only two capacitor values and one resistor value! Three 4.7-µF electrolytic capacitors are used for decoupling; they are sufficiently large to insure that they have no effect on the frequencies of interest. The 2-nF and 4-nF capacitors can be formed by connecting 1-nF capacitors in parallel. R8, the 800-k**Ω** resistor, can be made by connecting four 200-k**Ω** resistors in series.

A subwoofer section can be added to the crossover network in Figure 5 to enhance subsonic frequencies (see Figure 6).

Figure 6 shows a true subwoofer circuit. It will not work with 6- or 8-inch "subwoofers." It is for 15- to 18-inch woofers in a good infinite-baffle, bass-reflex, or folded-horn enclosure, driven by an amplifier with at least 100 watts. Most of the gain is below the range of human hearing; and these frequencies, when used in recorded material, are designed to be felt, not heard. The filter is designed to give 20 dB of gain to 13 Hz, rolling off to unity gain at about 40 Hz. There is no broadcast material in the United States that extends below 50 Hz; even most audio CDs do not go below 20 Hz. This will prove most useful for home theater applications, which play material that does have subsonic audio content. Examples are "Earthquake" and the dinosaur stomp in "Jurassic Park."

The combined response of the three circuits is shown in Figure 7. One active crossover network will be required per channel, with the exception of the subwoofer crossover.

Figure 6. Subwoofer circuit



There is no stereo separation of low bass frequencies, and either channel (or both) can be used to drive the subwoofer circuit (sum into an inverting input with a second C1 and R1).

Tone control

One rather unusual op amp circuit is the tone control circuit shown in Figure 8. It bears some superficial resemblance to the twin T circuit configuration, but it is not a twin T topology. It is actually a hybrid of one-pole, low-pass, and high-pass circuits with gain and attenuation.

The midrange frequency for the tone adjustments is 1 kHz. It gives about ±20 dB of boost and cut for bass and treble. The circuit is a minimum-component solution that limits cost. This circuit, unlike other similar circuits, uses linear instead of logarithmic pots. Two different potentiometer values are unavoidable, but the capacitors are the same value except for the coupling capacitor. The ideal capacitor value is 0.016 µF, which is an E-24 value; so the more common E-12 value of 0.015 µF is used instead. Even that value is a bit odd, but it is easier to find an oddball capacitor value than an oddball potentiometer value.

The plots in Figure 9 show the response of the circuit with the pots at the extremes and at the 1/4 and 3/4 positions. The middle position, although not shown, is flat to within a few millidecibels. The compromises involved in reducing circuit cost and in using linear potentiometers lead to some slight nonlinearities. The 1/4 and 3/4 positions are not exactly 10 and –10 dB, meaning that the pots are most sensitive towards the end of their travel. This may be preferable to the listener, giving a fine adjustment near the middle of the potentiometers and more rapid adjustment near the extreme positions. The center frequency shifts slightly, but this should be inaudible. The frequencies nearer the midrange are adjusted more rapidly than the frequency extremes, which also may be more desirable to the listener. A tone control is not a precision audio circuit, and therefore the listener may prefer these compromises.

Figure 7. Combined filter response

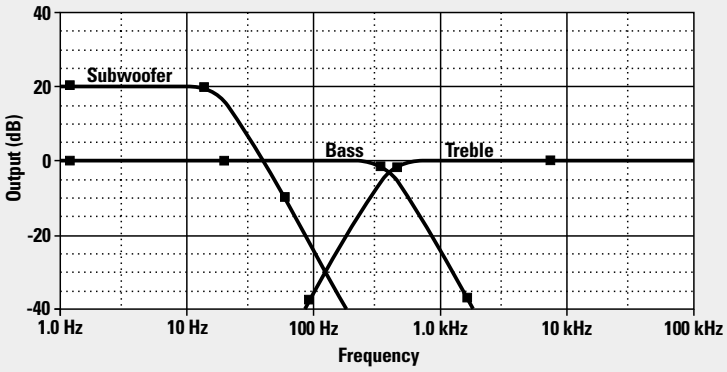


Figure 8. Tone control circuit

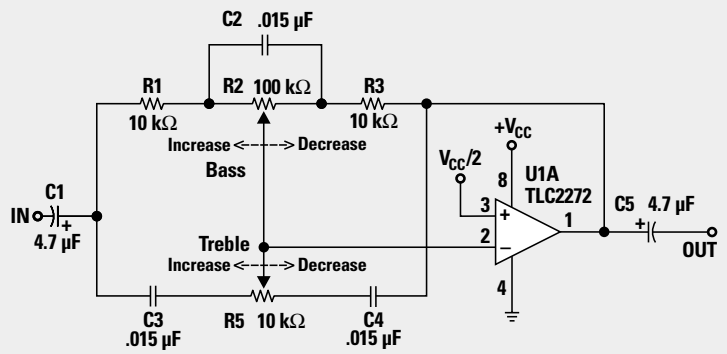
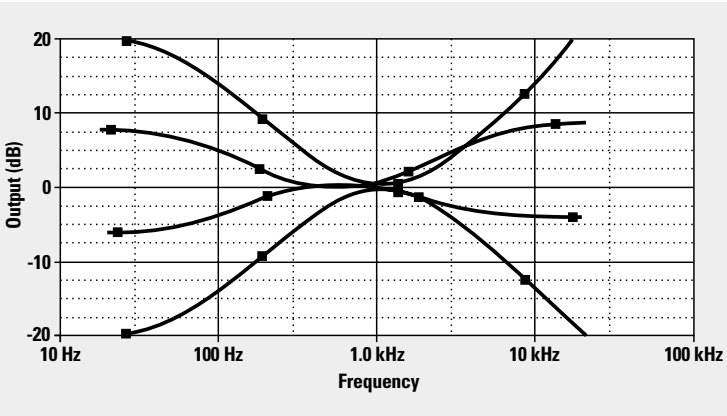


Figure 9. Circuit response with pots at the extremes



References

1. *Audio Circuits Using the NE5532/54*, Philips Semiconductor, Oct. 1984.
2. *Audio Radio Handbook*, National Semiconductor, 1980.
3. *Op Amp Circuit Collection*, National Semiconductor AN-031.

Related Web sites

www.ti.com/sc/docs/products/analog/*device*.html

Replace *device* with tlc074, tlc2272, tle2426, tlv2221, or tlv2464

www.ti.com/sc/docs/products/msp/amp_comp/default.htm

Thermistor temperature transducer-to-ADC application

By John Bishop
Applications Specialist, Advanced Analog Products/Op Amp Applications

Introduction

One of the applications of op amps is converting and conditioning signals from transducers into signals that other devices, including analog-to-digital converters (ADCs), can use. The reason any conversion or conditioning is necessary is that the range and offset of the transducer and the ADC are almost never the same.

A very inexpensive temperature transducer uses a diode whose forward-biased junction voltage changes with temperature. When higher repeatability between devices and/or better linearity is needed, other types of transducers, such as the interchangeable thermistor, should be considered.

This application uses an interchangeable negative temperature coefficient (NTC) thermistor device. Because NTC thermistor devices are inherently nonlinear, multiple vendors supply thermistors that contain more than one device, designed for a linear change of resistance with temperature. Since these thermistors are precisely calibrated, they can also be replaced by a part of the same type and still retain their accuracy—in other words, they are interchangeable.

Transducer information

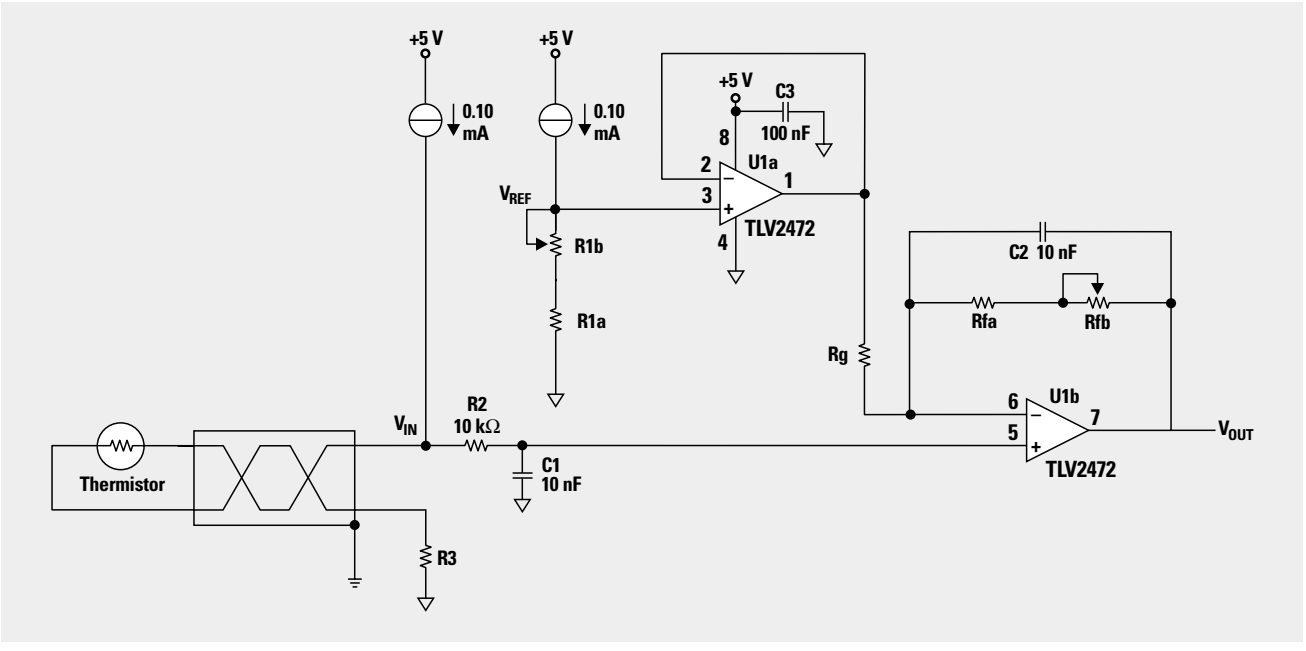
The sensor selected for this application is a thermistor with the part number ACC-004, manufactured by RTI. It has a resistance of 32,650 ohms at 0°C and 678.3 ohms at 100°C. This part's precision is ±0.2°C (from 0°C to 70°C), but parts are available at a lower cost when less accuracy is required. For instance, part number ACC-024 is a ±1°C part. The specifications for this and similar devices may be found at www.rtie.rti-corp.com/accurv.htm. Another manufacturer of similar devices is Alpha Sensors Inc. Their devices are introduced at www.alphasensors.com/interchange.html.

Current source information

A simple method of obtaining a voltage signal from a thermistor is to measure its resistance by connecting a dc power source through a resistor to the thermistor. The voltage developed across the device will be its resistance times the current through the device (Ohm's law). This method is flawed because the amount of current through the thermistor changes when its resistance changes. Another consideration when designing a thermistor circuit is that when too much current is delivered to the thermistor it "self heats," causing an error in the temperature measurement.

To overcome these errors, a regulated low current (100 µA) is supplied through a current regulator. The one chosen for this circuit is a Texas Instruments REF200. This device contains two current regulators and a current mirror (the current mirror will not be used). It is useful for configuring regulated current sources of varying magnitudes for many applications. A data sheet for this device can be found by searching for REF200 at www.ti.com.

Figure 1. Op amp circuit



One of the two current regulators supplies 100 µA ±0.5% to the thermistor. From resistance and current information, the thermistor voltage is 0.06783 V for 100°C and 3.265 V for 0°C.

Since any current used by the input of the amplifier affects the measured signal, an amplifier with high input impedance is necessary. The number of components in a circuit should be kept to a minimum, because each component that is added increases cost, circuit errors, and complexity. Since fewer components are required to make a noninverting amplifier with high input impedance than an inverting amplifier with high input impedance, the noninverting configuration was chosen. The output of the ADC will be fed into a digital signal processor (DSP) and inverted there if needed.

The other current source is used to establish the reference voltage in combination with R1 and U1a.

ADC information

Systems engineering selected the TLV2544 ADC for this application. The device is a single-supply unit with an analog input range of 0 to 5 V. The amplified sensor signal should completely fill this span. The voltage required to power this device is from a single 5-V supply. Other ADC devices could be used with corresponding changes in input range, resolution, and input impedance considerations. See "Related Web sites" at the end of this article to locate the data sheet for the TLV2544.

The TLV2544 is a 12-bit ADC, and the voltage value of each bit is calculated as 1.22 mV/bit:

$$\frac{\text{Input}}{\text{Resolution}} = \frac{5}{2^{12}-1} = 1.22\frac{\text{mV}}{\text{bit}}. \qquad \textbf{(1)}$$

Op amp choice

Since the analog input range for this ADC is 0 to 5 V and the power available is a single 5-V supply, a rail-to-rail output (RRO) device is required for best performance. The op amp chosen for this application, TI's TLV2472, will also be able to handle the full input range of the transducer because it is also a rail-to-rail input (RRI) device. See "Related Web sites" at the end of this article to locate the data sheet for this op amp.

In this application, the voltage supplied to the ADC is to be a single 5-V dc. The analog input of the ADC is 0 to 5 V. When a single supply is used, the output range will not quite be able to reach these limits, even on a rail-to-rail op amp. The high output voltage with a 2-kΩ load is 4.85 V minimum and 4.96 V nominal. The low output voltage with a 2-kΩ load is 150 mV maximum and 70 mV nominal. Because the actual load of the ADC is about 20 kΩ, the actual limits are likely to be better than the nominal limits. Using the nominal limits, the number of codes that will be sacrificed at the high output is .04/.00122 ≅ 33 bits and at the low output is .07/.00122 ≅ 57 bits, a total of 90 bits out of 4094 bits. It will allow each °C to be broken into 40 codes, which is much more resolution than the transducer's accuracy of ±0.2°C.

Basic equations

With the previous data, the gain of the circuit can be calculated by dividing the output voltage range by the input voltage range:

$$m = \frac{\text{Output}_{MAX} - \text{Output}_{MIN}}{R_{0°C}I_{SENSOR} - R_{100°C}I_{SENSOR}} = 1.564. \qquad \textbf{(2)}$$

Defining the circuit

Figure 1 is a schematic of the op amp circuit for this application.

The temperature of the thermistor is converted into a voltage that is increased by R3 and amplified by U1b. The resistor R3 is used because it allows for a higher reference voltage. This reference voltage is developed by R1 and buffered by U1a. This higher reference voltage causes the output to move closer to the negative rail at the 100°C point.

Op amp U1a is a unity gain amplifier whose output is the same voltage (but at a lower impedance) as its input. The nominal voltage for V_{REF} is 0.06783 (thermistor voltage at 100°C) plus V_{R3} (the resistance of R3 multiplied by 100 µA). With R3 set at 3.01 kΩ, V_{REF} is calculated as 0.406 V.

The basic voltage signals and resistors in Figure 1 are defined in Equations 3, 4, and 5.

The other op amp, U1b, is used to amplify and filter the signal from the thermistor. Equation 3 defines the gain of this op amp:

$$|m| = \frac{R_F}{R_G} + 1. \qquad \textbf{(3)}$$

Using the gain of 1.569 and letting R_G = 26.7 kΩ (a 1% value), we can calculate R_F in Equation 3 as 15.056 kΩ. The closest 1% value for R_F is 15 kΩ.

Using the equation for a basic voltage divider, we can calculate V_{REF} at a temperature of 100°C:

$$\frac{R_{100°C} - V_{REF} - I_{SENSOR}}{V_{REF} - \text{Output}_{100°C}} = \left(\frac{R_F + R_G}{R_G}\right). \qquad \textbf{(4)}$$

Substituting values for $R_{100°C}$, I_{SENSOR}, $\text{Output}_{100°C}$, R_G, and R_F into Equation 4 yields V_{REF} = 0.406 V. Using Ohm's law, we can calculate the value of R1:

$$R1 = \frac{V_{REF}}{I_{VREF}} = 4.59 \text{ kΩ (1\% resistor)}. \qquad \textbf{(5)}$$

Calibration devices

Because the temperature coefficient of potentiometers is higher (worse) than that of resistors, it is wise to replace R_1 and R_F with a potentiometer in series with a resistor. These parts are designated R_{1A} and R_{FA} for the fixed resistors and R_{FB} and R_{1B} for the potentiometers. In addition, when a fixed resistor is used in series with a potentiometer, adjustment is less critical.

Component values will drift as the components age. Therefore, when the values of R_F and R_1 are calculated, the life expectancy of the application should be taken into account.

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Long-life applications

Resistors designated to have 1% tolerance may drift about 3%. The current regulators, temperature sensor, and op amps will drift too. The resistances R_1 and R_F are 4020 Ω and 15 kΩ, respectively, but because of the drift in circuit components, they each must be able to absorb a total of ±9% (3% + 3% + 3%) drift. This is done in each case by using a fixed resistor for 91% of the resistance and a small pot to permit adjustment for the 9% drift. To ensure that the ability to compensate is always possible, the size of the pots is doubled. Gain is scaled with R_F and offset is zeroed with R_1 using the fixed and variable resistance values shown in Equations 6–9. The fixed resistors are selected to the nearest 1% values, and potentiometers to the next higher value:

$$R_{FA} = 0.91 \times R_F = 13.7\ k\Omega \text{ (1\% resistor)} \quad \textbf{(6)}$$

$$R_{FB} = 2 \times 0.09 \times R_F = 5\ k\Omega \text{ (Cermet potentiomenter)} \quad \textbf{(7)}$$

$$R_{1A} = 0.91 \times R_1 = 3.65\ k\Omega \text{ (1\% resistor)} \quad \textbf{(8)}$$

$$R_{1B} = 2 \times 0.09 \times R_1 = 1\ k\Omega \text{ (Cermet potentiomenter)} \quad \textbf{(9)}$$

Short-life applications

If the design life of the circuit is significantly shorter than the theoretical end-of-life of the devices, the tolerances of the devices themselves (±1%) can be used for the calculations. The reference diode, temperature sensor, and op amp will drift less as well. Allow 2% for errors not caused by resistors for a maximum total possible drift of ±4% (1% + 1% + 2%). Again, if gain is adjusted with R_F and offset with R_1, values for the new resistors and potentiometers can be calculated with Equations 10–13, where fixed resistors have been selected for the nearest 1% values, and the potentiometers for the next higher value:

$$R_{FA} = 0.96 \times R_F = 14.3\ k\Omega \text{ (1\% resistor selection)} \quad \textbf{(10)}$$

$$R_{FB} = 2 \times 0.04 \times R_F = 2\ k\Omega \text{ (Cermet potentiomenter)} \quad \textbf{(11)}$$

$$R_{1A} = 0.96 \times R_1 = 3.92\ k\Omega \text{ (1\% resistor selection)} \quad \textbf{(12)}$$

$$R_{1B} = 2 \times 0.04 \times R_1 = 500\ \Omega \text{ (Cermet potentiomenter)} \quad \textbf{(13)}$$

Calibration

To calibrate the circuit, a resistance decade box (or individual resistors or potentiometers) is connected in place of the thermistor. This calibration device is adjusted to the resistance corresponding to various temperatures. Calibration is done by adjusting first the gain and then the reference voltage. There is some interaction between these adjustments. Because both the lowest (0°C) and highest (100°C) temperatures in the range coincide with the power rail, the adjustments should be made at 5°C and 95°C. Linearity can be checked at 25°C , 50°C, and 75°C. Repeating this sequence provides verification of the calibration's precision.

Signal filtering

When a transducer is connected to an input, the wiring is subjected to noise signals because of the electrical and magnetic environment surrounding the transducer and wiring. To prevent this noise from interfering with the desired signals, some shielding is necessary. Using a twisted pair from the transducer to the conversion circuit and shielding this pair (grounding the shield only at the instrument) will reduce the noise.

Without an input filter, the op amp will act as a radio frequency detector, converting high-frequency signals from other devices into signals with low-frequency components. Placing a resistor and capacitor on the input forms a low-pass filter, preventing high-frequency signals from interfering with the temperature signal. The cutoff frequency of this filter is defined by

$$F_C = \frac{1}{2\pi RC}. \quad \textbf{(14)}$$

Using Equation 14, we know that if R_2 is 10 kΩ and C_1 = 10 nF, then F_C is about 1600 Hz.

Resistor R_F and capacitor C2, connected from the output of U1b to its noninverting input, cause the circuit to act as a low-pass filter. The purpose of this filter is to remove any further noise generated by the components in this circuit and low enough in frequency to get past the previous filter. An additional purpose is to remove any frequency near or above the sampling frequency of the ADC that will cause alias signals. The frequency response of this filter is also defined by Equation 14 to be 1060 Hz.

Decoupling

Power-supply decoupling is required to prevent the noise from the power supply from being coupled into the signal being amplified, and vice versa. This is accomplished using a 6.8-µF tantalum in parallel with a 100-nF ceramic capacitor on the supply rails. The tantalum capacitor may be shared between multiple packages, but one ceramic capacitor should be connected as close as possible (preferably within 0.1 inch) to each package.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "Understanding Basic Analog—Ideal Op Amps," Application Report	slaa068
2. "Single Supply Op Amp Design Techniques," Application Report	sloa030
3. "Active Low Pass Filter Design," Application Report	sloa049
4. "Application of Rail-To-Rail Operational Amplifiers," Application Report	sloa039
5. Ron Mancini, "Sensor to ADC—analog interface design," *Analog Applications Journal* (May 2000), pp. 22-25	slyt015

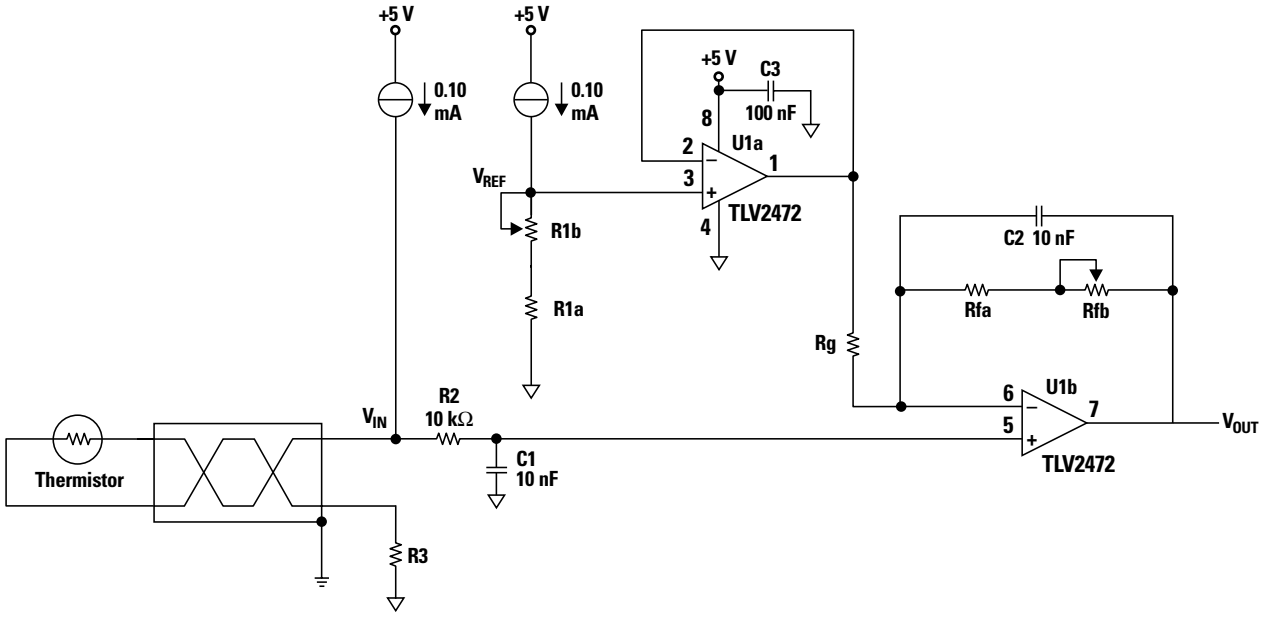
Related Web sites

www.rtie.rti-corp.com/accurv.htm
www.alphasensors.com/interchange.html
www.ti.com/sc/docs/products/analog/tlv2472a.html
www.ti.com/sc/docs/products/analog/tlv2544.html

For a complete op amp application index, see:
www.ti.com/sc/docs/apps/analog/operational_amplifiers.html

Appendix A. Calculations

The following summary shows values and equations used in this application note. Values in bold are calculated. All entered values are non-bold.



Given:

$R_{0°C}$ = 32650.0 ohms
$R_{100°C}$ = 678.3 ohms
I_{SENSOR} = 100.0 µA
$V_{0°C}$ = **3.26500** V
$V_{100°C}$ = **0.06783** V

$Output_{MAX}$ = 5 V
$Output_{MIN}$ = 0 V

	1%	
R_3 = 3000	**3010** ohms	V_{R3} = **0.301** V

$$m = \frac{Output_{MAX} - Output_{MIN}}{(R_{0°C} - R_{100°C})\, I_{SENSOR}}$$

m = **1.564**

Resistor values:

$m = R_F/R_G + 1$
$R_F = (m - 1)R_G$
$R_F = \mathbf{5.944}R_G$

Gain resistor values:

	1%
R_G = 27000	**26700** ohms
R_F = **15055.68**	**15000** ohms

At 100°C:

$$\frac{V_{REF} - V_{R3} - Output_{MIN}}{R_{100°C} \times I_{SENSOR}} = \frac{R_F + R_G}{R_G}$$

V_{REF} = **0.40594** V

$R1 = V_{REF}/I_{SENSOR}$

	1%
R1 = **4059**	**4020** ohms

End-of-life adjustment calculations

	1%	Pot.	
R_{1A} = **3694.0**	**3650**		ohms
R_{1B} = **730.7**		**1000**	ohms
R_{FA} = **13650**	**13700**		ohms
R_{FB} = **2700**		**5000**	ohms

Expendable adjustment calculations

	1%	Pot.	
R_{1A} = **3897**	**3920**		ohms
R_{1B} = **324.7**		**500**	ohms
R_{FA} = **14400**	**14300**		ohms
R_{FB} = **1200**		**2000**	ohms

C = 0.01 µF
$F_{IN} = 1/(2\pi R_I C)$ = **1592** Hz
$F_{Amp} = 1/(2\pi R_F C)$ = **1061** Hz

Analysis of fully differential amplifiers

By Jim Karki
Systems Specialist, High-Speed Amplifiers

Introduction

The August issue of *Analog Applications Journal* introduced the fully differential amplifiers from Texas Instruments and illustrated their basic operation (see Reference 1). This article explores the topic more deeply by analyzing gain and noise. The fully differential amplifier has multiple feedback paths, and circuit analysis requires close attention to detail. Care must be taken to include the V_{OCM} pin for a complete analysis.

Circuit analysis

Circuit analysis of fully differential amplifiers follows the same rules as normal single-ended amplifiers, but subtleties are present that may not be fully appreciated until a full analysis is done. The analysis circuit shown in Figure 1 is used to calculate a generalized circuit formula and block diagram from which specific circuit configurations can be easily solved. The voltage definitions are required to arrive at practical solutions.

A_F is used to represent the open-loop differential gain of the amplifier such that $(V_{OUT}+) - (V_{OUT}-) = A_F(V_P - V_N)$. This assumes that the gains of the two sides of the differential amplifier are well matched and that variations are insignificant. With negative feedback, this is typically the case when $A_F >> 1$.

Figure 1. Analysis circuit

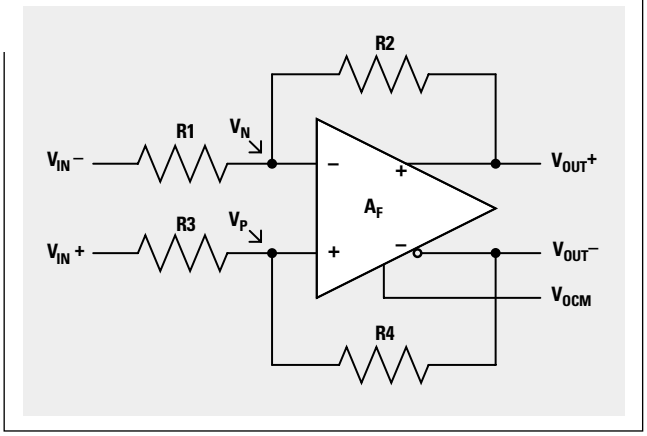
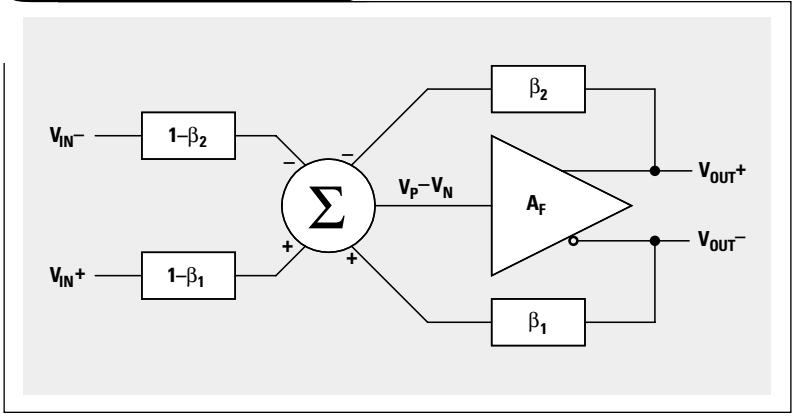


Figure 2. Block diagram



Input voltage definitions:

$$V_{ID} = (V_{IN}+) - (V_{IN}-) \quad \textbf{(1)}$$

$$V_{IC} = \frac{(V_{IN}+) + (V_{IN}-)}{2} \quad \textbf{(2)}$$

Output voltage definitions:

$$V_{OD} = (V_{OUT}+) - (V_{OUT}-) \quad \textbf{(3)}$$

$$V_{OC} = \frac{(V_{OUT}+) + (V_{OUT}-)}{2} \quad \textbf{(4)}$$

$$(V_{OUT}+) - (V_{OUT}-) = A_F(V_P - V_N) \quad \textbf{(5)}$$

$$V_{OC} = V_{OCM} \quad \textbf{(6)}$$

There are two amplifiers: the main differential amplifier (from V_{IN} to V_{OUT}) and the V_{OCM} error amplifier. The operation of the V_{OCM} error amplifier is the simpler of the two and will be considered first. It may help to review the simplified schematic shown in Reference 1.

$V_{OUT}+$ and $V_{OUT}-$ are filtered and summed by an internal RC network. The V_{OCM} amplifier samples this voltage and compares it to the voltage applied to the V_{OCM} pin. An internal feedback loop is used to drive "error" voltage of the V_{OCM} error amplifier (the voltage between the input pins) to zero, so that $V_{OC} = V_{OCM}$. This is the basis of the voltage definition given in Equation 6.

There is no simple way to analyze the main differential amplifier except to sit down and write some node equations, then do the algebra to massage them into practical form. We will first derive a solution based solely on nodal analysis. Then we will make use of the voltage definitions given in Equations 1–6 to derive solutions for the output voltages, looking at them single-ended; i.e., $V_{OUT}+$ and $V_{OUT}-$. These are then used to calculate V_{OD}.

Solving the node equations at V_N and V_P yields

$$V_N = (V_{IN}-)\left(\frac{R2}{R1+R2}\right)+(V_{OUT}+)\left(\frac{R1}{R1+R2}\right) \quad \text{and} \quad V_P = (V_{IN}+)\left(\frac{R4}{R3+R4}\right)+(V_{OUT}-)\left(\frac{R3}{R3+R4}\right).$$

By setting $\beta_1 = \left(\frac{R3}{R3+R4}\right)$ and $\beta_2 = \left(\frac{R1}{R1+R2}\right)$, V_N and V_P can be rewritten as

$$V_N = (V_{IN}-)(1-\beta_2)+(V_{OUT}+)(\beta_2), \text{ and} \tag{7}$$

$$V_P = (V_{IN}+)(1-\beta_1)+(V_{OUT}-)(\beta_1). \tag{8}$$

With Equations 7 and 8, a block diagram of the main differential amplifier can be constructed, like that shown in Figure 2. Block diagrams are useful tools for understanding circuit operation and investigating other variations.

By using the block diagram, or combining Equations 7 and 8 with Equation 5, we can find the input-to-output relationship:

$$(V_{OUT}+)(1+A_F\beta_2)-(V_{OUT}-)(1+A_F\beta_1)=A_F[(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)]. \tag{9}$$

Although accurate, Equation 9 is somewhat cumbersome when the feedback paths are not symmetrical. By using the voltage definitions given in Equations 1–4 and Equation 6, we can derive more practical formulas.

Substituting $(V_{OUT}-) = 2V_{OC} - (V_{OUT}+)$, and $V_{OC} = V_{OCM}$, we can write

$$(V_{OUT}+)(2+A_F\beta_1+A_F\beta_2)-2V_{OCM}(1+A_F\beta_1)=A_F[(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)], \text{ or}$$

$$(V_{OUT}+)=\frac{1}{(\beta_1+\beta_2)}\frac{(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)+2V_{OCM}\left(\frac{1}{A_F}+\beta_1\right)}{\left(1+\frac{2}{A_F\beta_1+A_F\beta_2}\right)}. \tag{10}$$

With the "ideal" assumption $A_F\beta_1 >> 1$ and $A_F\beta_2 >> 1$, this reduces to

$$(V_{OUT}+)=\frac{(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)+2V_{OCM}\beta_1}{(\beta_1+\beta_2)}. \tag{11}$$

$V_{OUT}-$ is derived in a similar manner:

$$(V_{OUT}-)=\frac{1}{(\beta_1+\beta_2)}\frac{-(V_{IN}+)(1-\beta_1)+(V_{IN}-)(1-\beta_2)+2V_{OCM}\left(\frac{1}{A_F}+\beta_2\right)}{\left(1+\frac{2}{A_F\beta_1+A_F\beta_2}\right)}. \tag{12}$$

Again, assuming $A_F\beta_1 >> 1$ and $A_F\beta_2 >> 1$, this reduces to

$$(V_{OUT}-)=\frac{-(V_{IN}+)(1-\beta_1)+(V_{IN}-)(1-\beta_2)+2V_{OCM}(+\beta_2)}{(\beta_1+\beta_2)}. \tag{13}$$

To calculate $V_{OD} = (V_{OUT}+) - (V_{OUT}-)$, subtract Equation 12 from Equation 10:

$$V_{OD}=\frac{1}{(\beta_1+\beta_2)}\frac{2[(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)]+2V_{OCM}(\beta_1-\beta_2)}{\left(1+\frac{2}{A_F\beta_1+A_F\beta_2}\right)} \tag{14}$$

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Again, assuming $A_F\beta_1 >> 1$ and $A_F\beta_2 >> 1$, this reduces to

$$V_{OD} = \frac{2[(V_{IN}+)(1-\beta_1)-(V_{IN}-)(1-\beta_2)]+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)}. \quad \textbf{(15)}$$

It can be seen from Equations 11, 13, and 15 that even though the obvious use of a fully differential amplifier is with symmetrical feedback, the gain can be controlled with only one feedback path.

Using matched resistors R1 = R3 and R2 = R4 in the analysis circuit of Figure 1 balances the feedback paths so that $\beta_1 = \beta_2 = \beta$, and the transfer function is

$$\frac{(V_{OUT}+)-(V_{OUT}-)}{(V_{IN}+)-(V_{IN}-)} = \frac{A_F}{(1+A_F\beta)} = \frac{1-\beta}{\beta} \times \frac{1}{\left(1+\frac{1}{A_F\beta}\right)}.$$

The common-mode voltages at the input and output do not enter into the equation, V_{IC} is rejected, and V_{OC} is set by the voltage at V_{OCM}. The ideal gain (assuming $A_F\beta >> 1$) is set by the ratio

$$\frac{1-\beta}{\beta} = \frac{R2}{R1}.$$

Note that the normal inversion we might expect, given two balanced inverting amplifiers, is accounted for by the output voltage definitions, resulting in a positive gain.

Many applications require that a single-ended signal be converted to a differential signal. The circuits in Figures 3–7 show various approaches. Using Equations 11, 13, and 15, we can easily derive circuit solutions.

With a slight variation of Figure 1 as shown in Figure 3, single-ended signals can be amplified and converted to differential signals. $V_{IN}-$ is now grounded and the signal is applied to $V_{IN}+$. Substituting $V_{IN}- = 0$ in Equations 11, 13, and 15 results in

$$(V_{OUT}+) = \frac{(V_{IN}+)(1-\beta_1)+2V_{OCM}\beta_1}{(\beta_1+\beta_2)},$$

$$(V_{OUT}-) = \frac{2V_{OCM}\beta_2-(V_{IN}+)(1-\beta_1)}{(\beta_1+\beta_2)}, \quad \text{and}$$

$$V_{OD} = \frac{2(V_{IN}+)(1-\beta_1)+2V_{OCM}(\beta_1-\beta_2)}{(\beta_1+\beta_2)}.$$

If the signal is not referenced to ground, the reference voltage will be amplified along with the desired signal, reducing the dynamic range of the amplifier. To strip unwanted dc offsets, use a capacitor to couple the signal to $V_{IN}+$. Keeping $\beta_1 = \beta_2$ will prevent V_{OCM} from causing an offset in V_{OD}.

The circuits in Figures 4–7 have nonsymmetrical feedback. This causes V_{OCM} to influence $V_{OUT}+$ and $V_{OUT}-$ differently, making V_{OCM} show up in V_{OD}. This will change the operating points between the internal nodes in the

Figure 3. Single-ended to differential amplifier

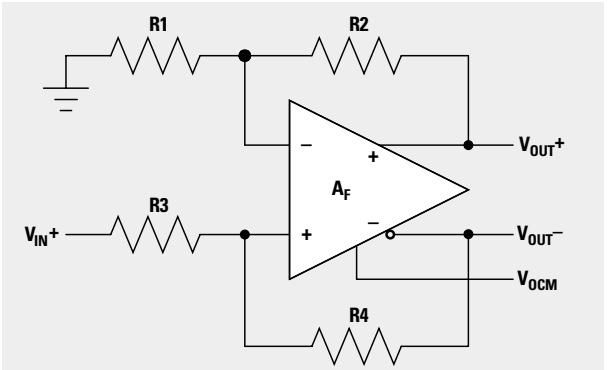


Figure 4. $\beta_1 = 0$

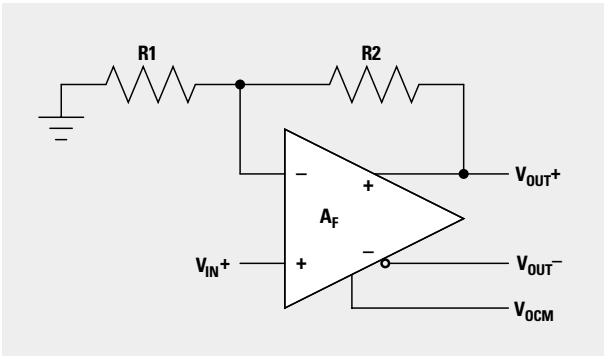


Figure 5. $\beta_2 = 0$

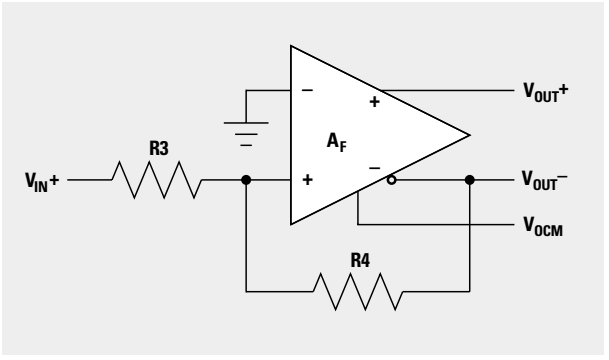


Figure 6. $\beta_2 = 1$

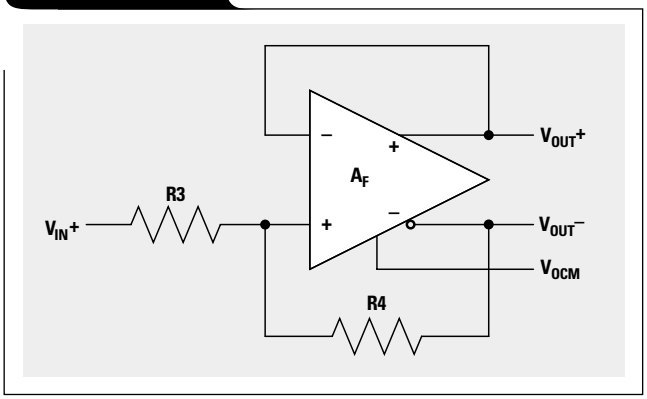
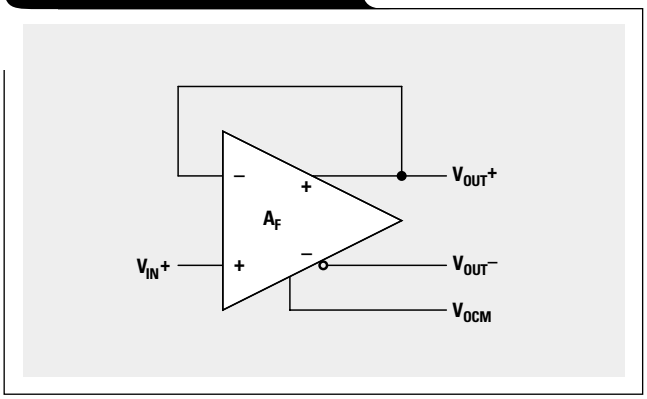


Figure 7. $\beta_1 = 0$, and $\beta_2 = 1$



differential amplifier, and matching of the open-loop gains will degrade. CMRR is not a real issue with single-ended inputs, but the analysis points out that CMRR is severely compromised when nonsymmetrical feedback is used. In the discussion of noise analysis that follows, it is shown that nonsymmetrical feedback also increases noise introduced at the V_{OCM} pin. For these reasons, even though the circuits shown in Figures 4–7 have been tested to prove they work in accordance with the equations given, they are presented mainly for instructional purposes. They are not recommended without extensive lab testing to prove their worthiness in your application.

In the circuit shown in Figure 4, $V_{IN}- = 0$ and $\beta_1 = 0$. The output voltages are

$$(V_{OUT}+) = \frac{(V_{IN}+)}{\beta_2},$$

$$(V_{OUT}-) = 2V_{OCM} - \frac{(V_{IN}+)}{\beta_2}, \quad \text{and}$$

$$V_{OD} = \frac{2(V_{IN}+)}{\beta_2} - 2V_{OCM}.$$

With $\beta_1 = 0$, this circuit is similar to a noninverting amplifier.

In the circuit shown in Figure 5, $V_{IN}- = 0$ and $\beta_2 = 0$. The output voltages are

$$(V_{OUT}+) = \frac{(V_{IN}+)(1-\beta_1)}{\beta_1} + 2V_{OCM},$$

$$(V_{OUT}-) = \frac{-(V_{IN}+)(1-\beta_1)}{\beta_1}, \quad \text{and}$$

$$V_{OD} = \frac{2(V_{IN}+)(1-\beta_1)}{\beta_1} + 2V_{OCM}.$$

With $\beta_2 = 0$, the gain is twice that of an inverting amplifier (without the minus sign).

In the circuit shown in Figure 6, $V_{IN}- = 0$ and $\beta_2 = 1$. The output voltages are

$$(V_{OUT}+) = \frac{(V_{IN}+)(1-\beta_1) + 2V_{OCM}\beta_1}{\beta_1 + 1},$$

$$(V_{OUT}-) = \frac{2V_{OCM} - (V_{IN}+)(1-\beta_1)}{\beta_1 + 1}, \text{ and}$$

$$V_{OD} = \frac{2(V_{IN}+)(1-\beta_1) + 2V_{OCM}(\beta_1 - 1)}{(\beta_1 + 1)}.$$

The gain is 1 with $\beta_1 = 0.333$; or, with $\beta_1 = 0.6$, the gain is 1/2.

In the circuit shown in Figure 6, $V_{IN}- = 0$, $\beta_1 = 0$, and $\beta_2 = 1$. The output voltages are

$$(V_{OUT}+) = (V_{IN}+), \quad (V_{OUT}-) = 2V_{OCM} - (V_{IN}+),$$

and $\quad V_{OD} = 2[(V_{IN}+) - V_{OCM}]$.

This circuit realizes a gain of 2 with no resistor.

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Noise analysis

The noise sources are identified in Figure 8, which will be used for analysis with the following definitions.

E_{IN} is the input-referred RMS noise voltage of the amplifier: $E_{IN} \approx e_{IN} \times \sqrt{ENB}$ (assuming the 1/f noise is negligible), where e_{IN} is the input white noise spectral density in volts per square root of the frequency in Hertz, and ENB is the effective noise bandwidth. E_{IN} is modeled as a differential voltage at the input.

$I_{IN}+$ and $I_{IN}-$ are the input-referred RMS noise currents that flow into each input. They are taken as equal and called I_{IN}. $I_{IN} \approx i_{IN} \times \sqrt{ENB}$ (assuming the 1/f noise is negligible), where i_{IN} is the input white noise spectral density in amps per square root of the frequency in Hertz, and ENB is the effective noise bandwidth. I_{IN} develops a voltage in proportion to the equivalent input impedance seen from the input nodes. Assume the equivalent input impedance is dominated by the parallel combination of the gain setting resistors:

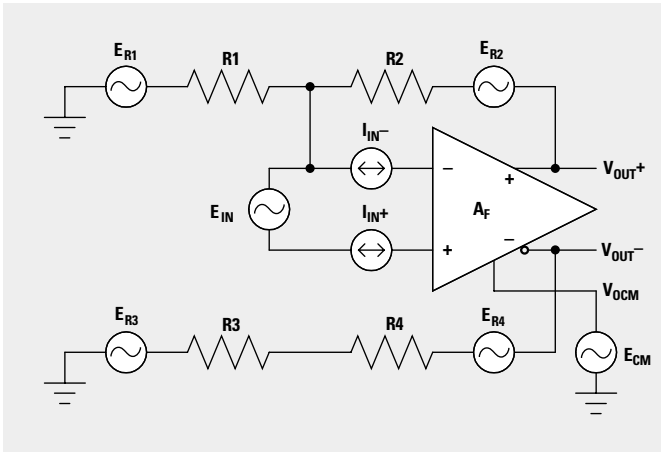
$$R_{EQ1} = \frac{R1R2}{R1+R2} \quad \text{and} \quad R_{EQ2} = \frac{R3R4}{R3+R4}.$$

E_{CM} is the RMS noise at the V_{OCM} pin, taking into account the spectral density and bandwidth as with the input-referred noise sources.

Noise current into the V_{OCM} pin will develop a noise voltage across the impedance seen from the node. It is assumed that proper bypassing of the V_{OCM} pin is done to reduce the effective bandwidth, so this voltage is negligible. If this is not the case, the added noise should be added to E_{CM} in a similar manner, as shown below.

E_{R1} through E_{R4} are the RMS noise voltages from the resistors, calculated by $E_{Rn} = \sqrt{4kTR \times ENB}$, where n is the resistor number, k is Boltzmann's constant (1.38×10^{-23}j/K), T is the absolute temperature in Kelvin (K), R is the resistance in ohms (Ω), and ENB is the effective noise bandwidth.

Figure 8. Noise analysis circuit



E_{OD} is the differential RMS output noise voltage. $E_{OD} = A(E_{ID})$, where E_{ID} is the input noise source, and A is the gain from the source to the output. Half of E_{OD} is attributed to the positive output ($+E_{OD}/2$), and half is attributed to the negative output ($-E_{OD}/2$). Therefore, ($+E_{OD}/2$) and ($-E_{OD}/2$) are correlated to one another and to the input source, and can be directly added together; i.e.,

$$\left(\frac{+E_{OD}}{2}\right) - \left(\frac{-E_{OD}}{2}\right) = E_{OD} = A(E_{ID}).$$

Independent noise sources typically are not correlated. To combine noncorrelated noise voltages, a sum-of-squares technique is used. The total RMS voltage squared is equal to the square of the individual RMS voltages added together. The output noise voltages from the individual noise sources are calculated one at a time and then combined in this fashion.

The block diagram shown in Figure 9 helps in analyzing the amplifier's noise sources.

Considering only E_{IN}, from the block diagram we can write:

$$E_{OD} = A_F\left[E_{IN} + \frac{(-E_{OD})\beta_1}{2} - \frac{(+E_{OD})\beta_2}{2}\right].$$

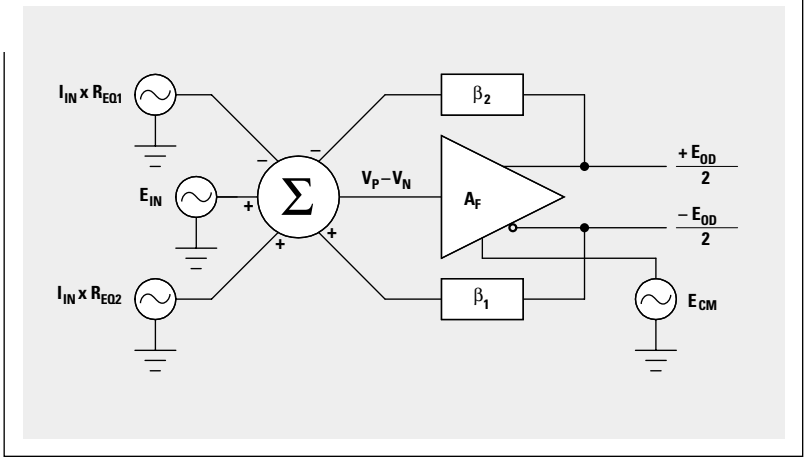
Solving yields

$$E_{OD} = \left(\frac{2E_{IN}}{\beta_1+\beta_2}\right)\left(\frac{1}{1+\frac{2}{A_F(\beta_1+\beta_2)}}\right).$$

Assuming $A_F\beta_1 >> 1$ and $A_F\beta_2 >> 1$,

$$E_{OD} = \frac{2E_{IN}}{(\beta_1+\beta_2)}.$$

Figure 9. Block diagram of the amplifier's input-referred noise



Given $\beta_1 = \beta_2 = \beta$ (symmetrical feedback),

$$E_{OUT} = \frac{E_{IN}}{\beta},$$

the same as a standard single-ended voltage feedback op amp.

Similarly, the noise contributions from $I_{IN} \times R_{EQ1}$ and $I_{IN} \times R_{EQ2}$ will be

$$\frac{2I_{IN} \times R_{EQ1}}{(\beta_1 + \beta_2)} \quad \text{and} \quad \frac{2I_{IN} \times R_{EQ2}}{(\beta_1 + \beta_2)}, \text{ respectively.}$$

The V_{OCM} error amplifier will produce a common-mode noise voltage at the output equal to E_{CM}. Due to the feedback paths, β_1 and β_2, a noise voltage is seen at the input that is equal to $E_{CM}(\beta_1 - \beta_2)$. This is amplified, just as an input, and seen at the output as a differential noise voltage equal to

$$\frac{2E_{CM}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2)}.$$

Noise gain from the V_{OCM} pin ranges from 0 (given $\beta_1 = \beta_2$) to a maximum absolute value of 2 (given $\beta_1 = 1$ and $\beta_2 = 0$, or $\beta_1 = 0$ and $\beta_2 = 1$).

Noise from resistors R1 and R3 appears like signals at $V_{IN}+$ and $V_{IN}-$ in Figure 1. From the circuit analysis presented earlier, the differential output noise contribution is

$$\frac{2(E_{R1})(1-\beta_2)}{(\beta_1 + \beta_2)} \quad \text{and} \quad \frac{2(E_{R3})(1-\beta_1)}{(\beta_1 + \beta_2)}$$

for each resistor respectively.

Noise from resistors R2 and R4 (E_{R2} and E_{R4}, respectively) is imposed directly on the output with no amplification.

Adding the individual noise sources yields the total output differential noise:

$$E_{OD} = \sqrt{\frac{(2E_{IN})^2 + (2I_{IN} \times R_{EQ1})^2 + (2I_{IN} \times R_{EQ2})^2 + [2E_{CM}(\beta_1 - \beta_2)]^2 + [2(E_{R1})(1-\beta_2)]^2 + [2(E_{R3})(1-\beta_1)]^2}{(\beta_1 + \beta_2)^2} + E_{R2}{}^2 + E_{R4}{}^2}.$$

The individual noise sources are added in sum-of-squares fashion. Input-referred terms are amplified by the noise gain of the circuit:

$$G_n = \frac{2}{\beta_1 + \beta_2}.$$

If symmetrical feedback is used where $\beta_1 = \beta_2 = \beta$, the noise gain is

$$G_n = \frac{1}{\beta} = 1 + \frac{R_F}{R_G},$$

where R_F is the feedback resistor and R_G is the input resistor, the same as a standard single-ended voltage feedback amplifier.

Reference

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Jim Karki, "Fully differential amplifiers," *Analog Applications Journal* (August 2000), pp. 38-41	slyt018

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