Analog and Mixed-Signal Products

Analog Applications Journal

July 2001

SLYT027

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Signal Conditioning (High-Speed Op Amps, Audio Amplifiers)

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

A/D and D/A conversion of PC graphics and component video signals, Part 2: Software and control

By Bart DeCanne
Systems/Applications & Strategic Marketing—Digital Video Products

Introduction

The first article of this two-part series, published in the February 2001 issue of *Analog Applications Journal*, discussed the THS8083EVM hardware, a TI evaluation module featuring the THS8083 (a triple 8-bit high-speed ADC with integrated PLL for component video and PC graphics digitizing) and the THS8134 (a triple 8-bit video DAC). Having presented an overview of the features and EVM block diagram in the earlier article, we now turn our attention to the design of the complex programmable logic device (CPLD) on the EVM and the design of the PC-user software.

First we will describe the overall functionality of the CPLD, which operates in combination with the THS8083 to enable the display of a digitized PC graphics or video signal on an LCD flat-panel display connected to the board. Then we will focus on the implementation of the communication protocol between the PC and the EVM that eliminates the need for a microcontroller and therefore is more generally applicable as a methodology for rapid hardware prototyping. We will illustrate some of the EVM and THS8083 features using the PC software graphical user interface (GUI); and, in particular, we will implement an algorithm for white-balance calibration.

CPLD design

While the THS8083 is a contained solution for the digitizing of a PC graphics or component video signal, it does not include the circuitry to generate the synchronization signals for the digital display. In this example, we use a Sharp XGA flat panel that accepts 6-bit R, G, and B data (using the 6 MSBs of each 8-bit bus) over a double-pixel interface bus. Additionally this requires Hsync, Vsync, and Data Enable signals. While the THS8083 does provide an output Hsync, we like to have the option of centering the image, a standard feature on any LCD or CRT computer monitor. This is accomplished by changing the timing of the sync signals with respect to the active video data by feeding both Hsync (from the THS8083 or from the input video signal) and Vsync (from the video input) to the CPLD, where they are used as references to, respectively, a horizontal (pixel) and vertical (line) counter. The horizontal counter is reset by each Hsync and increments with the sample (pixel) clock; the vertical counter is incremented by Hsync and reset by Vsync.

The EVM provides digital output from the ADC to the flat-panel display as well as analog output from a back-to-back connection of ADC and DAC to a computer CRT monitor. To provide image centering on both displays, the CPLD generates two sets of syncs that can be independently controlled. A third set of output sync signals from the CPLD is routed to the THS8083 for test purposes. When these signals are selected via board jumpers, it is possible to use them instead of an external video source for synchronizing the THS8083.

The user can program start and stop values for each set of sync signals (and the data_enable signals for the digital LCD output) in units of pixels (for the horizontal dimension) or lines (for the vertical dimension). Additionally, the polarity of the sync signals is programmable. The programmable logic generates these signals by comparing the programmed start/stop values with the current state of the pixel and line counters.

Note that the data output of the THS8083 is not routed through the CPLD, and therefore it is not possible to implement on-screen display (OSD), image data capture, or other video processing in the digital data path on this board.

The THS8134 DAC can be configured in different modes, depending on the desired color space (RGB vs. YPbPr) and sync insertion features. There are also dedicated inputs to this device to control the timing of the sync insertion. The programmability of these signals is register-controlled through the CPLD.

The CPLD itself is configured via an I^2C interface. The CPLD design contains a full I^2C slave implementation with writeable and readable configuration registers. Since it is only an I^2C slave, the CPLD can respond only to data transfer requests initiated by the host (PC).

Reference 1 fully details the CPLD design. The design was accomplished using schematic entry and, for some functional blocks, via a behavioral description in Altera® High Level Description Language (AHDL). The complete design was compiled with Max+Plus II® version 9.6 and was fitted into an Altera Flex10K30 device, occupying its manufacturer-stated 30K gate capacity for about 50%.

Serial communication interface

Since there is no need for real-time communication between any of the devices on this board outside the video data path, there is no need for a microcontroller in this design. The control communication is only for configuration and status reporting between the PC and EVM and therefore can be run at low speed. We chose to implement a standard I^2C* interface directly onto the PC parallel port.

The I^2C interface consists of bidirectional data (SDA) and clock (SCL) lines, which have been implemented with two terminals of the standard PC LPT1 port's 25-pin connector.

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*The I^2C (inter-IC) communication bus is an industry-standard control bus and specifies a 2-wire physical interface that is shared by I^2C-compatible devices. The bus protocol is widely used for consumer video ICs. See Reference 2 for specifications.

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Figure 1 shows the bidirectional communication. The I^2C bus is an open-collector type (to enable a wired-AND operation inherent to the bus specification) and requires the use of open-collector buffer inverters to transform the unidirectional LPT1 port communication into bidirectional communication on the EVM.

On the THS8083EVM, both the THS8083 and the CPLD are slave devices connected to the (SCL1,SDA1) bus. The second I^2C bus is unused on this EVM but was provided to control other boards from the same host PC (via an extension connector) in the future.

THS8083EVM PC software

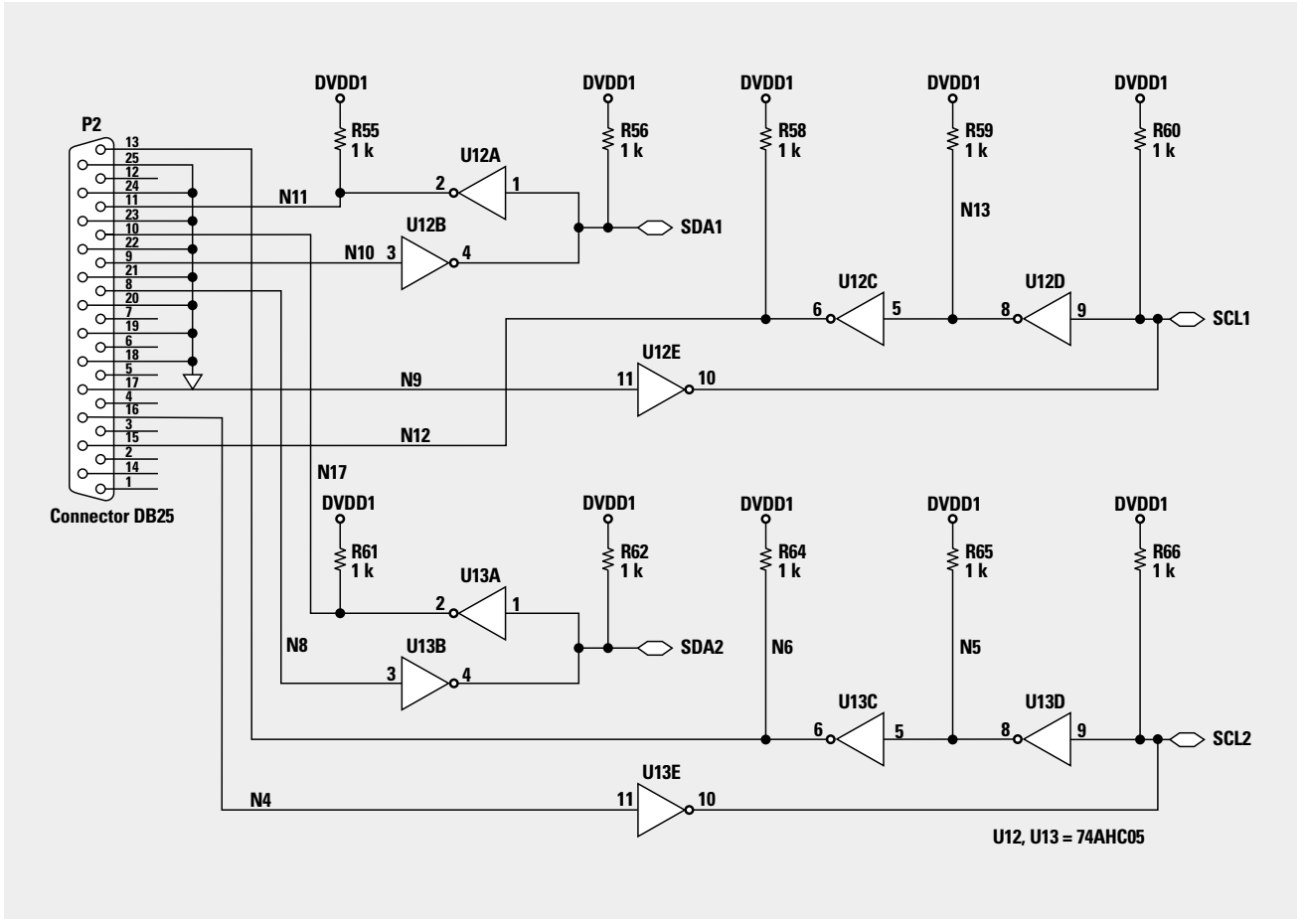
The PC software consists of a (shareware) parallel-port driver and the THS8083EVM graphical user interface (GUI).

Before the EVM can be used, the port driver needs to be installed. This will set up a Windows™ dynamic link library (DLL) that enables data I/O on LPT1 under both Windows 98 and Windows NT™ platforms. Once installed, this DLL is called transparently by the EVM's GUI.

As shown in Figure 2, the user interface is implemented as a property sheet, or tabbed dialog box, that groups logically related controls on the same page. For each video mode, a set of default settings can be selected via the "combo" box in the lower left of the main window. The user can change and re-save these defaults to disk for later use. Furthermore, each individual setting can be changed with the high-level controls on the different property pages. The I^2C register map of the THS8083 and/or the CPLD, as shown in Figure 2, immediately adapts to the new setting. Which device implements each software function is transparent to the user. The software keeps track of changes versus the previous device settings and will update only those registers that have been affected.

Additional control buttons are available for checking the I^2C status (a data pattern is written to and read from each I^2C device and compared for equality) or for the retrieval of settings currently loaded in the devices. Furthermore, using an automatic PC interrupt invoked by the GUI, the software automatically polls the I^2C bus every 3 seconds for status indicators such as the availability of an input video signal or lock of the PLL in the THS8083 to this

Figure 1. Implementing two independent I^2C buses on a standard PC parallel port



input signal. The main page also displays readouts from the THS8083 for the pixel clock frequency and the frequencies of HSync (line rate) and Vsync (frame rate). They are continuously updated through this polling function and thus can be used, e.g., for the detection of an input video format change.

Instead of programming the devices from this high level, an expert user can control each register setting on the Register Map page individually for both the CPLD (controller) and the THS8083 by changing individual register bytes in decimal or hexadecimal format, as shown in Figure 2.

Once a setting is changed, the Apply button becomes active. When it is pressed, the new settings are downloaded onto the EVM.**

White-balance calibration

Besides programming the device, the user software implements an offset and gain calibration algorithm for the R, G, and B channels to ensure white balance in the digital output. When the button at the top of the page in Figure 3 is pressed, the software will first create a full-screen almost-black (R=G=B=32) and afterwards a full-screen almost-white (R=G=B=240) image to establish two points of reference. The black image will be used to establish equal offset on all channels and to create an offset-correction factor expressed as a value in the 0 to 255 range (a value of 128 on all channels means no correction). Similarly, the white image will compensate for any gain error by means of a gain-correction factor. For this procedure to work, the same PC must be used both for controlling the EVM via its LPT1 port and for video input.

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Figure 2. THS8083EVM PC software Register Map page

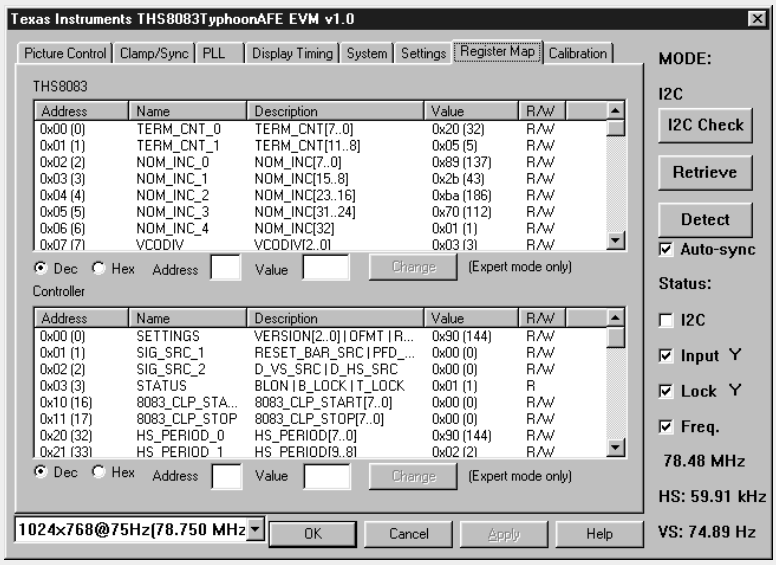
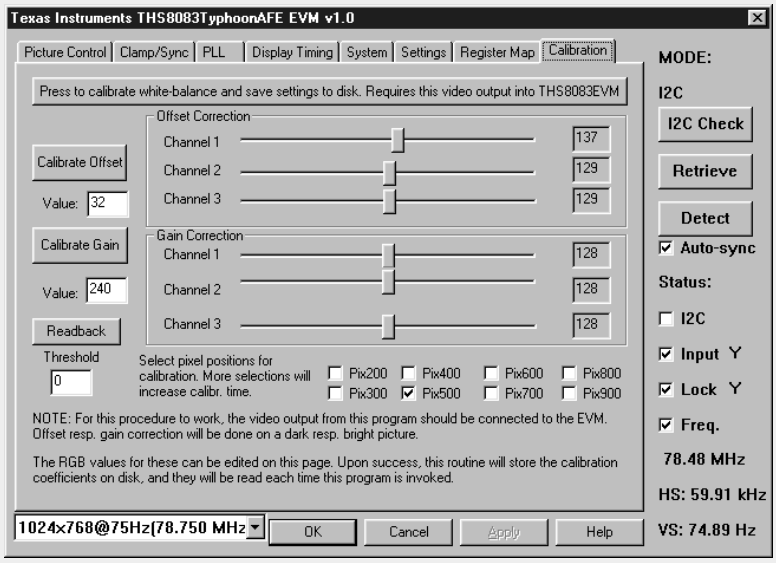


Figure 3. THS8083EVM PC software Calibration page



**Some selected settings, such as brightness/contrast control and the PLL phase setting, are updated as soon as they are changed in the software.

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Although the board does not have any provision for data capture as explained before, the THS8083 itself can read back the ADC output values on all three channels via dedicated I^2C registers. The user can program which horizontal location is used for readback. As shown in Figure 3, the default horizontal position for calibration is pixel 500 with respect to the Hsync, which will keep this position out of the horizontal blanking range for most video formats. More positions can be selected (pixel averages will be used) at the expense of a longer calibration time. Once calibration-correction factors are determined, they are taken into account automatically whenever the user changes brightness or contrast settings, so that white balance is preserved. The correction factors are also saved to disk and automatically loaded the next time the software is started, eliminating the need for re-calibration. More details, including the formula to determine corrected brightness/contrast settings, are given in Reference 1.

Conclusion

While this software control has been specifically designed for the THS8083EVM, its implementation of an I^2C interface from a standard PC parallel port is more widely applicable and can be of use for rapid prototyping in lab environments where there is no need for real-time host communication through a microcontroller. We have shown that a standard I^2C slave interface can be easily implemented in a CPLD, which opens up many possibilities for adding features to a prototype board via only software changes, by simply adding additional I^2C register map settings. For internal use, TI developed a derivative of this board—a board that routes the video data through a programmable device of larger density and pinout—and uses this to prototype image processing algorithms. We have also shown how one of the differentiated features of the THS8083—i.e., the ADC readback—can be used to implement a useful video algorithm.

References

1. THS8083EVM User Manual (furnished with THS8083 EVM kit).
2. "I^2C-bus specification (version 2.0)," Philips Semiconductors (December 1998).

Related Web sites

www.dataconverter.com

Get more product information at:
www.ti.com/sc/device/ths8083
www.ti.com/sc/ths8083evm
www.ti.com/sc/device/ths8134

Power supply solution for DDR bus termination

By Robert Kollman, *Senior Applications Manager, Power Management*
John Betten, *Applications Engineer, Power Management*
and Bang S. Lee, *Application Specialist, Power Management*

Introduction

Power dissipation in CMOS logic systems is related to the clock frequency, the input capacitance of the various gates within the system, and the supply voltage. As device feature sizes, and hence supply voltages, have been reduced, significant gains have been made in lowering system power dissipation. Reduced dissipation and higher operating speeds of these lower-voltage devices have allowed system clock frequencies to be pushed into the hundreds of megahertz. At these very high clock frequencies, clock distribution changes from the digital world back into the analog world. Controlled impedances, properly terminated buses, and minimal cross-coupling provide a high-fidelity clock signal. Traditionally, logic systems have been designed to clock data on only one edge of the clock, while the new double data rate (DDR) memories clock on both the leading and falling edges of the clock. This doubles the data rate while slightly increasing system power dissipation.

The increased data rate requires that the clock distribution network be carefully designed to minimize ringing and reflections that can inadvertently clock logic devices. Two possible bus termination schemes are presented in Figure 1. In Figure 1a, bus termination resistors are placed at the end of the distribution network and are connected to ground. If the bus driver is in the low state, the resistors have zero dissipation. In the high state, the resistors dissipate power equal to the supply voltage (V_{DD}) squared divided by the bus resistance. With a random voltage on the bus, the average loss is the supply voltage squared divided by twice the bus resistance. In Figure 1b, the termination resistor is connected to a supply voltage (V_{TT}) that is one-half the V_{DD} voltage. The dissipation in the termination resistor is then constant regardless of the supply voltage and is equal to V_{TT} [or (V_{DD}/2)] squared divided by the termination resistance. This results in a factor of two power savings when compared with the first approach (in case a bus signal is high 50% of the time and low 50% of the time), but at the cost of an additional power supply. The requirements of this power supply are a little unique. First, its output needs to be one-half the driver voltage (V_{DD}). Second, it needs to both source and sink current. When the driver output voltage is low, current flows from the V_{TT} supply into the driver. However, when the driver is high, current flows from the driver into the supply. Third, the supply needs to go from either operating mode into the other mode as the system data changes.

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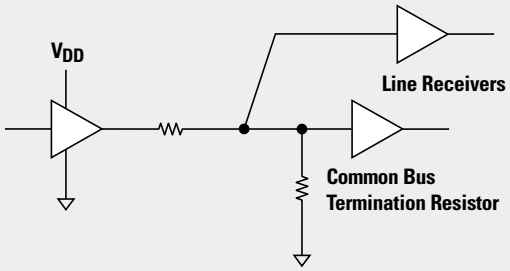
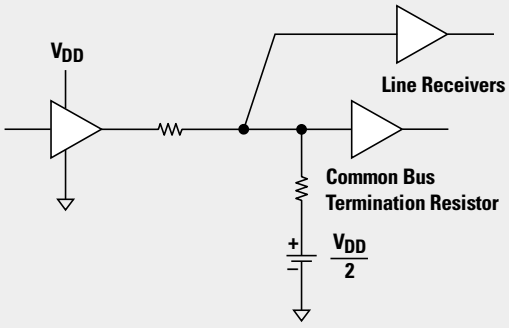
Figure 1. Bus termination schemes



(a) Termination resistors tied to ground



(b) Termination resistors tied to V_{TT}

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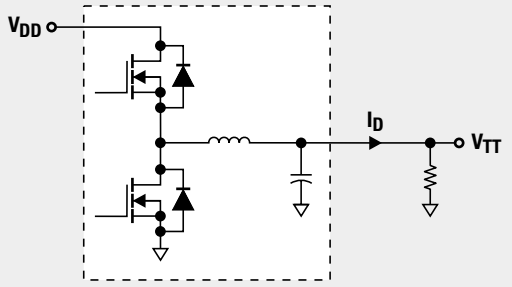
Topology

Figure 2 shows the power supply topology proposed for DDR applications. Depending on output-current demands, the circuit operates in two modes. With a sourcing requirement, the circuit operates as a synchronous buck power stage taking input power from the source and providing it to the load; however, with a sinking requirement, the circuit operates as a synchronous boost power stage taking power from the output and returning it to the input. These two different operating modes create challenges in maintaining good efficiency and good transient response.

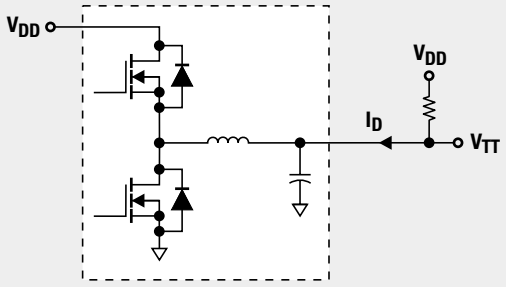
With the DDR supply operating as a boost and buck converter, a new scheme to control switching of the MOSFET power switches is needed. In synchronous buck control schemes, the transition from where the high-side MOSFET conducts to where the low-side MOSFET conducts and the transition from where the low-side MOSFET conducts to where the high-side MOSFET conducts have been handled differently. The high-side to low-side transition can be made almost without loss. The high-side switch can be turned off, allowing the inductor to swing the phase voltage to zero. A comparator can be used to sense the phase voltage and turn the bottom switch on with zero volts across it, resulting in zero voltage switching of both devices. The other transition is hard switched; and losses are incurred because the phase voltage must be switched positive, resulting in cross-conduction and capacitive loss. In the boost mode of operation, the zero-voltage-switching transition occurs at the low-side to high-side transition; and the hard switching occurs as the inductor node is pulled low. This means that a control strategy is needed to respond to the two operating modes to maintain good efficiency.

Figures 3 and 4 illustrate waveforms of the two operating modes. The waveform in Figure 3 shows the phase

Figure 2. Two operating modes of the DDR power supply



(a) Synchronous buck mode (sourcing current)



(b) Synchronous boost mode (sinking current)

Figure 3. Phase voltage while sourcing current

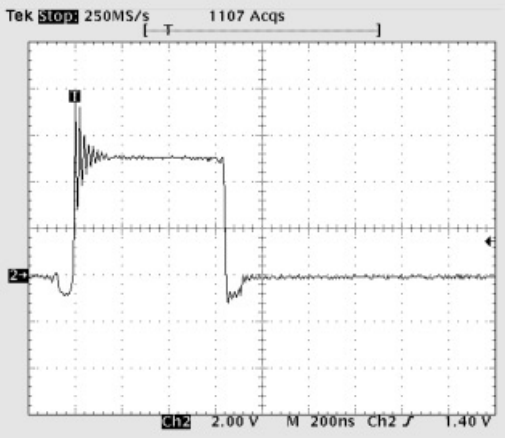
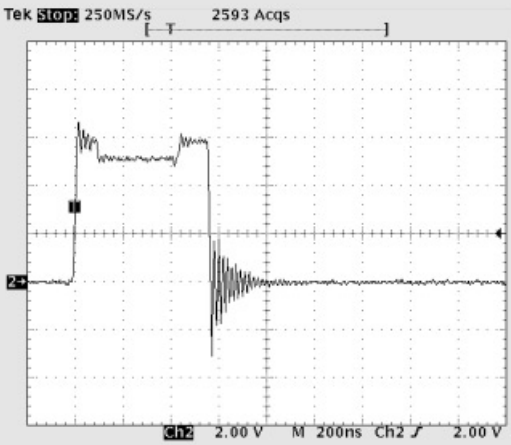


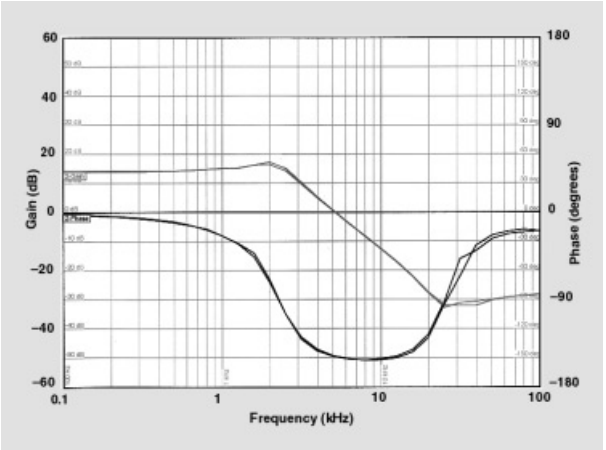
Figure 4. Phase voltage while sinking current



voltage during the buck mode of operation. At the left side, the bottom switch is on. Later the current starts to transition to the internal diode, and the top switch is turned on in a short time. The top switch conducts at the proper duty factor and is then turned off. The inductor then drives the phase voltage toward the low rail. The bottom catch diode (body diode of the synchronous FET) limits the voltage, at which time the bottom switch is then turned back on. The waveform in Figure 4 shows the phase voltage during the boost mode of operation and starts with the bottom FET switch on. The bottom synchronous FET is then turned off, and the phase voltage is driven positive by the inductor. The top diode conducts for a brief amount of time before the top switch is turned on. This transition allows both switches to be turned on and off without loss. The high-to-low transition begins with the top switch turning off and current transitioning to its internal diode.

With two modes of operation, it is not intuitive what the control characteristics of the supply should be. In the buck operating mode, the supply will maintain output voltage (V_{TT}) independently of output current and input voltage. In the boost operating mode, the supply will maintain input voltage (V_{TT}) independently of output voltage and output current. The supply is just a buck converter operating at less-than-positive output current. As shown in Figure 5, loop gain is essentially independent of operating mode.

Figure 5. Power stage gain characteristics (sourcing and sinking modes)



TL5002 controller

Figure 6 presents the block diagram of a new, very simple and inexpensive IC available for DDR control, the TL5002. Rated for 3.6- to 40-V operations, it can be used in a number of applications besides DDR. The monolithic chip contains minimal circuitry to perform frequency generation, voltage regulation, and pulse width modulation (PWM). The operating frequency can be programmed up to 500 kHz by a single external resistor. An error amplifier with uncommitted inputs is provided to compare the V_{TT} output voltage to one-half the V_{DD} supply. The amplifier has a gain bandwidth product of almost 3 MHz, allowing a wide control loop bandwidth. The output of the error amplifier is internally compared against a sawtooth waveform generated by the oscillator and sets the pulse width during normal operation. A third input to the comparator provides a soft-start function during the initial turn-on interval and can be used to set a maximum pulse width. An internal current source provides this feature with minimal external components. An under-voltage lockout circuit prevents spurious operation during a low-input-voltage condition by gating an output AND gate. The output of the chip is an open-collector transistor that is easily interfaced to a number of drive circuits.

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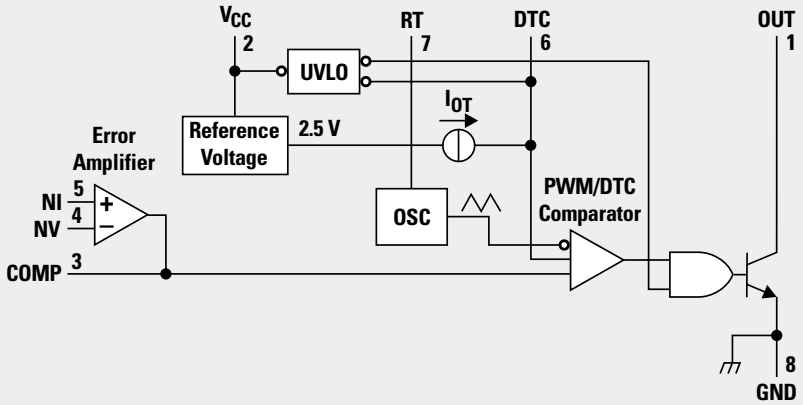
Figure 6. TL5002 block diagram



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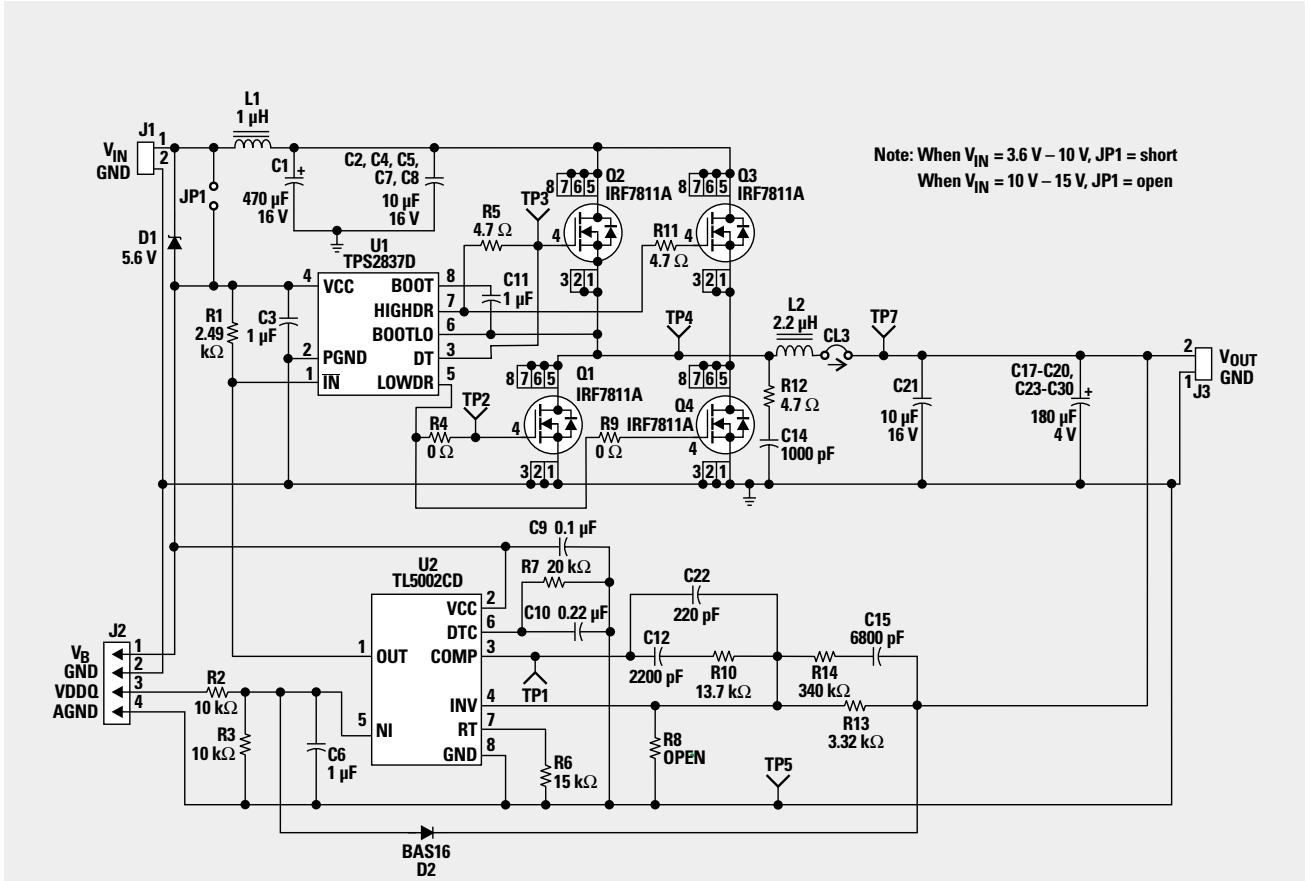
Prototype performance

The schematic of a power supply that can be used to power DDR memory is shown in Figure 7. This circuit is available as an evaluation module from Texas Instruments (SLVP180C). The top and bottom power MOSFETs are switched on and off by the TPS2837, a high-/low-side synchronous MOSFET driver, while the TL5002 controller maintains the output-voltage regulation. The TL5002's regulation method differs from that of a typical controller that contains a fixed internal reference voltage. In the TL5002, an external voltage is used in place of the internal reference voltage. The reference voltage input to the tracking regulator (designated V_{DDQ}) is typically scaled by 0.5 to provide an output voltage equal to one-half of V_{DDQ}. The TL5002 then compares this scaled voltage to the sensed output voltage and creates an error signal that is used to adjust the on time of the top-side MOSFETs.

The TL5002 EVM DDR tracking regulator operates in voltage-mode control and has a nominal switching frequency of 400 kHz. The high-side and low-side switches are each implemented with two parallel connected SO-8 package FETs to reduce the power dissipation in each device to an acceptable level for an SO-8 package. Heavy copper etch is used on multiple layers to spread the heat away from the MOSFETs and distribute it across the PWB. An input filter inductor minimizes the ripple voltage imposed back on the input voltage source. Two high-side MOSFETs and two low-side MOSFETs provide the optimal combination to handle the power dissipated as switching and conduction losses in the MOSFETs. Although this design is optimized for 12 A, changing the quantity of top and bottom FETs can generate more or less output current. If a total of one top and one bottom FET were used, the output current capability would be approximately 6 A. Several other design factors would need to be taken into account. Fewer input capacitors are needed to handle the input ripple current, and an output inductor rated for less current reduces the overall circuit area. If higher output current were desired, more MOSFETs and a larger inductor would be required. In addition, a second TPS2837 FET driver may be required due to the power dissipation limits of the driver package. A 40-A design utilizing a second

Figure 7. TL5002 EVM schematic

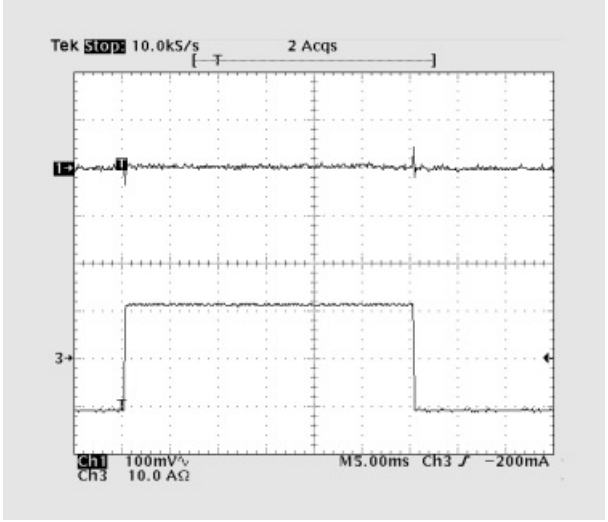


TPS2837 driver and a total of ten top and bottom FETs has been built and successfully tested. Thus, this design is scalable to the output current needed by increasing the power dissipation capability of the power stage.

Figure 8 shows the transient output voltage performance. The bottom waveform shows the output current transitioning from sinking –12 A to sourcing 12 A of current. The top waveform shows the resulting output-voltage transients. The power supply maintains voltage regulation within an acceptable window of 40 mV at these extreme conditions. The current being sourced from or sunk into the tracking regulator is a function of the address data states being driven and the amount of memory being addressed. This test is an extreme of all the data lines simultaneously changing from one state to another (see the test set-up in Figures 3-1 and 3-2 of Reference 1). Actual operating conditions likely will not be as severe.

Figure 9 shows the measured efficiency of the TL5002 EVM while operating as a tracking regulator with 5-V_{IN} and 1.25-V_{DC} output (V_{DDQ} is equal to 2.5 V). Efficiency is good and approaches 86% even with the low-voltage output of 1.25 V. Higher efficiency is possible with an increase in MOSFET count and cost. The efficiency when sourcing current is higher than it is when sinking current. Improvements in the sinking-current mode can be made with the introduction of faster power switches or a different control method. In the present implementation, the gate-drive voltage of the top FET controls the turn-on of the bottom FET during the high-side to low-side transition. The gate-drive timing during the low-side to high-side transition is controlled by a simple delay. This method takes advantage of the zero-voltage switching of the buck mode of operation but results in lower efficiency for the boost mode.

Figure 8. Full sourcing to full sinking transient response



The power stage was also designed to be a dedicated synchronous buck regulator with an output as high as 3.3 V_{DC} when powered from a 5-V_{DC} input voltage. This is accomplished by replacing the TL5002 controller with the TL5001 pulse width modulator controller and making

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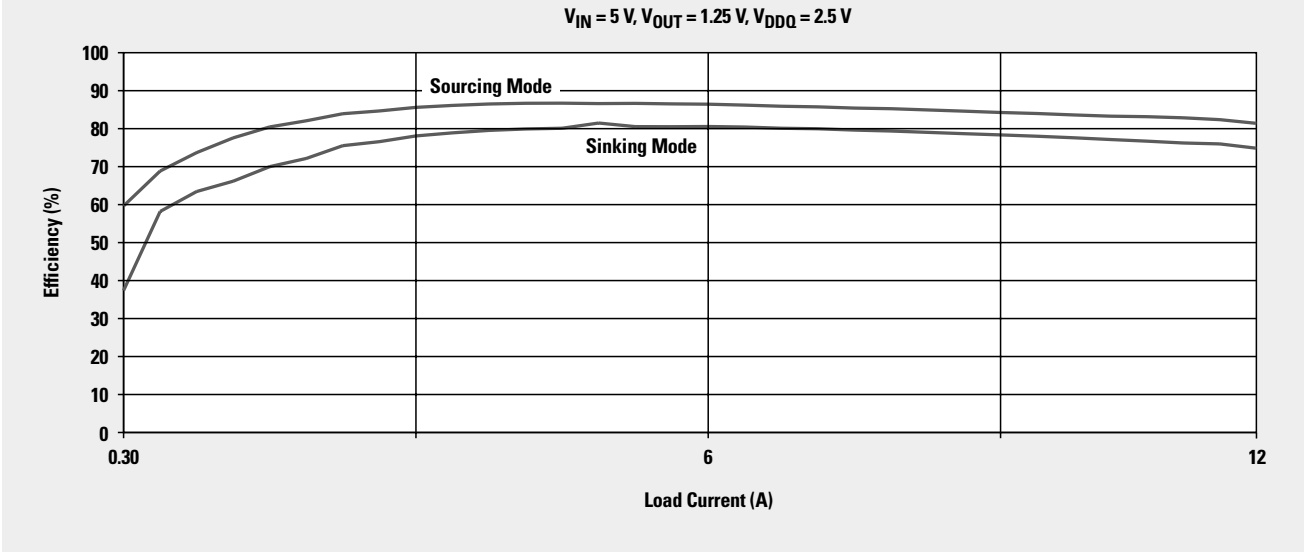
Figure 9. TL5002 EVM efficiency as a V_{TT} tracking regulator



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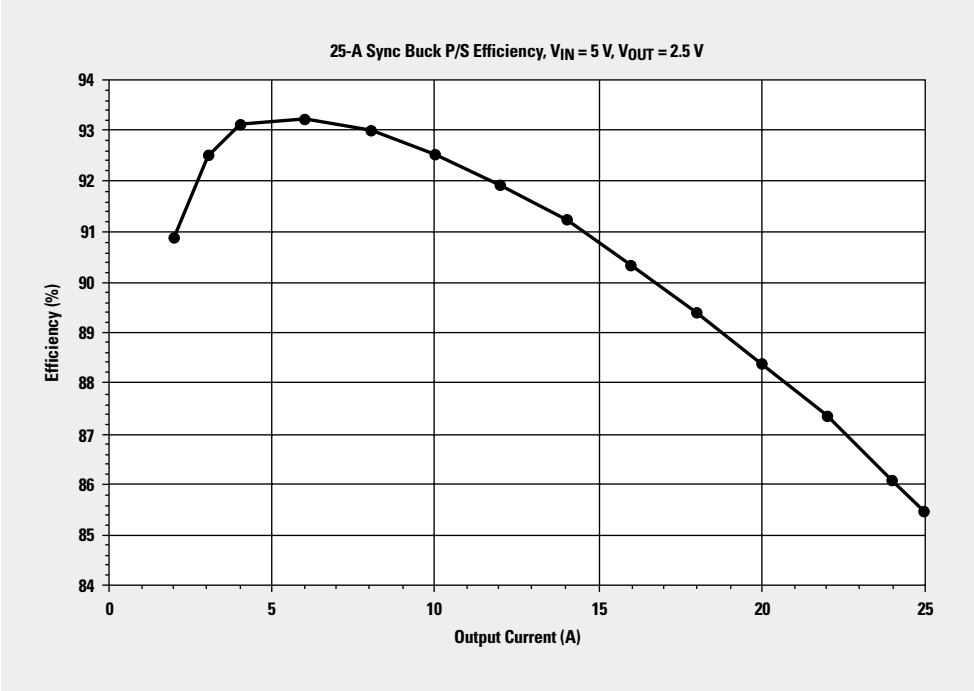
some minimal component changes. Figure 10 shows the efficiency of the TL5001 implementation configured for a fixed 2.5 V_{OUT} when powered from a 5-V input. The improvement in efficiency can be attributed to the increased output voltage.

A summary of the prototype operating specifications for the DDR power supply is given in Table 1. Data was measured under the conditions indicated in the footnotes.

Figure 10. TL5001 EVM efficiency as a 2.5-V V_{DD} regulator



Conclusion

TI has introduced a new TL5002 controller IC to address the needs of the DDR bus termination power. The controller provides voltage tracking of a reference supply and both sourcing and sinking current, while maintaining high efficiency over a wide current range. An example DDR design of 12 A of output current with outputs between 0.9 V and 1.25 V was presented. Design issues and their solutions were provided for the power supply operating as a traditional buck power stage in the sourcing mode and as a synchronous boost regulator in the sinking mode. Control-loop characteristics that allowed fast transient load were found to be identical in both sinking and sourcing modes of operation. The design is scalable from as low as 1 A up to 40 A of output current. Sufficient design detail was provided to form the basis for a successful DDR power supply.

Table 1. Prototype operating specifications

Specification		min	typ	max
Input Voltage Range (V)		3.6	5	15
V_{DDQ} Voltage Range (V)		1.8	2.5	3
Output Voltage Range (V)		$\frac{V_{DDQ}}{2}$ - 40 mV	$\frac{V_{DDQ}}{2}$	$\frac{V_{DDQ}}{2}$ + 40 mV
Output Current Range (A)		–12		12
Operating Frequency (kHz)			400	
Output Ripple	Steady State (mV)			5*
	at Load Transient of 0.4 A/µsec (mV)	–35**		+35**
Efficiency (%)			85***	86.3***

* V_{IN} = 5 V, V_{OUT} = 1.25 V, I_O = 12 A
** V_{IN} = 5 V, V_{OUT} = 1.25 V, I_O = ±12 A
*** V_{IN} = 5 V, V_{OUT} = 1.25 V, I_O = 4.6 A

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

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1. "TL5002EVM-180 DDR Power Supply EVM Using TL5002 (Synchronous Buck Converter) User's Guide" slvu044
2. Y.R. Kim, "DDR, Today and Tomorrow," Platform Conference, Silicon Conference Center, San Jose, California, July 18–19, 2000. —
3. "TL5002 Pulse-Width-Modulation Control Circuit," Data Sheet slvs304
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Related Web sites

power.ti.com
www.ti.com/sc/ddr

Get more product information at:
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Runtime power control for DSPs using the TPS62000 buck converter

By Markus Matzberger
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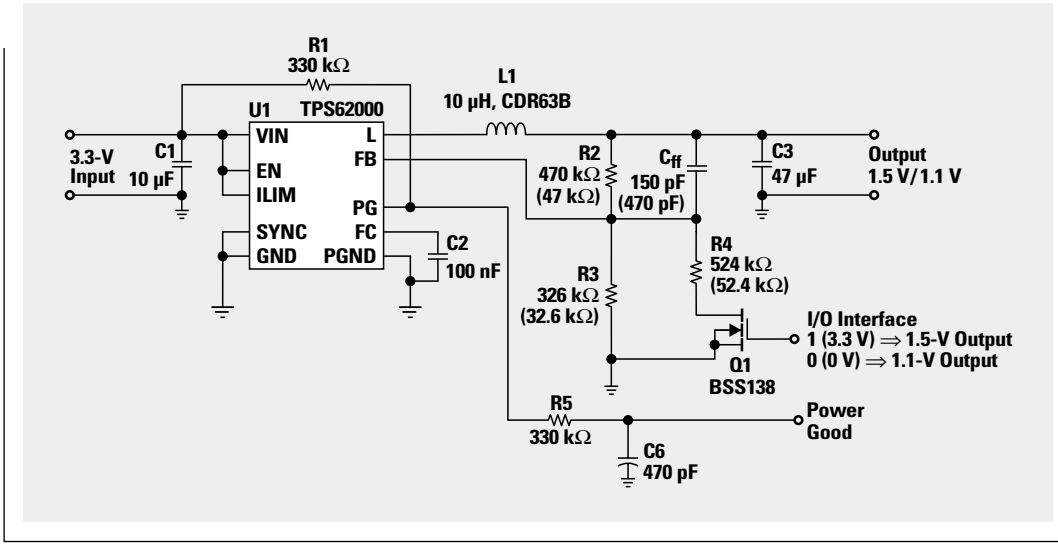
Introduction

This article describes how to reduce core power consumption of a digital signal processor (DSP) or microprocessor using runtime power control (RPC). This technique becomes more and more attractive for portable battery-powered systems where low power consumption is critical for extended operating time.

In many portable applications like Internet audio, MP3 players, or digital still cameras, the full processing power of a DSP is not needed all the time. This presents the opportunity to reduce the processor core power consumption by decreasing the core supply voltage and clock frequency. The technique of adjusting the core voltage to the required core performance is called dynamic voltage scaling (DVS) or RPC.

This article describes a circuit solution for DVS based on the TPS62000 buck converter. During the periods in which maximum DSP performance is not required, the core supply voltage is reduced and the DSP operates at a reduced clock rate. For the next generation of microprocessors and DSPs, the ability to handle this technology will become an important feature. RPC extends battery life in handheld applications like MP3 players, digital cameras, and PDAs. Actual measurements using an MP3 player application resulted in a 23% reduction of DSP core power.

Figure 1. Circuit diagram for dynamic voltage scaling



Core supply considerations

The DSP power supply can be separated into an I/O interface supply and a core supply. The I/O interface is typically powered by the 3.3-V system supply voltage; whereas the core supply requires voltages below 1.5 V. The minimum required core supply voltage depends on the clock rate, which is a function of the DSP performance that the application demands. For the MP3 player application chosen for this example, dynamic voltage scaling was implemented by switching the core supply between the two voltage levels, 1.5 V and 1.1 V. These two values seem practicable for modern DSP applications but need to be determined by the system designer and carefully validated against data sheet limits. The following simplified equation describes the power consumption of a DSP core:

$$P_C \sim (V_C)^2 \times f,$$

where P_C = core power consumption, V_C = core voltage, and f = core clock frequency. It can be seen that power consumption can be reduced by lowering the internal clock frequency and the core supply voltage.

Circuit description

The TPS62000 is a member of the TPS6200X high-efficiency synchronous buck converter family, which is specially designed for portable applications. The TPS62000 provides a wide adjustable output voltage range, going as low as 0.8 V. Efficiency up to 95% and output current up to 600 mA make this device ideally suited for core voltage supply. It comes in a tiny MSOP10 package and enables a wide input voltage range of 2 V to 5.5 V. Due to decreasing core supply voltages in modern DSP systems, using synchronous step-down converters like TPS62000 is far more efficient than using LDO regulators.

The TPS62000 buck converter is powered by a 3.3-V system supply. A general-purpose I/O (GPIO) port on the DSP selects the requested core voltage. Figure 1 illustrates the circuit that was used for the DVS implementation. By varying the feedback resistor network, the core voltage can be adjusted to between 1.1 V and 1.5 V. A MOSFET modifies the resistive voltage divider connected

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between the output of the DC/DC converter and its feedback (FB) pin by switching a parallel resistor in the circuit. In this application, a general-purpose BSS138 MOSFET is used with a V_{GSth} of 1.6 V. The GPIO 3.3-V port drives the MOSFET. The feedback resistor network consists of R2, R3, and R4. C_{ff} is a feed-forward capacitor that is used in the compensation network of the regulator to improve regulation.

Modifying the resistor network by switching R4 parallel to R3 is recommended. The parasitic capacitances of the MOSFET then have the least influence on the regulation behavior of the DC/DC converter. The proposed MOSFET has an $R_{DS(on)}$ below 10 Ω. This value is very small compared to the values of the resistive divider and can therefore be neglected in the calculation of the resistance values of the modified resistive divider.

General requirements for this application are:

- Output voltage 1 (DSP core): 1.5 V
- Output voltage 2 (DSP core): 1.1 V
- Input voltage: 3.3 V
- Output current: 150 mA (10-Ω load)

To keep current and power losses through the adjustment resistor network as low as possible, the resistors are calculated to R2 = 470 kΩ and R3 = 326 kΩ. For R3 and R4 in parallel to equal 201 kΩ, the value of R4 is calculated to 524 kΩ. The calculation of the feedback resistor network is described in Reference 1. With this resistor choice, the quiescent current through the resistor network is less than 2 µA. This is about 4% of the typical 50-µA quiescent current of the converter. To reduce the influence of the MOSFET's gate-drain capacity during switching, a 150-pF capacitor is recommended for C_{ff}. The calculation of the C_{ff} capacitor value is also explained in Reference 1.

Figure 2 shows a complete voltage scaling cycle. I_{OUT} is the output current, powered in a 10-Ω load. V_{SEL} represents the I/O voltage applied to the MOSFET gate. A low level of V_{SEL} scales the output voltage to 1.1 V; a high level to 1.5 V. Figures 3 and 4 show the V_{OUT} variation in more detail.

Influence of the MOSFET on the regulation loop

In Figure 3, a small voltage overshoot on V_{OUT} is generated when V_{SEL} is switched from high- to low-level. The reason for this is the gate-drain capacitance of the MOSFET, which injects the negative edge of the V_{SEL} signal into the feedback resistor network.

If lower values for the feedback resistor network are used, the influence of the gate-drain capacitance can be reduced. Lower resistor values result in higher values for C_{ff}. As an experiment, the resistor values are lowered with a factor of 10 to R2 = 47 kΩ, R3 = 32.6 kΩ, and R4 = 52.4 kΩ. C_{ff} is increased to 470 pF.

Figure 2. Complete voltage scaling cycle

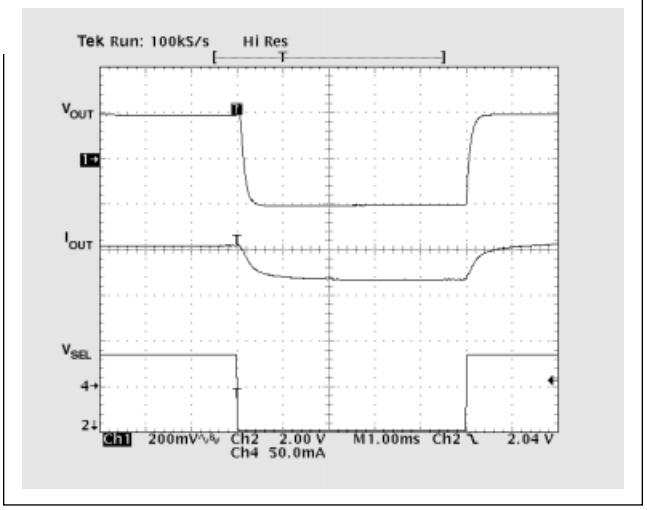


Figure 3. V_{OUT} scaled from 1.5 V to 1.1 V

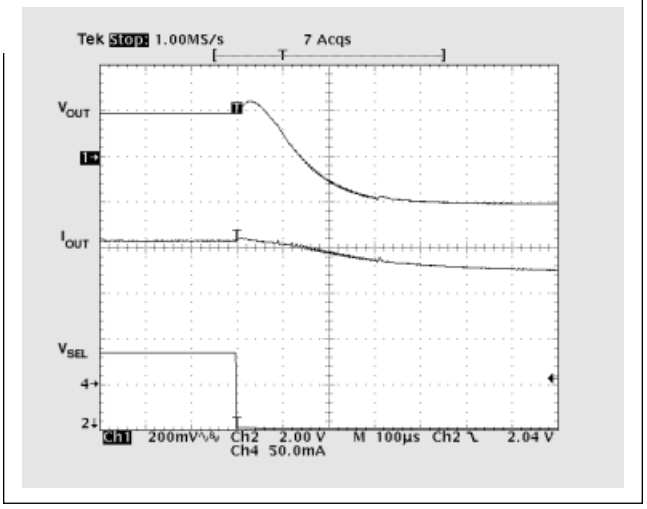
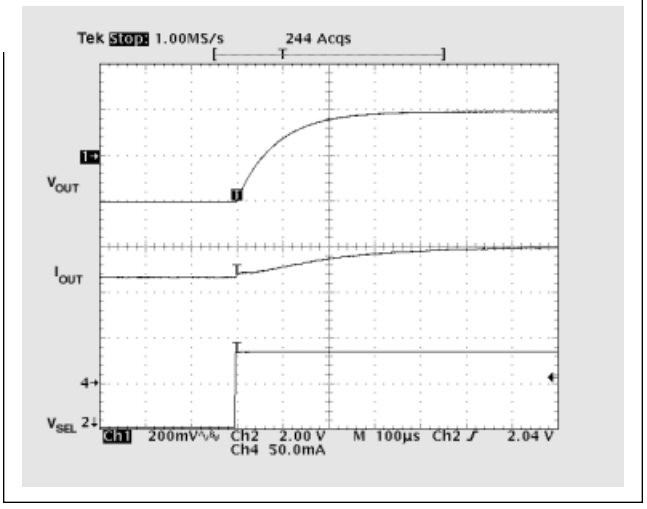


Figure 4. V_{OUT} scaled from 1.1 V to 1.5 V



With this modification, the overshoot (when the converter is switched to regulate to 1.1 V) is decreased to less than 20 mV, as can be observed in Figure 5.

Figure 6 shows the feedback resistor network with MOSFET gate-drain (C_{GD}) capacity. With an increased value of C_{ff}, the influence of gate-drain capacity C_{GD} is reduced. C_{ff} then works as a low-impedance connection to V_{OUT} and minimizes the docked V_{SEL} signal at the FB pin. Furthermore, the influence can be reduced if a MOSFET with lower internal capacitance is used instead of a general-purpose MOSFET.

Timing considerations

The timing behavior of the V_{OUT} signal depends on the values of the output and input capacitors, the coils, and the feedback resistor network. Exact values that are valid for all applications can't be specified here, because the fall time of V_{OUT} depends on the output current as well as on the inductor and output capacitor. During the fall time, the load must absorb the energy stored in the output capacitor until the lower voltage is in regulation.

As shown in Figure 7, the timings are described as follows:

- *Delay time t_0 to t_1:* Range within 50 µs in this application, measured with a 10-Ω load. This represents the settle time of the resistor network on the FB pin.
- *Fall time t_1 to t_2:* This time is mainly defined by the output current. It also depends on the values of the inductor and the output capacitor.
- *Delay time t_3 to t_4:* In this application, about 10 µs.
- *Rise time t_4 to t_5:* 125 µs to 150 µs measured in this application. This also depends on the components and the load current.

Power Good output

The Power Good comparator (see Figure 1) has an open-drain output that becomes active-high if the output voltage exceeds 94.5% of its nominal value. The dynamic variation of the resistor network can affect the Power Good detection circuit, because it compares the FB voltage with an internal reference. Depending on output current, a short /PG spike can occur during rise time from 1.1-V to 1.5-V core level. Using a little RC filter on PG output is recommended to eliminate this short spike and to get a defined PG signal, if used. R1 is the PG pull-up resistor, and R5 and C6 form the RC-filter network, as can be seen in Figure 1.

Core-voltage monitoring

After the core voltage reaches 1.5 V, the DSP can be switched to higher internal clock rates again. To do that, the time t_5, when the DC/DC converter output is in regulation again, must be detected. This can be achieved by either of the following alternatives.

- *A software timer* (activated after the DSP initiates the control signal to increase the supply voltage). Since the rise time of V_{OUT} is application-specific, the designer has to determine it based on measurements.

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Figure 5. Reduced voltage overshoot

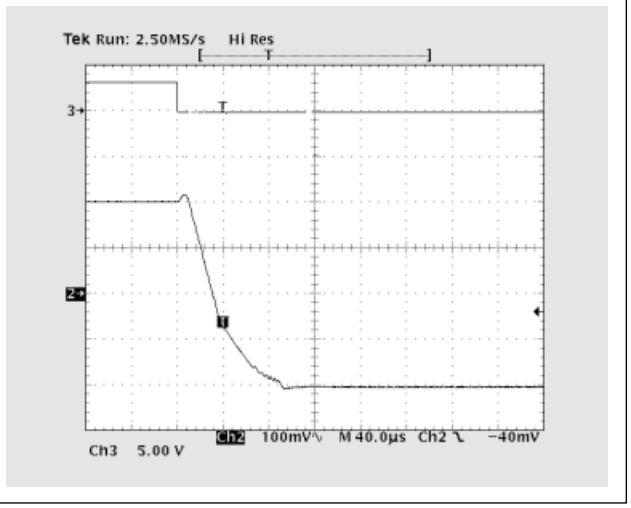


Figure 6. Feedback resistor network with gate-drain capacity

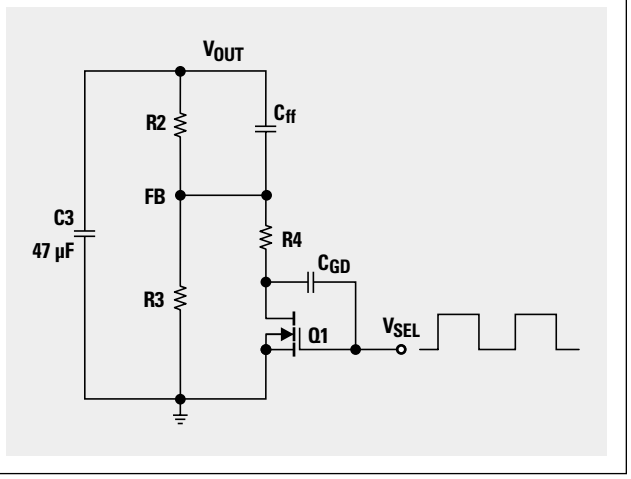
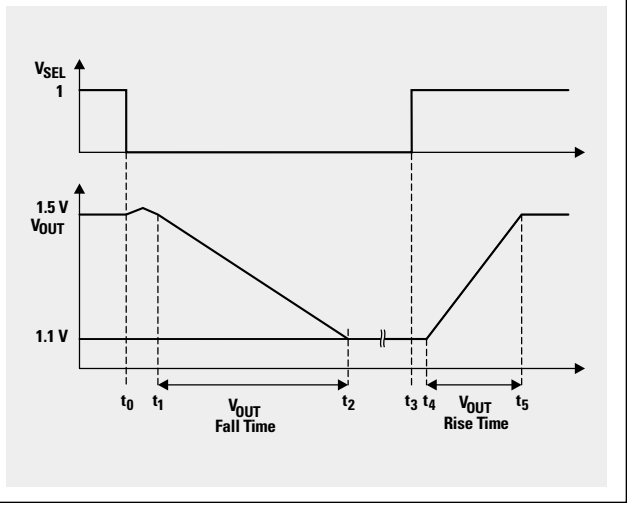


Figure 7. Timing



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- *Voltage monitoring.* Figure 8 shows the relation between V_{OUT} and the signal core-voltage detection (CVD). This CVD signal can be generated by the Power Fail comparator of a supply voltage supervisor (SVS) circuit, like the TPS3705 family with internal 1.25-V reference. This method detects the exact moment when the 1.5-V core voltage fails or matches. As many processors request negative edges for interrupt generation, inverting the CVD signal can be useful. The SVS circuit is supplied by the 3.3-V system supply. The threshold voltage for core-voltage detection can be adjusted by external resistors. The basic block diagram of this circuit is shown in Figure 9.

Conclusion

The solution for dynamic voltage scaling, as described in this article, is a simple approach to reduce the core power consumption of next-generation DSPs and microprocessors. Based on the TPS62000 high-efficiency step-down converter, only a few additional passive components and a general-purpose MOSFET are required. The benefit of reduced core power consumption will compensate the effort in additional components, especially in portable applications where power consumption is critical. Actual measurements using TI's Internet audio player reference design resulted in a 23% reduction of DSP core power consumption and an appropriately extended operating time from one battery set.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "TPS62000, TPS62001, TPS62002, TPS62003, TPS62004, TPS62005, TPS62006, TPS62007 High-Efficiency Step-Down Low Power DC-DC Converter," Data Sheet	.slvs294

Acknowledgments

Special thanks to Oliver Nachbaur, Juergen Neuhaeusler, Y. Matsumoto, and Guenter Sporer, all of Texas Instruments.

Related Web sites

power.ti.com
www.ti.com/dsp

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www.ti.com/sc/device/*device*
Replace *device* with tps3705-30, tps3705-33, tps3705-50, tps3707-30, tps3707-50, or tps62000

Figure 8. Timing of core-voltage detection

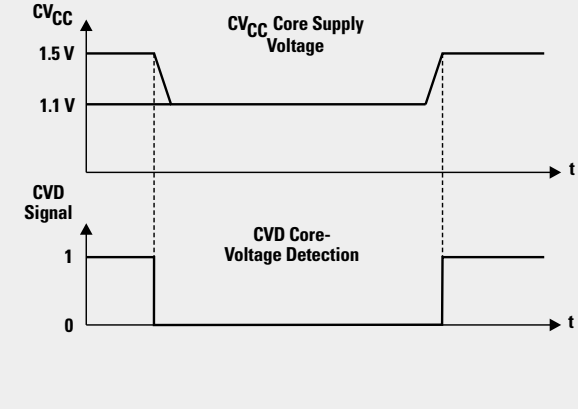
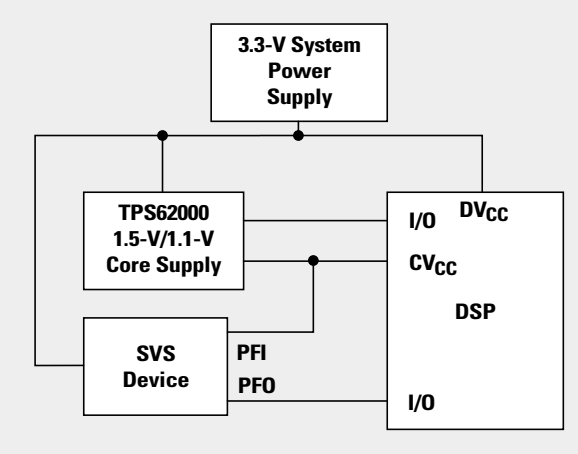


Figure 9. Basic block diagram for voltage monitoring



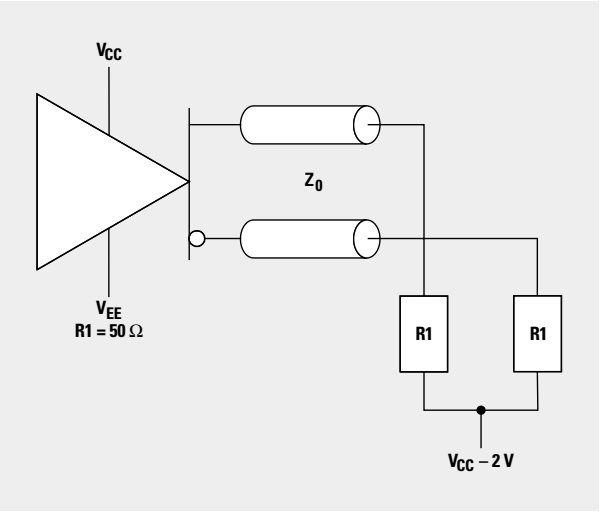
The SN65LVDS33/34 as an ECL-to-LVTTL converter

By Chris Sterzik
Applications Specialist, Interface Products

Introduction

Emitter-coupled logic (ECL) has often been the physical layer of choice for system designers to meet high-speed data transmission requirements. The fast edges (rise and fall times) of ECL have permitted higher speeds, but at the expense of increased PC board complexity, power consumption, and electromagnetic interference (EMI). Now, lower power and lower EMI technologies like LVDS provide designers with an alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to introduce LVDS receivers in ECL systems by implementing a resistor divider and capacitive coupling. These capacitors and resistors further add to the complexity and part count of a design. To alleviate the complexity of interfacing with ECL, TI has introduced the SN65LVDS33/34 receivers. This article describes a basic interface between an LVDS receiver and an ECL driver, and how the SN65LVDS33/34 receivers can be used to convert different types of ECL to LVTTL without a resistor divider or capacitive coupling. This article also demonstrates that, since no additional components are needed with wide common-mode receivers, these receivers can be used as a first step to replace an ECL physical layer with LVDS.

Figure 1. ECL characteristic load



PECL and LVPECL to standard LVDS

For ECL devices including negative ECL (NECL), positive ECL (PECL), and low-voltage, 3.3-V PECL (LVPECL), the load seen by the driver must be 50 Ω biased to 2 VDC below the device (driver's) V_{CC}. This characteristic load is depicted in Figure 1.

Often the bias voltage level for the characteristic load is not available and is attained through a Thevenin equivalent circuit (resistor divider). Figure 2 shows a Thevenin equivalent circuit intended to provide the characteristic load and the necessary voltage divider to translate the ECL output levels of node V_A and $\overline{V_A}$ to the LVDS level desired at node V_B and $\overline{V_B}$.

Equations 1–3 are used to calculate the resistor values in Figure 2.

$$50 = R1 \parallel (R2 + R3) \quad \textbf{(1)}$$

$$\frac{V_{CC} - 2 - V_{EE}}{V_{CC} - V_{EE}} = \frac{R2 + R3}{R1 + R2 + R3} \quad \textbf{(2)}$$

$$\text{Gain} = \frac{R3}{R2 + R3} \quad \textbf{(3)}$$

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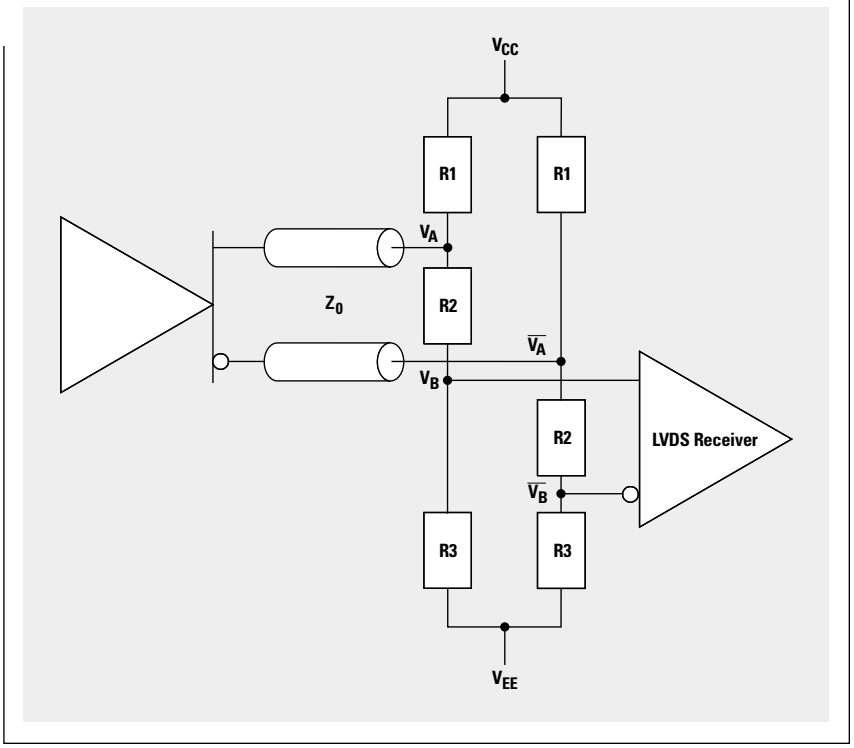
Figure 2. Differential ECL interface to standard LVDS equivalent circuit



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Equations 1 and 2 establish the necessary Thevenin equivalent termination and voltage as seen by the driver. The Thevenin equivalent termination is equal to the common-mode characteristic impedance of the transmission line, 50 Ω (100 Ω differential impedance). This equality satisfies Equation 4, the impedance matching of the load with the transmission line.

$$Z_0 = R1 \parallel (R2 + R3) \quad \textbf{(4)}$$

When Z_0 is not equal to 50 Ω, then Equations 1 and 4 are incompatible; and trade-offs need to be made with respect to driver flexibility and tolerance to reflections on the transmission line.

Equation 3 establishes the gain of the resistor network. The gain of the resistor network should provide the voltages within the valid input range of the receiver, given the range of the driver output. The minimum and maximum levels for the LVPECL, PECL, and NECL devices are given in Table 1.

Table 1. LVPECL, PECL, and NECL outputs

	LVPECL	PECL	ECL
V_{OH}max (V)	2.42	4.120	–0.880
V_{OH}min (V)	2.275	3.975	–1.025
V_{OL}max (V)	1.68	3.380	–1.620
V_{OL}min (V)	1.49	3.190	–1.810

The LVDS standard requires a differential voltage magnitude of 100 to 600 mV at the input to the receiver, and the valid input voltage range is 0 to 2.4 V. Table 2 shows the relationships between the gain and the varied input and output levels. The intent of Table 2 is to limit the gain selection to values that provide valid input voltage levels over the entire output range of the driver.

From Table 2 we find that the gain of LVPECL and PECL can be bound to the following values:

$$\text{LVPECL} \rightarrow 0.168 \leq \text{Gain} \leq 0.645$$

$$\text{PECL} \rightarrow 0.168 \leq \text{Gain} \leq 0.583$$

The gain is chosen to be 0.4 for both the LVPECL and PECL termination schemes. The resistor values are calculated in Table 3.

Table 2 shows that the NECL output levels are not compatible with standard LVDS, given the resistor network of Figure 2. Most LVDS receivers do not support the input range needed for a NECL interface and often require some type of capacitive coupling to adjust the common-mode voltage seen at the receiver inputs. The capacitors are usually placed on each of the differential lines before the termination network and before the receiver. Besides the obvious disadvantage of increased part count, capacitive coupling also introduces inter-symbol interference (ISI) when dealing with non-dc-balanced transmissions. An alternative to this coupling is the use of receivers that accept a wide range of common-mode inputs, eliminating ISI problems and minimizing the number of parts needed to interface various types of ECL to LVDS.

Table 2. Gain limits for standard LVDS interface

		OUTPUT DIFFERENTIAL		OUTPUT VALUE	
		min (V)	max (V)	min (V)	max (V)
LVPECL		2.275 – 1.68 = 0.595	2.42 – 1.49 = 0.93	1.49	2.42
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x 1.49 > 0.0	Gain x 2.42 < 2.4
PECL		3.975 – 3.38 = 0.595	4.12 – 3.19 = 0.93	3.19	4.12
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x 3.19 > 0.0	Gain x 4.12 < 2.4
ECL		(–1.025) – (–1.620) = 0.595	(–0.880) – (–1.810) = 0.93	–1.81	–0.880
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 0.600	Gain x –1.81 > 0.0	Gain x –0.88 < 2.4

Table 3. Standard resistor values and theoretical output voltages for LVDS translation

DRIVER	V_{CC} (V)	V_{EE} (V)	R1:R2:R3 (Ω)	V_A HIGH (V)	V_A LOW (V)	V_B HIGH (V)	V_B LOW (V)
LVPECL	3.3	GND	127: 49.9: 33.2	2.42	1.49	0.71	0.34
LVPECL	3.3	GND	127: 49.9: 33.2	2.28	1.68	0.64	0.40
LVPECL	3.3	GND	127: 49.9: 33.2	2.42	1.68	0.67	0.37
PECL	5.0	GND	82.5: 75: 50	4.12	3.19	1.65	1.27
PECL	5.0	GND	82.5: 75: 50	3.98	3.38	1.59	1.35
PECL	5.0	GND	82.5: 75: 50	4.12	3.38	1.65	1.35

Table 4. Gain limits for the SN65LVDS33/34 interface

		OUTPUT DIFFERENTIAL		OUTPUT VALUE	
		min (V)	max (V)	min (V)	max (V)
LVPECL		2.275 – 1.68 = 0.595	2.42 – 1.49 = 0.93	1.49	2.42
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x 1.49 > –4.0	Gain x 2.42 < 5.0
PECL		3.975 – 3.38 = 0.595	4.12 – 3.19 = 0.93	3.19	4.12
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x 3.19 > –4.0	Gain x 4.12 < 5.0
ECL		(–1.025) – (–1.620) = 0.595	(–0.880) – (–1.810) = 0.93	–1.81	–0.88
	Gain	Gain x 0.595 > 0.100	Gain x 0.93 < 3.00	Gain x –1.81 > –4.0	Gain x –0.88 < 5.0

ECL to the SN65LVDS33/34

The SN65LVDS33/34 dual/quad receiver provides a wide common-mode capability and a maximum differential input voltage magnitude, both of which exceed the EIA-644 standard. The valid input range is increased to –4 to +5 V; and the differential inputs can vary from 100 mV to 3 V. These extended ranges provide wider bounds for the gain in Equation 3.

From Table 4 we see that the LVPECL-, PECL-, and ECL-to-SN65LVDS33/34 gain can be limited to the following values:

$$\text{LVPECL} \rightarrow 0.168 \le \text{Gain} \le 2.07$$

$$\text{PECL} \rightarrow 0.168 \le \text{Gain} \le 1.21$$

$$\text{ECL} \rightarrow 0.168 \le \text{Gain} \le 2.21$$

The SN65LVDS33/34 bounds for LVPECL, PECL, and NECL gain all include unit gain (Gain = 1). Choosing a unity gain value eliminates the need for the R2 resistors shown in Figure 2 and simplifies the circuit to the one shown in Figure 3.

The elimination of the R2 resistors also reduces the complexity of the equations used to calculate the resistor values in Figure 3.

$$50 = (R1 \parallel R3) \quad \textbf{(5)}$$

$$\frac{V_{CC} - 2 - V_{EE}}{V_{CC} - V_{EE}} = \frac{R3}{R1 + R3} \quad \textbf{(6)}$$

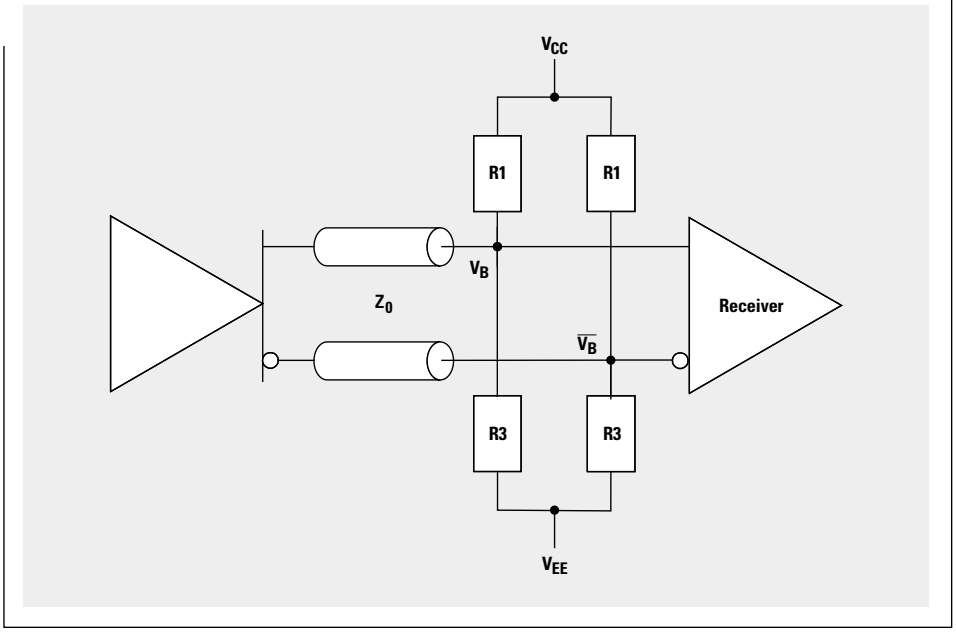
Equations 5 and 6 establish the necessary Thevenin equivalent termination and voltage as seen by the driver, and the third equation to establish gain is no longer needed. The calculated resistor values are shown in Table 5.

Continued on next page

Table 5. Standard resistor values for PECL- and LVPECL-to-SN65LVDS33/34 translation

DRIVER	V_{CC} (V)	V_{EE} (V)	R1:R2 (Ω)
LVPECL	3.3	GND	126.9: 82.5
PECL	5.0	GND	83.3: 125.1
ECL	GND	–5.0	83.3: 125.1

Figure 3. ECL to SN65LVDS33/34



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The eye patterns of the SN65LVDS33/34 output with the LVPECL and NECL drivers are shown in Figures 4 and 5, respectively.

ECL receipt at a distance

Up to this point, for receiving ECL signals, the assumptions have been that the voltage supplies used by the driver are available for the termination network and that the only common-mode voltage is the ECL offset voltages. Another consideration is that the receiver is in a remote location and/or only the 3.3-V supply for the LVDS receiver is available.

A remote receiver creates two problems for the resistor networks previously discussed. First, the voltages are simply not available; only the 3.3 V required by the LVDS receiver is available. Second, in the case of LVPECL, where the V_{CC} is the same for both the driver and receiver, potential differences between grounds becomes a factor. With a ground potential difference between the receiver

Figure 4. LVPECL to SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

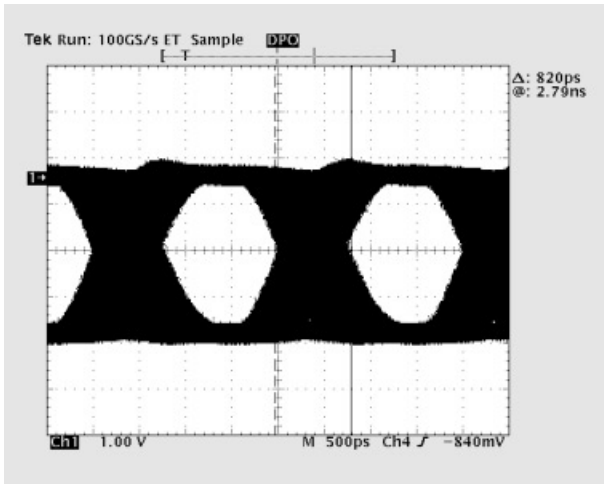


Figure 5. NECL to SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

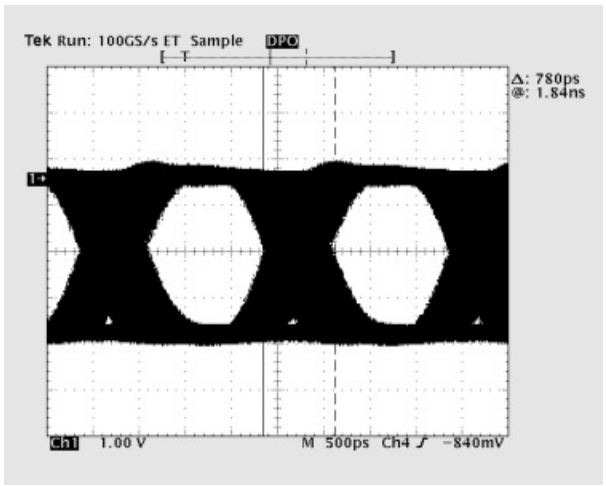


Figure 6. LVPECL and PECL to remote SN65LVDS33/34

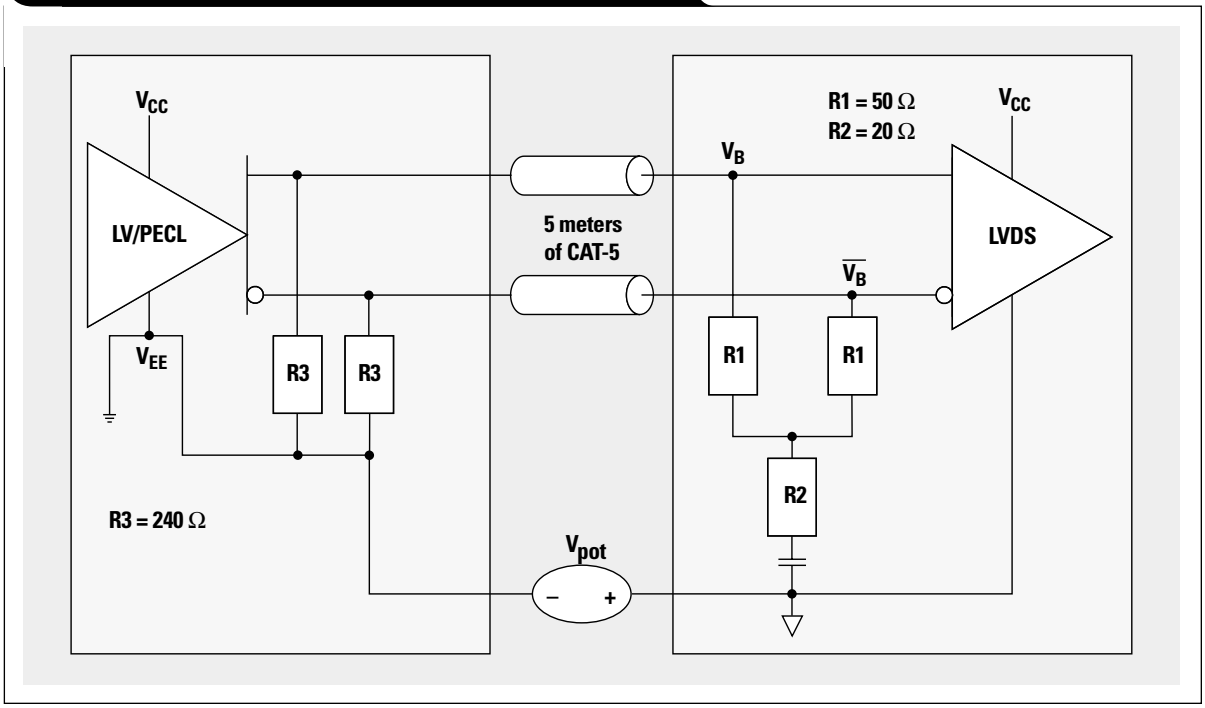
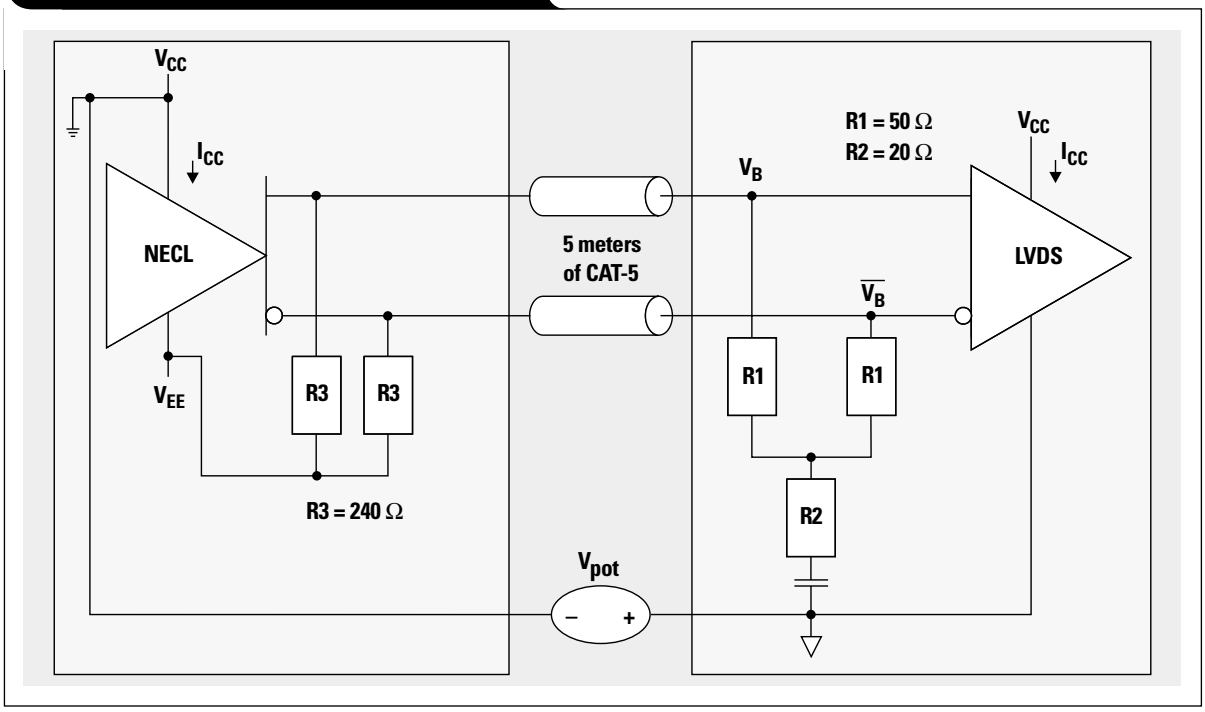


Figure 7. NECL to remote SN65LVDS33/34



and driver, the characteristic load voltage seen by the driver will not be the required $V_{CC} - 2$. The solution to the unavailability of voltages is ac termination. The ground noise problem is alleviated by the wide common-mode capabilities of the SN65LVDS33/34. Figures 6 and 7 depict the use of the SN65LVDS33/34 when the driver and receiver have different ground potentials and are separated by about 5 meters of CAT-5 cable. The eye pattern is shown in Figure 8. Table 6 shows that the SN65LVDS33/34 can tolerate a ground noise magnitude of 2.6 V for LVPECL, 1.1 V for PECL, and 2.3 V for NECL.

As mentioned earlier, the SN65LVDS33/34 receiver exceeds the EIA-644 requirement, and a resistor divider is not needed. With no resistor divider, R1 simply needs to match the characteristic transmission line impedance of 50 Ω. The value of R3 was chosen to provide a resistor path to ground for the ECL driver. When the designer uses a pre-existing source termination, the important parameter is the output voltages. If the voltage levels exceed the inputs of the receiver, then a resistor divider is required at the receiver. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

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Figure 8. NECL to remote SN65LVDS33/34 at 500 Mbps; receiver output (Ch1)

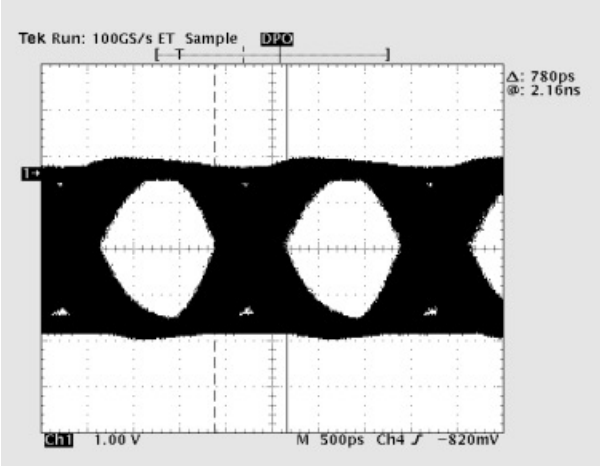

Table 6. LVDS inputs with respect to receiver ground

DEVICE DRIVER	DRIVER TO RECEIVER GROUND POTENTIAL (V_{pot})	V_B HIGH (V)	V_B LOW (V)
LVPECL	–2.64	5.0	4.24
LVPECL	0	2.36	1.60
LVPECL	5.60	–3.24	–4.00
PECL	–1.12	5.0	4.50
PECL	0	3.88	3.38
PECL	7.38	–3.50	–4.00
NECL	–5.87	5.0	4.17
NECL	0.0	–0.87	–1.70
NECL	2.30	–3.17	–4.00

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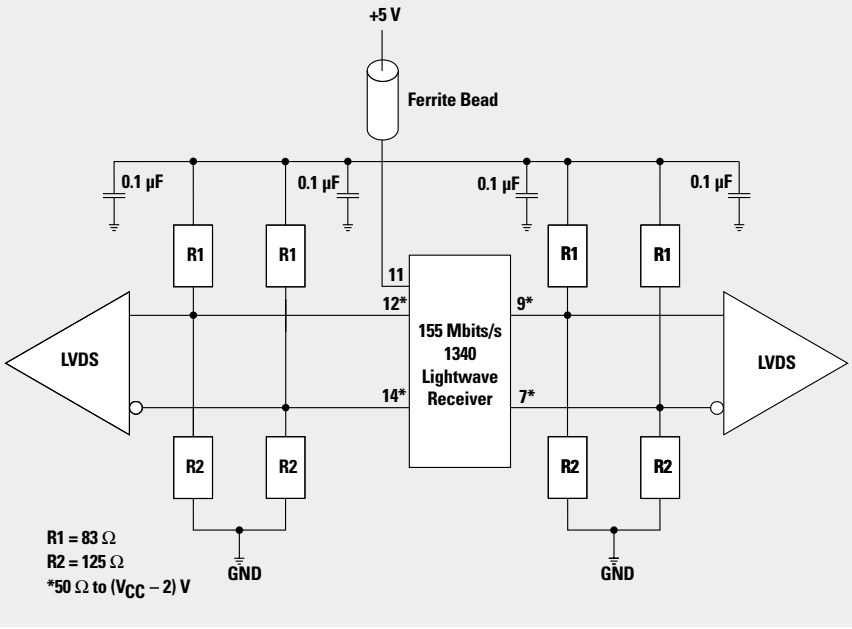
Conclusion

The SN65LVDS33/34 has the versatility and capability to be interchanged with ECL receivers without any component addition (beyond the bias resistor networks used in standard ECL transmission). In Figure 9, where the output structure of the optical device is PECL, the SN65LVDS33/34 can be installed just as easily as a PECL receiver. Also, the termination structures in Figure 9 provide equivalent differential impedances of 100 Ω, the recommended value for LVDS terminations. In the future, if the output structure of the optical device is changed from PECL to LVDS, then the circuit could be re-used as shown in Figure 10. (The connections between R1 and V_{CC} and the connections between R2 and GND would be removed, as shown in Figure 10.)

The idea of interfacing ECL to LVDS logic levels has been widely publicized, but the advantages of replacing ECL with LVDS are often not considered: +3.3-V operation, noise immunity, and low power consumption (which results in low EMI). Designers can now take into consideration the benefits of LVDS when upgrading legacy ECL systems, which no longer require the exclusive use of ECL receivers.

Figure 9. PECL-to-SN64LVDS33/34 application



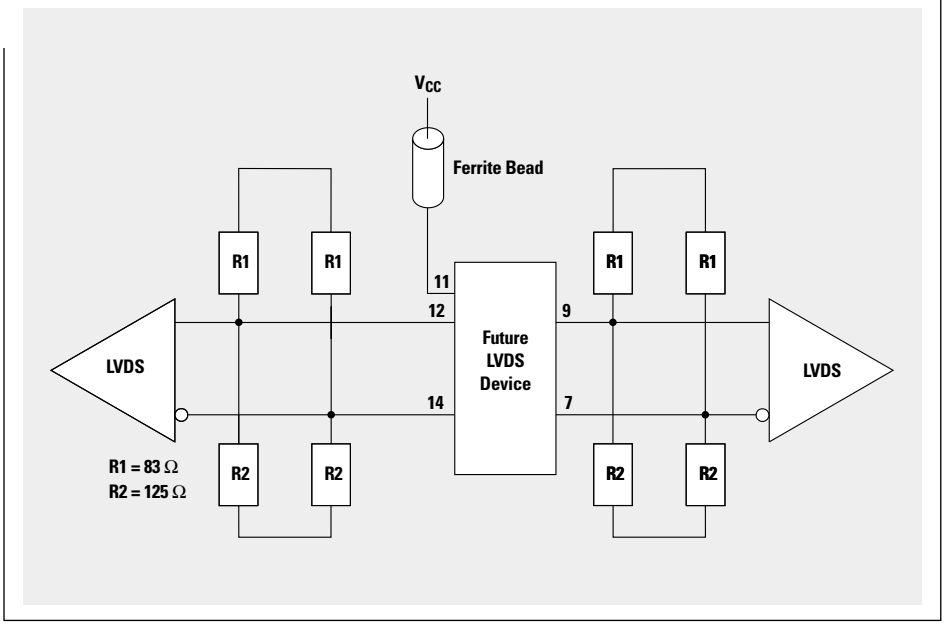
Related Web sites

www.ti.com/sc/interface

Get more product information at:

www.ti.com/sc/device/sn65lvds33
www.ti.com/sc/device/sn65lvds34
www-s.ti.com/sc/psheets/slls490/slls490.pdf

Figure 10. ECL-to-LVDS application



Designing for low distortion with high-speed op amps

By James L. Karki
Member, Group Technical Staff, High-Performance Linear

Introduction

The output of any amplifier contains the desired signal and unwanted signals. Noise is one unwanted output that is generated internally by the amplifier's components or is coupled in from external sources like the power supply or nearby circuitry. Distortion is another unwanted output that is generated when the amplifier's transfer function is non-linear.

In the formula of a straight line, y = b + mx, non-linearity refers to any deviation the output (y) may have from a constant multiple (m) of the input (x) plus any constant offset (b).

Many high-speed op amps use bipolar transistors as the basic active element to amplify the signal. In bipolar transistors, junction capacitances are a function of voltage, current gain is a function of collector current, collector current is influenced by collector-to-emitter voltage, transconductances are typically exponential functions, and so on. These all cause non-linear transfer functions.

When a transistor is driven into saturation or cut-off, it exhibits strong non-linearity. In this article, it is assumed that the devices are being operated below their saturation limits in what is typically referred to as linear operation.

Power series expansion

Expanding the non-linear transfer functions of basic transistor circuits into a power series is a typical way to quantify distortion products.[1] For example: assume a circuit has an exponential transfer function $y = e^x$, where x is the input and y is the output. Expanding e^x into a power series around x = 0 results in

$$e^x = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} + \frac{x^5}{120} + \cdots + \frac{x^n}{n!}.$$

Figure 1 shows the function $y = e^x$ along with estimates that use progressively more terms of the power series.

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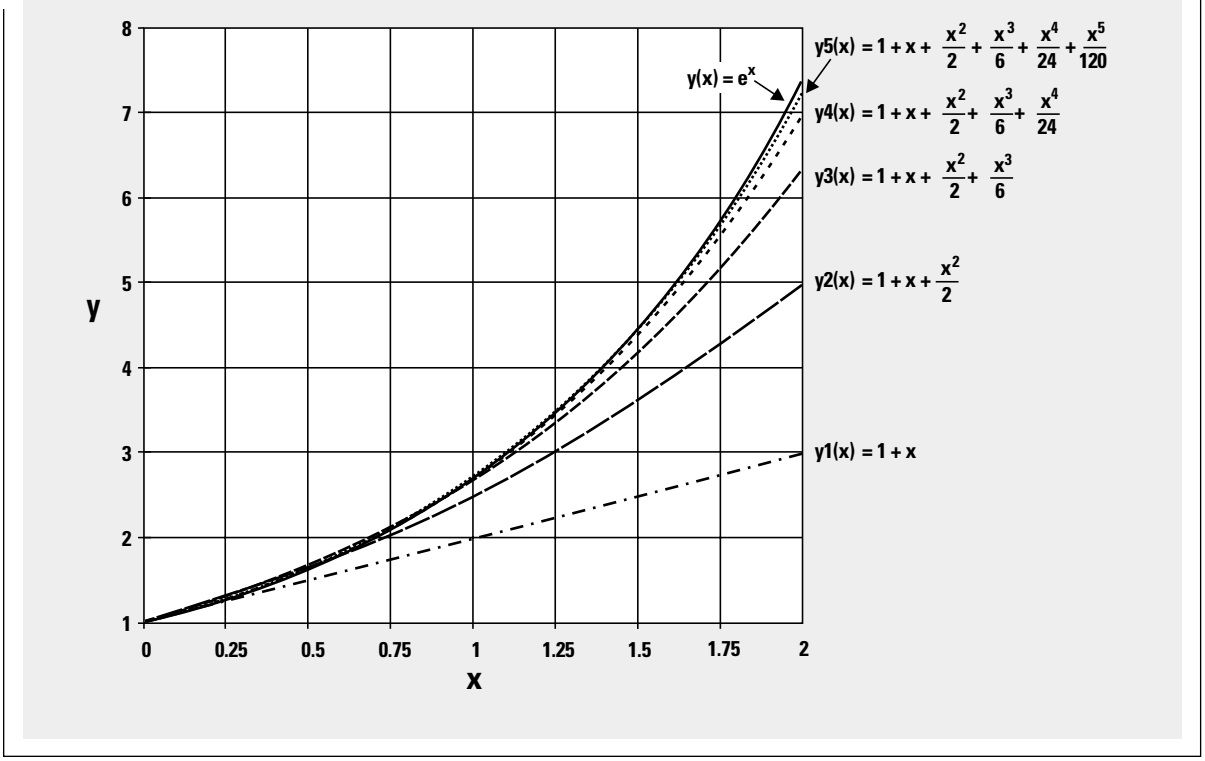
Figure 1. Function $y = e^x$ and its power series estimates



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The farther x is from 0, the more terms are required to properly estimate the value of e^x. If $x < 0.25$, then the linear term, $1 + x$, provides a close estimate of the actual function; and the circuit is linear. As x becomes larger, progressively more terms are required to properly estimate e^x, and the output now contains second-order, third-order, and higher distortion terms.

If the input to this circuit is a sinusoid, $x = \sin(\omega t)$, then trigonometric identities* show that the quadratic, cubic, and higher-order terms give rise to second-, third-, and higher-order harmonic distortion. In a similar manner,[2] if the input is comprised of two tones, then trigonometric identities show that the quadratic and cubic terms give rise to second-, third-, and higher-order intermodulation distortion.

Simplified op amp schematic

A simplified schematic of a high-speed op amp is shown in Figure 2. A simple feedback network and load resistor are included for completeness. A brief overview of its operation is given first for those unfamiliar with op amp circuit design.

*$\sin^2(\omega t) = \frac{1-\cos(2\omega t)}{2}$ and $\sin^3(\omega t) = \frac{3\sin(\omega t) - \sin(3\omega t)}{4}$

$V_{CC}+$ is the positive power supply input, and $V_{CC}–$ is the negative power supply input. $V_{IN}+$ and $V_{IN}–$ are the signal input pins, and V_{OUT} is the signal output. The op amp amplifies the differential voltage across its input pins to generate the output. By convention, the input voltage is the difference voltage, $V_{ID} = (V_{IN}+) – (V_{IN}–)$. It is amplified by the open-loop gain of the amplifier to produce the output voltage, $V_{OUT} = A_f V_{ID}$, where A_f is the frequency-dependent open-loop gain of the amplifier.

The input differential pair, Q1 and Q2, is balanced so the collector currents, I_{C1} and I_{C2}, are equal when the input differential voltage is zero. Applying a voltage across the input pins causes $I_{C1} \neq I_{C2}$.

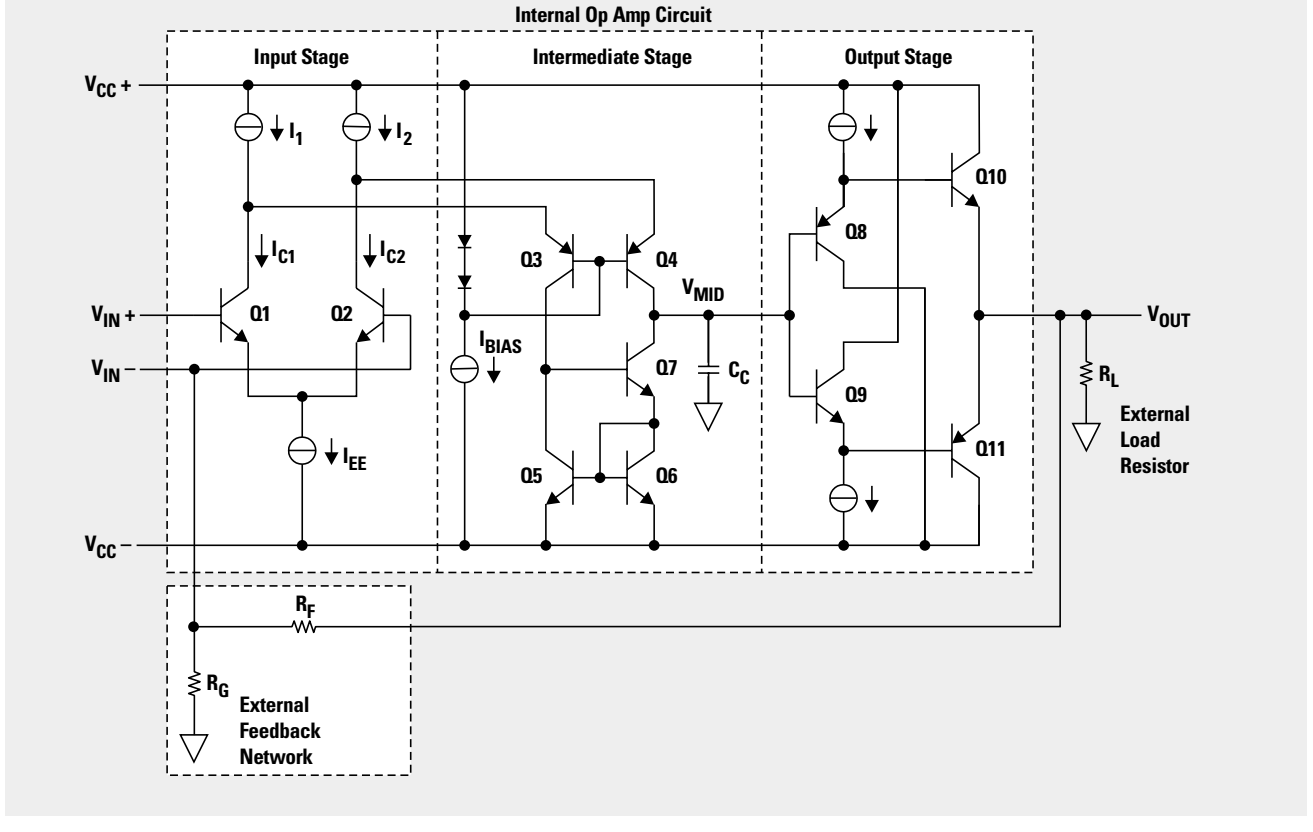
Q3 and Q4 fold the current from the input differential pair into the Wilson current mirror formed by Q5, Q6, and Q7. The mirror tries to maintain equal collector currents. Any difference current, $I_{C1} – I_{C2}$, develops a voltage at V_{MID}.

The capacitor, C_C, shown from V_{MID} to ground, is really multiple capacitors to the supply rails. It is used to stabilize the amplifier via dominant pole compensation.

V_{MID} is then buffered to the output via Q8 and Q10, or via Q9 and Q11, depending on polarity.

In the following discussion, we will examine the distortion mechanisms in each of these sub-circuits more closely.

Figure 2. Simplified high-speed op amp schematic



Intrinsic linearity

Intrinsic linearity refers to the linearity of each sub-circuit without the effect of feedback.

The input stage

The transfer function of the input differential pair is given in many texts.[3, 4] The input is the differential voltage, $V_{ID} = (V_{IN}+) - (V_{IN}-)$, and the output is the difference current, $I_{C1} - I_{C2}$, which is proportional to

$$\tanh\left(\frac{-V_{ID}}{2\times V_T}\right),$$

where V_T is the thermal voltage ($V_T \approx 26$ mV @ 25°C). Substituting

$$x = \frac{-V_{ID}}{2\times V_T}$$

and expanding tanh(x) around x = 0 in a power series, we find

$$\tanh(x) = x - \frac{x^3}{3} + \frac{2x^5}{15} - \cdots.$$

Since the power series contains no even-order terms, a perfect differential pair will not generate even-order harmonics. Figure 3 shows three estimates of y(x) = tanh(x), each using progressively more terms in the power series.

If $x < 0.25$, which corresponds to $V_{ID} < 0.5\ V_T$, the function is approximately linear; i.e., y1(x) = x. Under that condition, the input stage is very linear. With larger excursions, third- and fifth-order terms are required for an adequate approximation, and the input stage will distort the signal.

A typical high-speed op amp, without degeneration,** has a very large open-loop gain—on the order of 100 dB. Very small input voltages are required to keep the output from saturating. V_{ID} is normally much less than V_T, and the input stage is normally considered linear. For example: Assume that the output voltage swing is 10 V, with 100 dB of gain V_{ID} = 0.1 mV, which is much less than 0.5 $V_T \approx 13$ mV @ 25°C.

The intermediate stage

The difference current, $I_{C1} - I_{C2}$, from the input stage is the input to the intermediate stage; and the output is the voltage at V_{MID}. The voltage swing at V_{MID} in conjunction with the early voltages, V_A, and collector capacitances, C_J, of Q4 and Q7 causes non-linear behavior in the stage. The other transistors in the intermediate stage see very small voltage and current variations, and do not play a major role in distortion.

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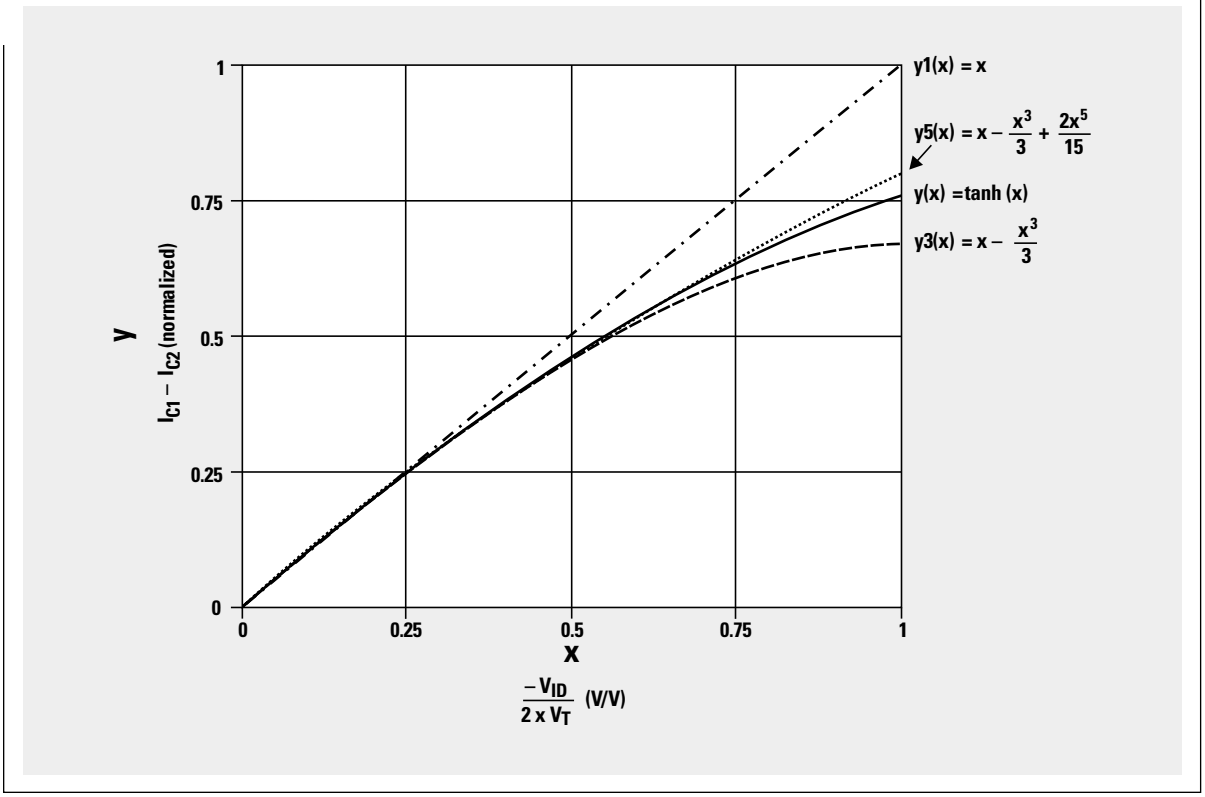
**Often emitter degeneration is used as part of the overall compensation scheme, where resistors are placed in the emitter leads of Q1 and Q2. This increases the linear input voltage range by reducing the gain.

Figure 3. Power series estimates of input pair transfer function



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Early voltage effects

V_A appears in the formula for a transistor's collector current:[3]

$$I_C = I_S \times \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE}}{V_A}\right),$$

where V_{BE} is the base emitter voltage, V_T is the thermal voltage, V_{CE} is the collector-to-emitter voltage, and I_S is the saturation current.

I_C comprises the input to the intermediate stage, and V_{CE} the output. Assuming that

$$I_S \times \exp\left(\frac{V_{BE}}{V_T}\right)$$

is linear should be valid, considering the previous discussion about the linearity of the input stage. As such, we can write a generalized formula for the intermediate stage: $y = zx(1+\alpha y)$, where y is V_{MID}, z is the impedance of the stage, x is the input current, and α depends on V_A. Rearranging gives us

$$y = \frac{zx}{1-zx\alpha}.$$

Using conservative numbers such as $z = 10^6$ and $\alpha = 100$, the power series expansion around x = 0 is: $10^6x + 10^{10}x^2 + 10^{14}x^3 + 10^{18}x^4 + 10^{22}x^5$ .... Figure 4 shows three estimates, each using progressively more terms in the power series—linear, quadratic, and cubic.

It can be seen that with voltage swings up to 4 V at V_{MID}, the linear term 10^6x is a close approximation, and it is expected that the transfer function is linear within these limits. At higher excursions, between 4 V and 12 V, the quadratic terms are required, resulting in second-order distortion products. Above 12 V, the cubic terms are required, giving rise to third-order distortion products.

Limiting voltage swings at V_{MID} reduces distortion due to the non-linear effects of V_A.

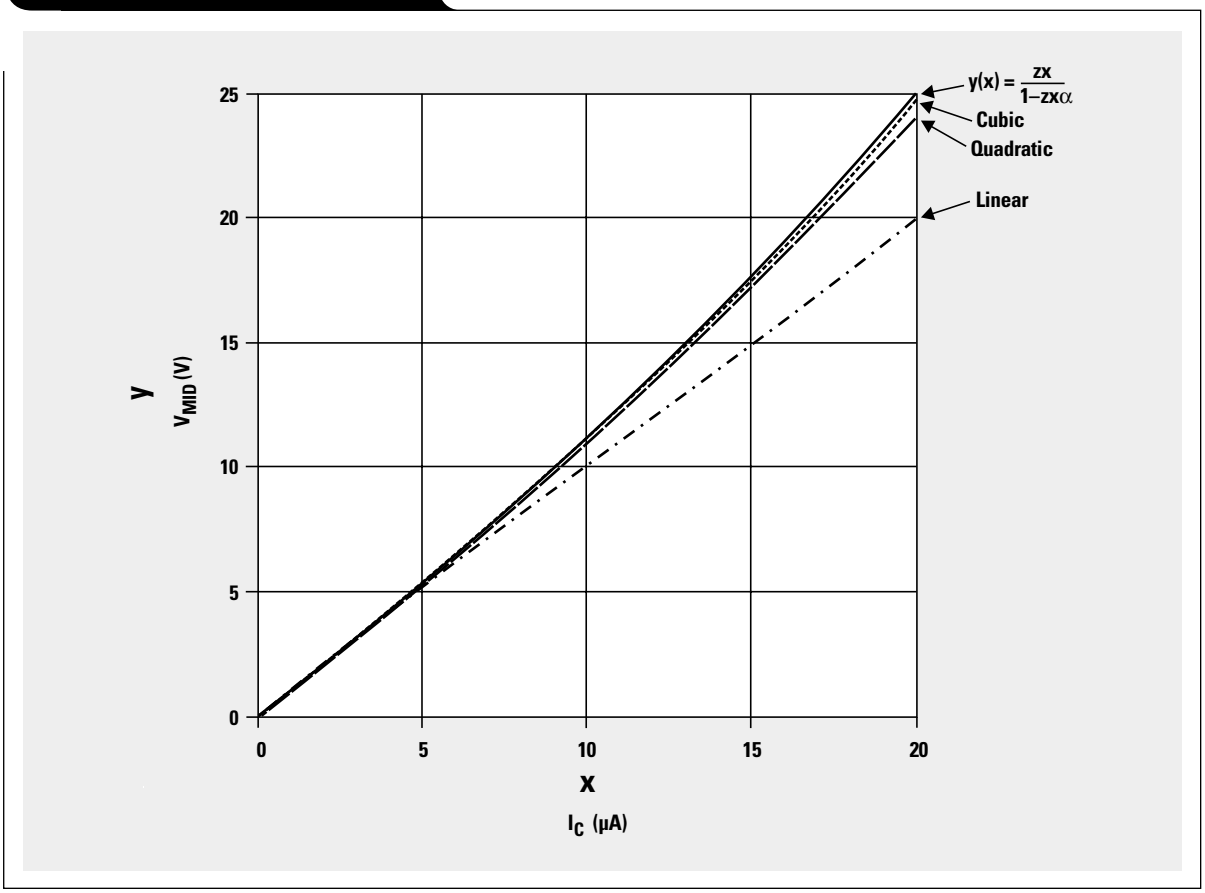
Junction capacitance effects

A simple model of junction capacitance[3] is given by the formula

$$C_J = \frac{C_O}{\sqrt[MJE]{1-\frac{V_J}{\psi_0}}},$$

where C_O is the zero-bias capacitance, V_J is the junction voltage, ψ_0 is the built-in potential, and MJE is the grading coefficient. The transfer function of the intermediate stage is influenced by this non-linear capacitance at V_{MID}.

Figure 4. Non-linear effect of V_A



Using $I_{C1} - I_{C2} = x$ and $V_{MID} = y$, we can write

$$y = x\left[Z \parallel \frac{1}{\omega\left(C_C + \frac{2 \times C_O}{\sqrt[MJE]{1 - y/\psi_0}}\right)}\right],$$

where Z is the linear, non-frequency-dependent impedance seen looking in the node V_{MID}; C_C is the dominant pole capacitor, and ω is the frequency in radians. At frequencies above the dominant pole, this can be simplified to

$$y = \frac{x}{\omega\left(C_C + \frac{2 \times C_O}{\sqrt[MJE]{1 - y/\psi_0}}\right)}.$$

With this equation, y cannot be solved for in closed form.

By looking at the impedance and taking y as the independent variable, we can write

$$Z_C(\omega) = \frac{1}{\omega\left(C_C + \frac{2 \times C_O}{\sqrt[MJE]{1 - y/\psi_0}}\right)}.$$

Typical numbers for TI's high-speed BiCom 1 process include: MJE = 3, $\psi_0 = 0.6$, $C_O = 200$ pF, and $C_C = 5$ pF. Using these values and setting $\omega = 10^6$, we can draw the plot shown in Figure 5. Again, power series estimates are shown that use progressively more terms of the series—linear, quadratic, and cubic.

With voltage swings of about 3 V_{PP}, the linear approximation is valid. At higher voltage swings, the quadratic and cubic terms are required, resulting in second- and third-order distortion products.

The effect of V_A is not frequency-dependent, but the effect of C_J is. Below the dominant pole of the amplifier, V_A dominates the non-linearity of the intermediate stage. Above the dominant pole, the non-linearity is a combination of the two. In either case, limiting the voltage swing at V_{MID} (and thus V_{OUT}) is the key to linear operation.

The output stage—Q8 through Q11

Q8 through Q11 form a double-buffered, class-AB output stage. The voltage at V_{MID} is buffered via these transistors to produce V_{OUT}. Depending on polarity, the signal path is either through Q8 and Q10, or through Q9 and Q11. The analysis is the same in either case. If we assume that the polarity is positive,

$$V_{OUT} = V_{MID} + V_{BE_{Q8}} - V_{BE_{Q10}}$$
$$= V_{MID} + V_T \times \ln\left(\frac{I_{C_8}}{I_{S_8}}\right) - V_T \times \ln\left(\frac{I_{C_{10}}}{I_{S_{10}}}\right).$$

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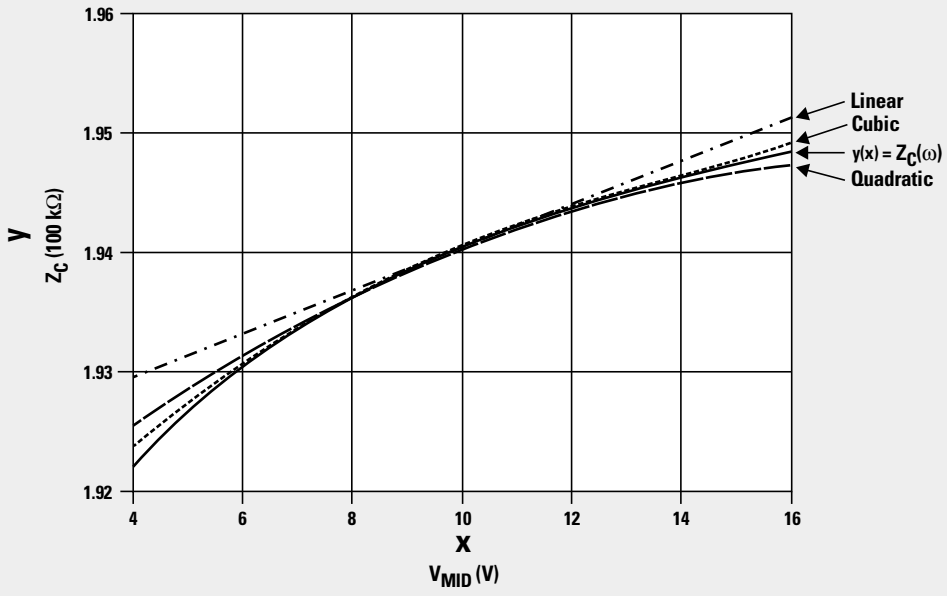
Figure 5. Non-linear C_J



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Q10 will see variations in collector current as it delivers power to the output load. Variations in Q8's collector current are reduced by the beta of Q10, resulting in $V_{BE_{Q10}}$ being the dominant non-linearity in the signal path from V_{MID} to V_{OUT}.

Again, using a power series expansion helps to highlight the nonlinear terms responsible for distortion. If we substitute

$$\frac{I_C}{I_S} = x$$

and expand the natural log function around the point x = a in a power series,

$$\ln(x) = \ln(a) + \frac{x-a}{a} - \frac{(x-a)^2}{2a^2} + \frac{(x-a)^3}{3a^3} + \cdots.$$

Figure 6, which uses typical numbers for V_{BE} = 0.6 V, shows three estimates that each use progressively more terms in the power series—linear, quadratic, and cubic.

Variations of 20% or more in collector current cause the output stage to become non-linear. Increasing the amplifier's load impedance reduces the current variations in the output transistors and helps to reduce distortion in the output stage.

A typical scenario may be an output stage that is designed for a quiescent bias current of 5 mA and can deliver up to 100 mA to the load—a 1:20 ratio. Under these circumstances, distortion in the output stage will dominate the intrinsic distortion of the amplifier.

Power-supply bypass capacitors

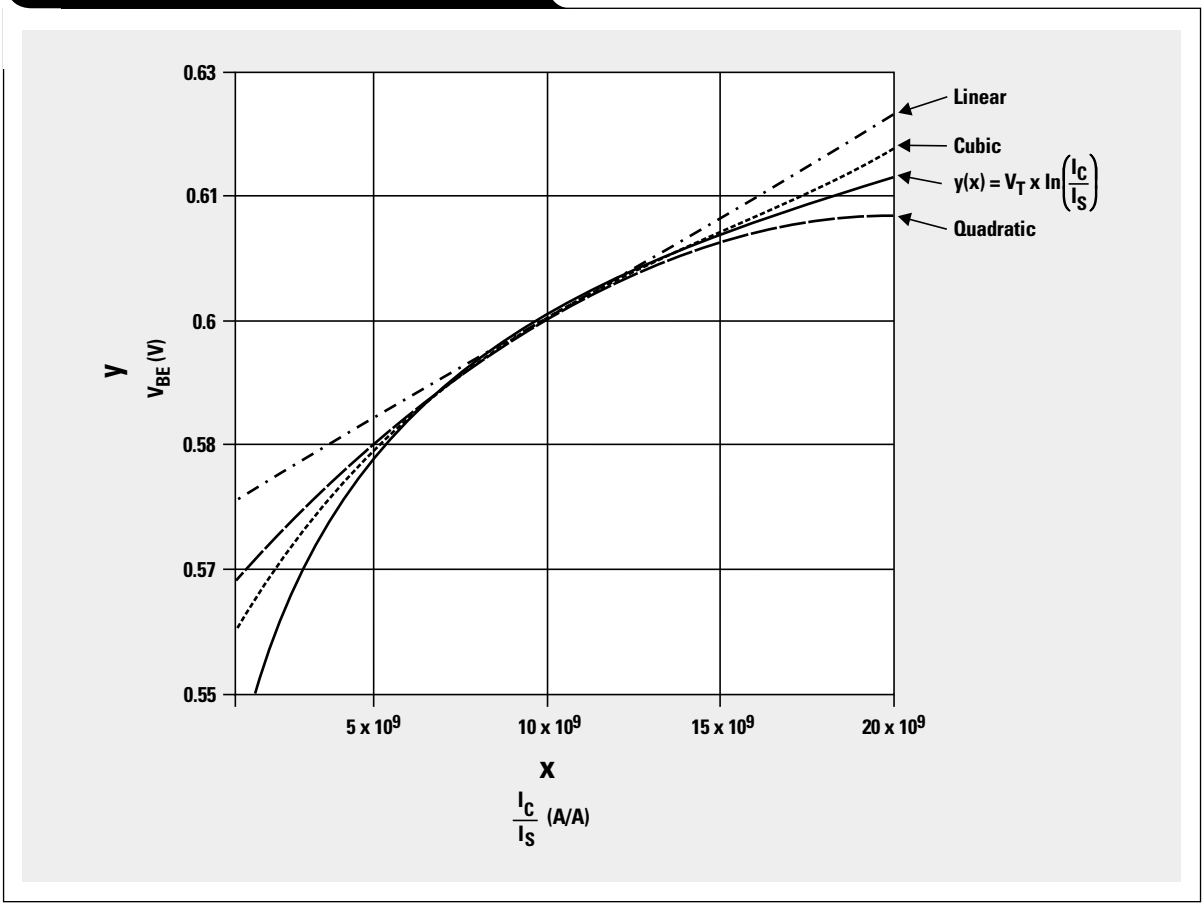
Figure 7 illustrates power-supply bypassing for a high-speed op amp. Current ($I_{CC}\pm$) supplied to the op amp from the power supply must pass through the distributed impedance between the power supply and the op amp. The distributed impedance is due to parasitic resistance and inductance in series with the power supply, and to stray capacitance to the ground plane. Due to the distributed impedance, bypass capacitors are required for high-speed operation.

The voltage drop across the resistance is negligible because the resistance is typically very small; but when the amplifier is required to output a fast rising (or falling) waveform, the series inductance can cause significant voltage drop:

$$V = L\frac{di}{dt}.$$

So what does this have to do with distortion? The voltage drop between V± and $V_{CC}\pm$ reduces the voltage across

Figure 6. Power series expansion of V_{BE}



the op amp, and the transistor operation moves towards saturation, causing significant distortion.

Bypass capacitors provide a local reservoir of energy used to support fast-rising transients, avoid dips in $V_{CC}\pm$, and keep the transistors out of saturation. The strategy shown uses bulk capacitors (typically 6.8 µF to 10 µF tantalum) within 1 inch of the power pins, along with high-frequency capacitors (0.01 µF to 0.1 µF ceramic) within 0.1 inch of the power pins.

The bulk capacitors store more energy but tend to have larger parasitic inductance and equivalent series resistance. For this reason, they can only provide energy at low frequencies. Due to the relaxed requirements for placement on the board, they are typically shared between several devices.

The high-frequency capacitors have lower inductance and equivalent series resistance, and are capable of supplying very fast di/dt. They are located as close as physically possible to the op amp power pins.

Using differential amplification to reduce even-order distortion

Differential signaling has been commonly used in audio, data transmission, and telephone systems for many years because of its inherent resistance to external noise sources. Today, differential signaling is becoming popular in high-speed data acquisition, where the analog-to-digital converter's (ADC's) inputs are differential and a differential amplifier is needed to properly drive them.

Another attractive advantage to differential signaling is that it significantly reduces even-order harmonics. This is easy to see by using a generic power series expansion of the output voltage.

A differential amplifier has two outputs that are ideally 180° out of phase: $(V_{OUT}+) = -(V_{OUT}-)$. The output is the differential voltage: $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$. If we assume that the amplifier is perfectly balanced, the generic expansion of each output is

$$(V_{OUT}+) = K_1(V_{IN}) + K_2(V_{IN})^2 + K_3(V_{IN})^3 + K_4(V_{IN})^4 + K_5(V_{IN})^5 \ldots$$

and

$$(V_{OUT}-) = K_1(-V_{IN}) + K_2(-V_{IN})^2 + K_3(-V_{IN})^3 + K_4(-V_{IN})^4 + K_5(-V_{IN})^5 \ldots,$$

where K_1 through K_5 are constants that depend on the characteristics of the amplifier. The odd-order terms retain their original polarity, but the even-order terms are always positive. Since V_{OUT} is the difference, the even-order terms cancel, but the odd-order terms increase by a factor of two:

$$V_{OUT} = 2K_1V_{IN} + 2K_3V_{IN}^3 + 2K_5V_{IN}^5 \ldots.$$

Balance is very important. Any imbalance in the two amplification paths will compromise the cancellation of even-order terms. Symmetrical layout and matched amplifiers are required.

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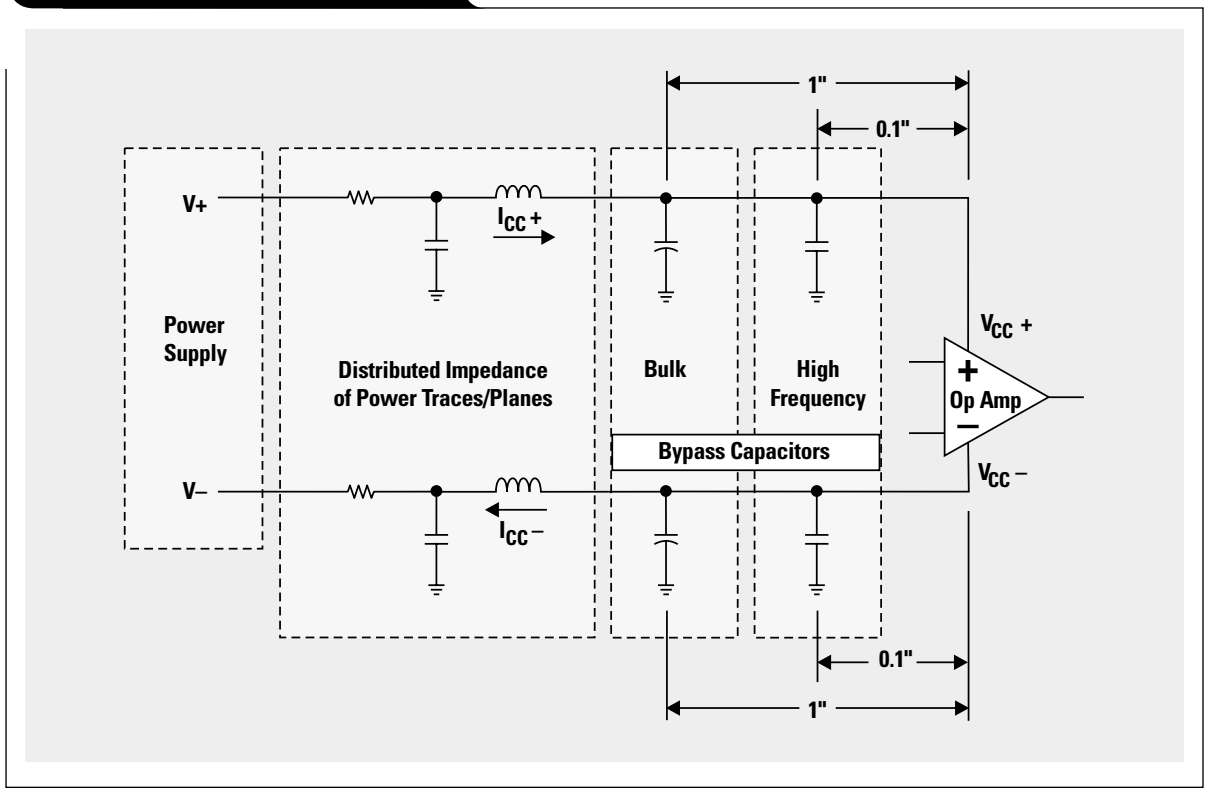
Figure 7. Power-supply bypassing



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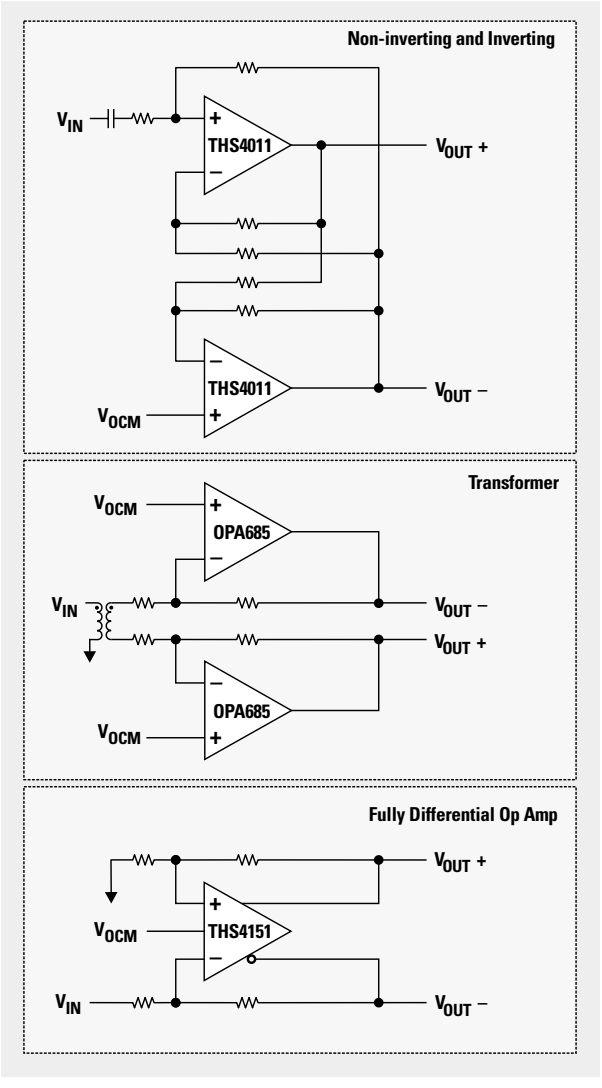
There are many ways to convert single-ended signals to differential signals, as shown in Figure 8. Some employ the use of transformers, multiple single-ended op amps, and various passive components. Integrated fully differential op amps are available that can provide a more elegant solution.

The curative effects of feedback

The curative effects of negative feedback refers to the effectiveness of negative feedback in reducing distortion. This effectiveness depends on the forward gain from the point where distortion is generated and the loop gain of the amplifier.

Figure 9 shows a block diagram of an op amp using negative feedback. The input stage is A1, the intermediate stage is A2, the output stage is the x1 buffer, and β is the feedback factor. The open-loop gain or forward gain of the amplifier is A_F = A1A2; the loop gain is $A_F\beta$ = A1A2β; and e1, e2, and e3 are generalized error sources. The following discussion analyzes the output response that is due to the individual error sources.

Figure 8. Single-ended to differential—alternative methods



An error source at the input stage, e1, is amplified by the full open-loop gain of the amplifier. If there is no feedback, setting all other sources to zero results in V_{OUT} = e1A1A2; but with feedback,

$$V_{OUT} = \frac{e1}{\beta + \frac{1}{A1A2}} \approx \frac{e1}{\beta}$$

if A1A2 >> 1. This means that e1 will be amplified by the closed-loop gain of the amplifier.

An error source at the intermediate stage, e2, is amplified only by A2. If there is no feedback, setting all other sources to zero results in V_{OUT} = e2A2; but with feedback,

$$V_{OUT} = \frac{e2}{A1\beta + \frac{1}{A2}} \approx \frac{e2}{A1\beta}$$

if A2 >> 1. Error source e2 is attenuated by A1β.

An error source at the output stage, e3, is buffered by a gain of +1 to the output. If there is no feedback, setting all other sources to zero results in V_{OUT} = e3; but with feedback,

$$V_{OUT} = \frac{e3}{1 + A1A2\beta} \approx 0$$

if A1A2β >> 1. Error source e3 is attenuated by the loop gain, A1A2β = $A_F\beta$.

Distortion in a high-speed op amp is attributed mainly to the intermediate and output stages. Distortion is reduced by taking advantage of the effect of loop gain in negative feedback. However, be aware that, in a voltage-feedback (VFB) op amp, loop gain decreases linearly with frequency, and so does its effects on reducing distortion.

Design guidelines for low distortion

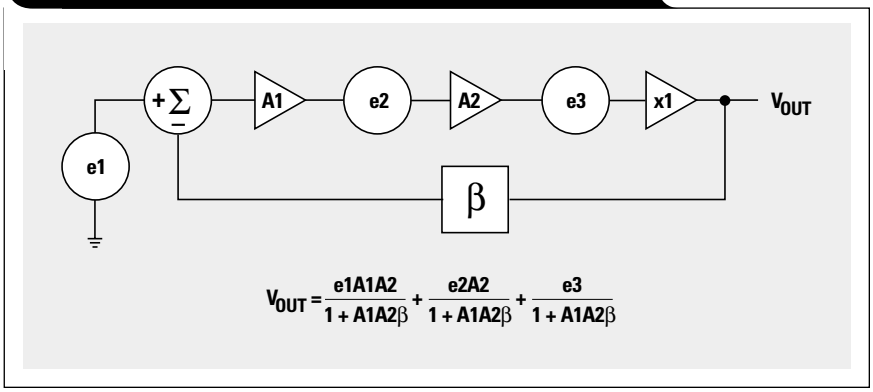
How does one go about designing for low distortion with high-speed op amps? The following are important design considerations.

Op amp selection

1. Look for an amplifier with low intrinsic distortion, high open-loop gain at the frequencies of operation, and high slew rate.
2. For VFB op amps, gain bandwidth (GBW) products in the gigahertz range may be required to provide enough loop gain to reduce distortion significantly in the range of 10 MHz to 100 MHz.
3. Current feedback (CFB) op amps have much higher slew rates than VFB op amps. If the output cannot track the input because of slew rate limitations, the effectiveness of negative feedback is null and void. For this reason, CFB op amps can provide lower distortion in high-frequency applications.
4. For high-gain applications, use decompensated op amps. Decompensated op amps sacrifice stability at lower gain for higher GBW, higher slew rate, and lower noise. They are easily spotted in data books and selection guides by their minimum gain requirements.

5. CFB op amps allow you to optimize loop gain by selecting the feedback resistor value based on the closed-loop gain of the amplifier. At higher gains, lower-feedback resistors can be used without sacrificing stability.[5]

Figure 9. Model of op amp with negative feedback



Circuit design

1. Reduce loading on the amplifier output as much as possible. A common practice when driving an ADC is to make a simple RC filter by placing a small series resistor and load capacitor to ground (or differentially). At the pole frequency, the impedance of the capacitor equals the resistor and the amplifier sees a significant load. Avoid loading the amplifier by using an active filter topology (like MFB, Sallen-Key, or simply a capacitor in parallel with the feedback resistor) to make the amplifier's gain roll off before the pole frequency of the output RC.
2. Use power-supply bypass capacitors. Place bulk capacitors in the range of 6.8 µF to 10 µF within 1 inch of the power pins, and high-frequency capacitors in the range of 0.01 µF to 0.1 µF within 0.1 inch of the power pins. Bulk capacitors typically have been tantalum, but high-value ceramics that may be viable are now available. High-frequency bypass capacitors are normally ceramic.
3. Minimize output voltage swings.
4. Minimize gains. Lower closed-loop gain = higher loop gain.
5. Fully differential architectures help reduce even-order distortion products and are resistant to extraneous common-mode noise sources. Most high-speed ADCs now use differential inputs, and differential amplification is commonly required. Integrated fully differential amplifiers can provide a viable solution.
6. The feedback path is critical. High-speed op amps are very susceptible to the effects of parasitic capacitance. Remove ground plane(s) from under the input pins and any traces leading to them, and use minimum-value feedback resistors. The idea is to avoid creating RC phase lags that decrease the amplifier's phase margin. The resulting peaking and group delay may cause distortion of non-sinusoidal signals.

Conclusion

We have looked at each stage of a simplified high-speed op amp and quantified the main distortion mechanisms. Most of the distortion is produced by the intermediate stage and the output stage due to their dynamic nature.

Reducing the voltage swings at the output and increasing the impedance of external loads will increase the intrinsic linearity of the amplifier. Higher loop gain increases the curative effects of negative feedback.

As frequency increases, the effects of nonlinear parasitic junction capacitance increase, and the curative effects of loop gain diminish. These combine to make distortion more problematic as frequency increases.

Choosing the right amplifier is key. High slew rate and high GBW are two important parameters. CFB op amps can provide for lower distortion, especially at high frequency.

Differential amplification reduces even-order harmonics and is important in driving high-speed ADCs.

Power-supply bypass capacitors are very important at high frequency due to the distributed impedance between the power supply and the op amp.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

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1. Piet Wambacq and Willy Sansen, *Distortion Analysis of Analog Integrated Circuits* (Kluwer Academic Publishers, 1998).	—
2. Christian Henn, *Intermodulation Distortion (IMD)*, Burr-Brown Application Bulletin AB-194.	—
3. Paul R. Gray and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. (John Wiley and Sons, Inc., 1993).	—
4. Donald O. Pederson and Kartikeya Mayaram, *Analog Integrated Circuits for Communications* (Kluwer Academic Publishers, 1991).	—
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Related Web sites

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An audio circuit collection, Part 3

By Bruce Carter
Advanced Linear Products, Op Amp Applications

Introduction

This is the third in a series of articles on single-supply audio circuits. The reader is encouraged to review Parts 1 and 2, which appeared in the November 2000 and February 2001 issues, respectively, of *Analog Applications Journal*. Part 1 concentrated on low-pass and high-pass filters. Part 2 concentrated on audio-notch-filter applications and curve-fitting filters. Part 3 focuses on the use of a simulated inductor as an audio circuit element.

The simulated inductor

The circuit in Figure 1 reverses the operation of a capacitor, simulating an inductor. An inductor resists any change in current, so when a dc voltage is applied to an inductance, the current rises slowly, and the voltage falls as the external resistance increases.

In practice, the simulated inductor operates differently. The fact that one side of the inductor is grounded precludes its use in low-pass and notch filters, leaving high-pass and band-pass filters as the only possible applications.

High-pass filter

Figure 2 shows a 1-kHz high-pass filter using a simulated inductor. The response of this high-pass filter is disappointing, as shown in Figure 3.

R_S is the equivalent series resistance of the inductor and capacitor. Various values of series resistance were tried. Only the R_S values ranging from 220 Ω to 470 Ω gave something close to the expected response. The 220-Ω and 100-Ω resistors provided the most rejection, but there is an annoying high-frequency roll-off that first shows up at 330 Ω and becomes quite pronounced at 100 Ω. Resistance

Figure 1. Simulated inductor circuit

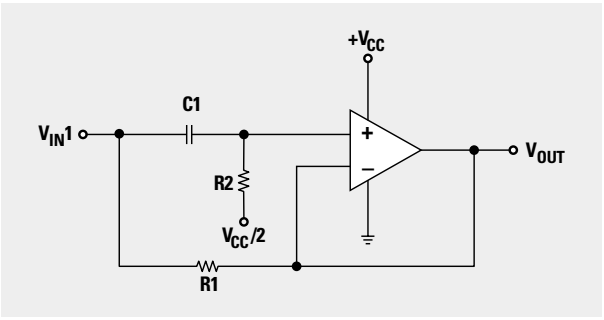


Figure 2. High-pass filter made with a simulated inductor

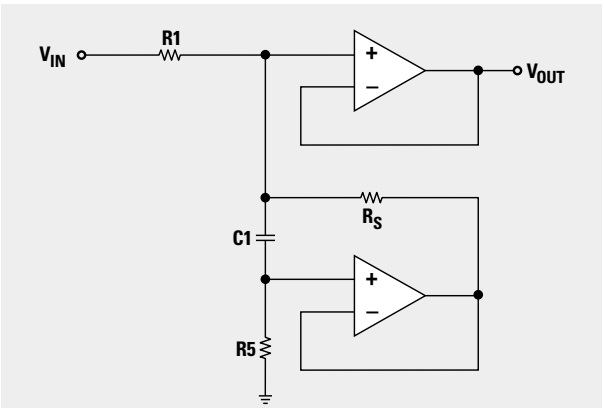
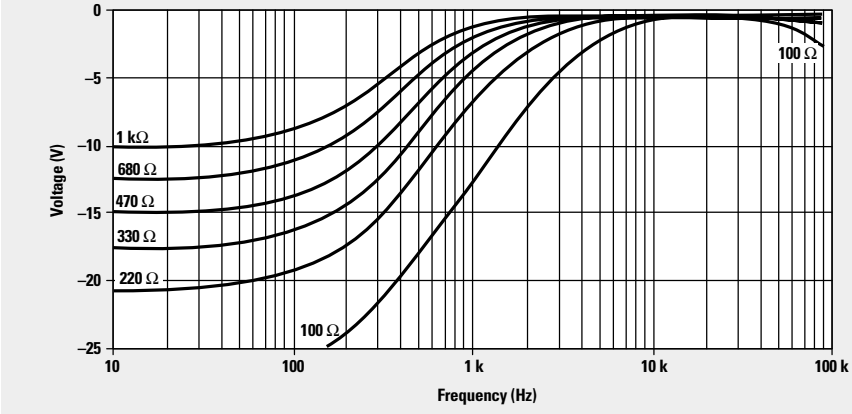


Figure 3. Response of a simulated inductor high-pass filter



values of 470 Ω and above have washed out stop-band rejection, but they at least have a flat high-frequency response.

The value of R_S that gives the most inductive response is 330 Ω, although it rolls off slightly more than 3 dB at 1 kΩ and is not 20 dB down a decade away. If high-frequency roll-off is not desirable, 470 Ω should be used, but maximum attenuation will be only about 15 dB. A high-pass filter constructed from a simulated inductor has poor performance and is not practical. This leaves band-pass filters as the only potential application for simulated inductors.

Band-pass filters and graphic equalizers

A series resistance of 220 Ω to 470 Ω is relatively high, which means that only relatively low-Q band-pass filters can be constructed with simulated inductors. There is an application that can use low-Q band-pass filters—graphic equalizers.

Graphic equalizers are used to compensate for irregularities in the listening environment or to tailor sound to a listener's preferences. Graphic equalizers are commonly available as 2-octave (5 bands) or 1-octave (10 or 11 bands). Professional sound re-enforcement systems utilize ⅓-octave equalizers (about 30 bands).

An octave is a repeating pattern of pitch used in musical scales. To the ear, a tone played at a given frequency has the same pitch as a tone at half or double the frequency, except for an obvious difference in frequency. Western cultures have divided octaves into 8 notes, Eastern cultures into 5 notes.

The center frequencies for a ⅓-octave equalizer are not equally spaced. The ear hears pitch logarithmically, so the center frequencies must be determined by using the cube root of 2 (1.26). The center frequencies are listed in Appendix A.

Graphic equalizers do not have to be constructed on octave intervals. Any set of center frequencies can be utilized. Musical content, however, tends to stay within octaves; so graphic equalizers that do not follow the octave scale may produce objectionable volume shifts when artists play or sing different notes within the octave. One of the latest trends is to compensate for poor response in small audio systems by moving the high- and low-frequency settings in from their extremes and placing the equalization frequencies at 100, 300, 1000, 3000, and 10000 Hz. It looks nicer on the front panel, makes more efficient use of the limited capabilities of such systems, but is musically incorrect.

Two strategies can be used to create graphic equalizers—the simulated inductor method and the MFB band-pass filter method. Reference 1 describes the MFB method in detail; this article is concerned with the use of simulated inductors and their use in a graphic equalizer.

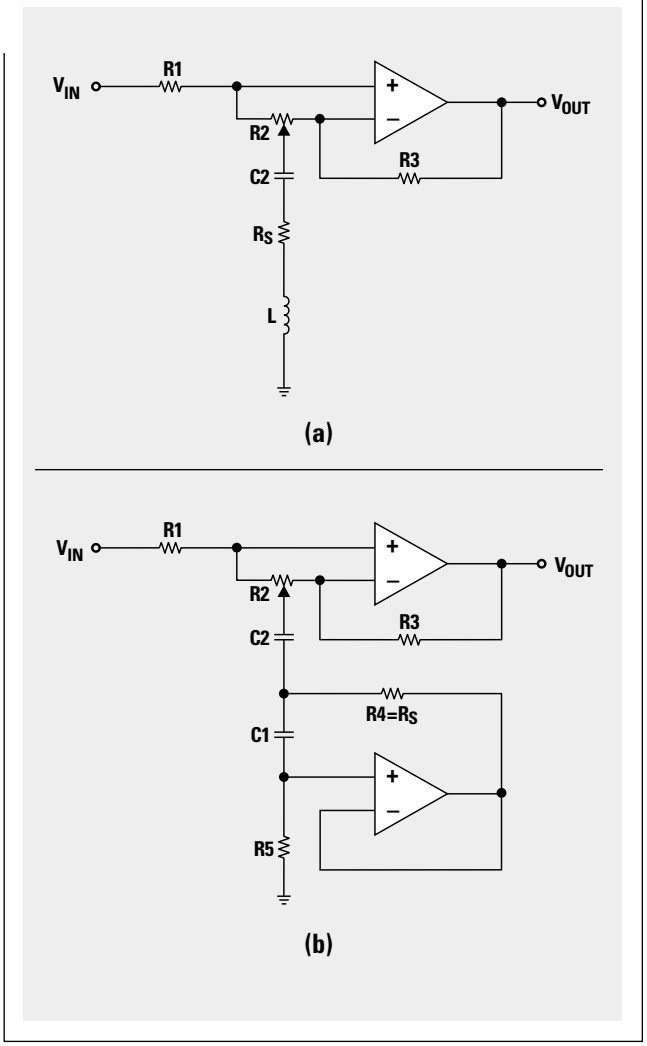
Building the equalizer

Start with $R_S \cong 470\ \Omega$.

A graphic equalizer can be built with stages based on the circuits shown in Figure 4.

Obtaining real inductors of the correct values would be difficult. It is much easier to use the simulated inductor

Figure 4. Graphic equalizer



implementation shown in Figure 4b, where R_S is approximately equal to R4. R4 does not include a negligible contribution from capacitor C2.

Gain of the equalizer

Now the gain of the circuit can be calculated. Selecting $R_S \cong 470\ \Omega$ constrains the input and feedback resistor of the graphic equalizer stage. Several sources use a gain of 17 dB. This gain, however, will appear only when the surrounding stages are also adjusted to their maximum level. Otherwise, the gain at the resonant stage will experience roll-off from adjacent stages according to their proximity and Q.

The potentiometer in Figure 4 is connected across the inverting and non-inverting inputs of the op amp and is in parallel with r_{id}, the differential input resistance. Therefore, it does not enter into the gain calculations for the op amp

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stage. R_S does, however. The equivalent circuit with the potentiometer at each end of its travel is shown in Figure 5.

The circuit in Figure 5a acts like a unity gain buffer, with a voltage divider on the input voltage. The gain will be at its minimum value of –17 dB (1/7). For R_S = 470 Ω, R1 can be calculated:

$$R1 = \frac{R_S}{A} - R_S = \frac{470\ \Omega}{7} - 470\ \Omega = 2820\ \Omega.$$

The circuit in Figure 5b acts like a non-inverting gain stage, with the input resistance R1 being ignored. The gain will be at its maximum value of 17 dB (7). For R_S = 470 Ω, the feedback resistor R3 is

$$R3 = R_S(A-1) = 470\ \Omega \times (7-1) = 2820\ \Omega.$$

This is the same value, which simplifies design. A standard E-6 value of 3.3 kΩ is selected for both, because the absolute value of gain is unimportant.

Potentiometer action

The gain at points between the ends of the potentiometer wiper travel is more difficult to calculate. It will combine both non-inverting and inverting gains. Superficially, the circuit looks like a differential amplifier stage, but the resistor values are not balanced for differential operation. This leads to an unusual taper for the potentiometer. One value of resistance for the potentiometer, in this case 20 kΩ, has ½ gain/loss at the 5% and 95% settings,

Figure 5. Equivalent circuits with gain at either end of potentiometer travel

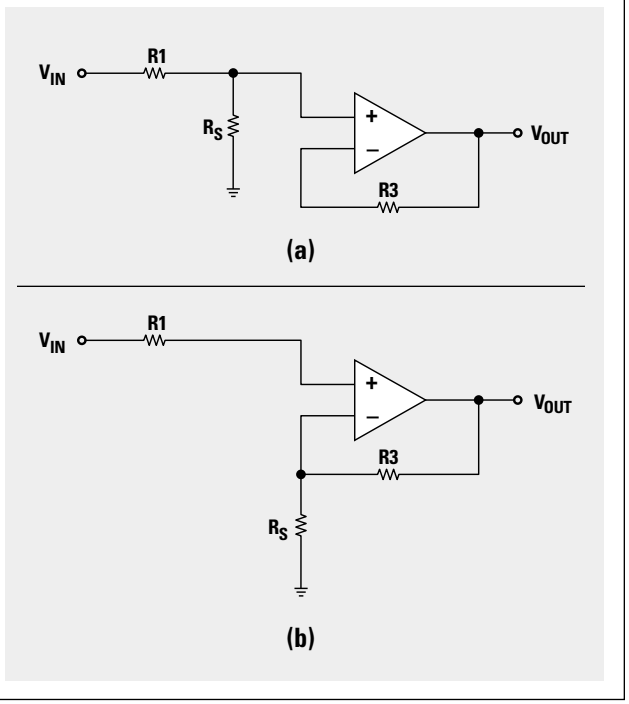
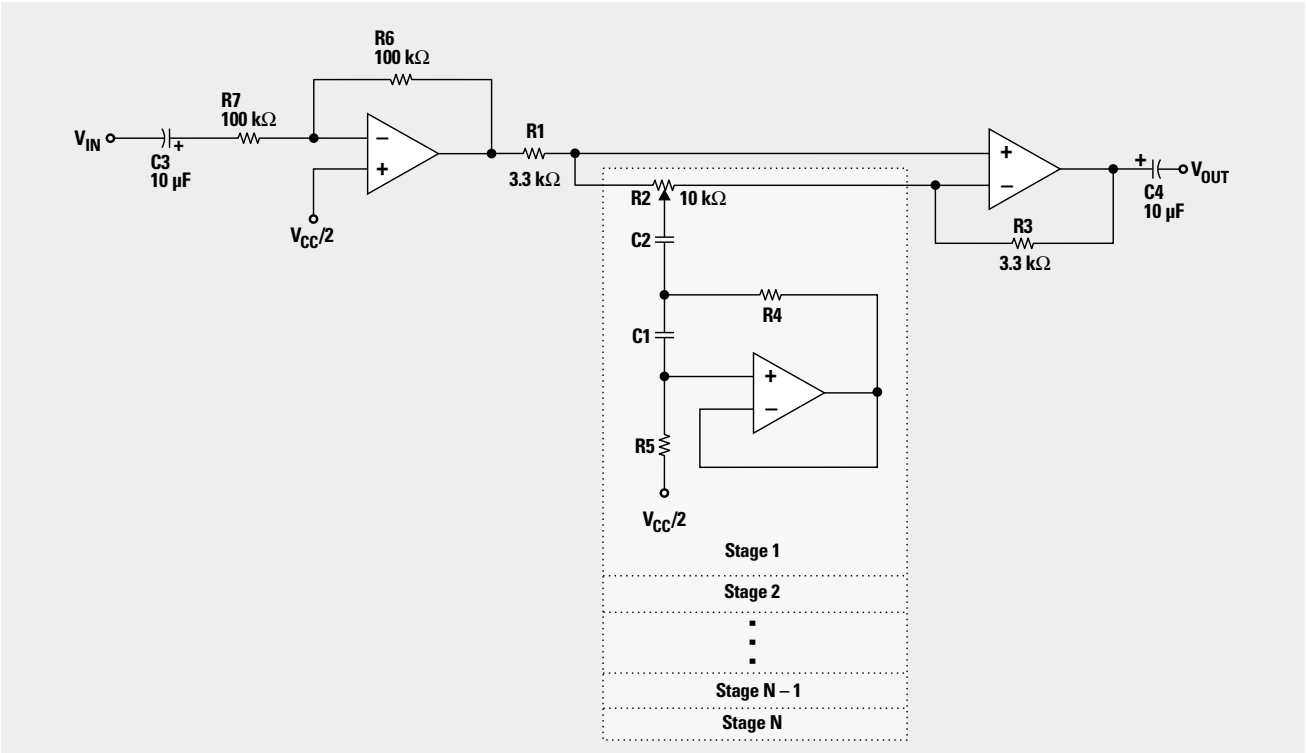


Figure 6. Graphic equalizer schematic

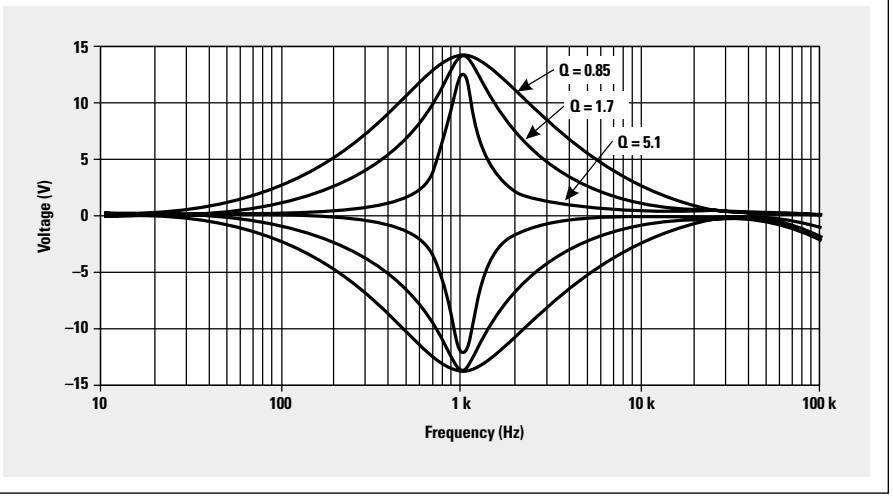


respectively. This requires a potentiometer with two logarithmic (audio) tapers joined in the center. This taper is non-standard and hard to obtain.

A partial solution to this is to reduce the value of the potentiometer. A value of 10 kΩ will diminish the logarithmic effects somewhat. Reducing the potentiometer to 5 kΩ will result in less improvement and will start to limit the bandwidth of the op amp. The best compromise is probably 10 kΩ.

Figure 6 shows the schematic of the equalizer. Capacitors C3 and C4 ac-couple the input and output, respectively. The first stage is an inverting unit gain buffer that insures that the input is buffered to drive a large number of stages. It also allows easy injection of the half-supply voltage to the equalization stages. The equalization stages are shown by the dotted lines. R5 is selected to be 100 kΩ. There may be some slight variation of R4 and R5 values to make capacitor values reasonable. The component values of the equalization stages are given in Appendix A.

Figure 7. Effect of Q on bandwidth for a graphic equalizer



Q and bandwidth

At this point, the designer needs to know the Q, which is based on how many bands the equalizer will have. The Q determines the bandwidth of a band-pass filter.

Different references suggest different values of Q, based on the ripple tolerable when all controls are set at their maximum or minimum values. This ripple is not desirable. If an end user is adjusting all controls to maximum, he needs a pre-amplifier, not an equalizer. Nevertheless, the maximum/minimum positions provide a good way to demonstrate the response capability of the unit.

Reference 2 recommends a Q of 1.7 for an octave equalizer. This value does give a ripple of 2.5 dB, which is reasonable for this type of device. Extending the line of reasoning, the Q of a 2-octave equalizer should be 0.85, and that of a ⅓-octave equalizer should be 5.1. The response of an equalizer stage with these Q values is shown in Figure 7.

A filter with a Q of 1.7 (Figure 7) will have a bandwidth that is 1/1.7, or 0.588 of the center frequency. Thus, the 1000-Hz filter with a Q of 1.7 has a bandwidth of 588 Hz. The –3-dB points, therefore, would be logarithmically equidistant from the center peak at 1 kHz, at approximately 750 Hz and 1350 Hz, respectively. Beyond the –3-dB points, the response of the filter flattens out to a first-order response of –6 dB per octave, eventually flattening to a limiting value. Increasing the Q does nothing to change this, as Figure 7 demonstrates. The only thing that increasing the Q accomplishes is to narrow the –3-dB bandwidth.

Capacitor values

The relationships that are known at this point are:

Inductive reactance:

$$X_L = 2\pi \times f_o \times L$$

Definition of Q:

$$Q = \frac{X_L}{R}, \quad \text{where R is R4}$$

Resonant frequency calculation:

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \quad \text{where C is C2}$$

Formula for simulated inductor:

$$L = (R5 - R4) \times R4 \times C1$$

After deriving the following from the expressions above, the value of C1 and C2 can be determined in terms of f_o, R4, and R5.

$$C1 = \frac{Q \times R4}{2\pi \times f_o \times (R5 - R4)}$$

$$C2 = \frac{1}{2\pi \times f_o \times R4}$$

The values of C1 and C2 for each value of frequency are shown in Appendix A.

Response

The response curves for equalizers with potentiometers at each extreme are shown in Figures 8–11.

References

1. Elliott Sound Products, Projects 28 and 64, http://sound.au.com
2. *Audio/Radio Handbook*, National Semiconductor (1980).

Related Web sites

www.ti.com/sc/opamps
www.ti.com/sc/audio

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Figure 8. Response of a 2-octave equalizer

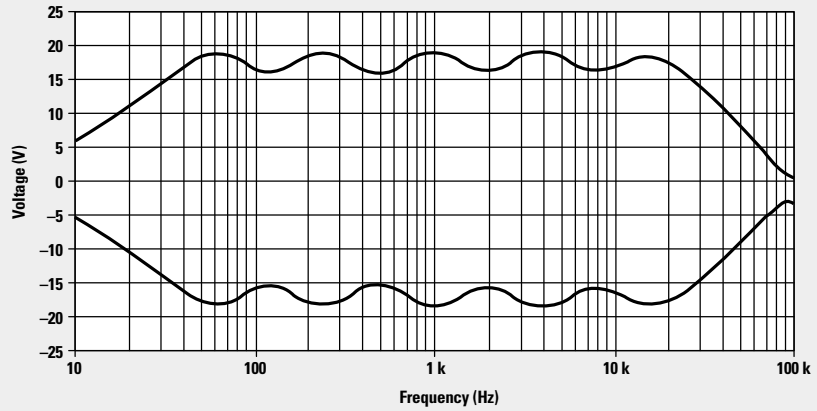


Figure 9. Response of a pseudo 2-octave equalizer

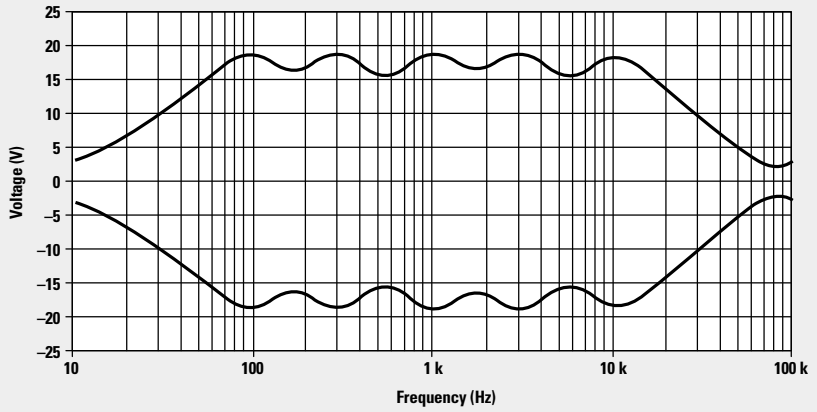


Figure 10. Response of a 1-octave equalizer

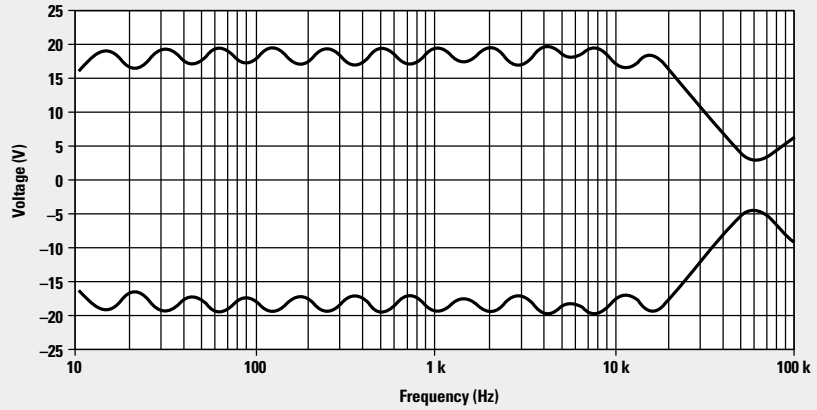
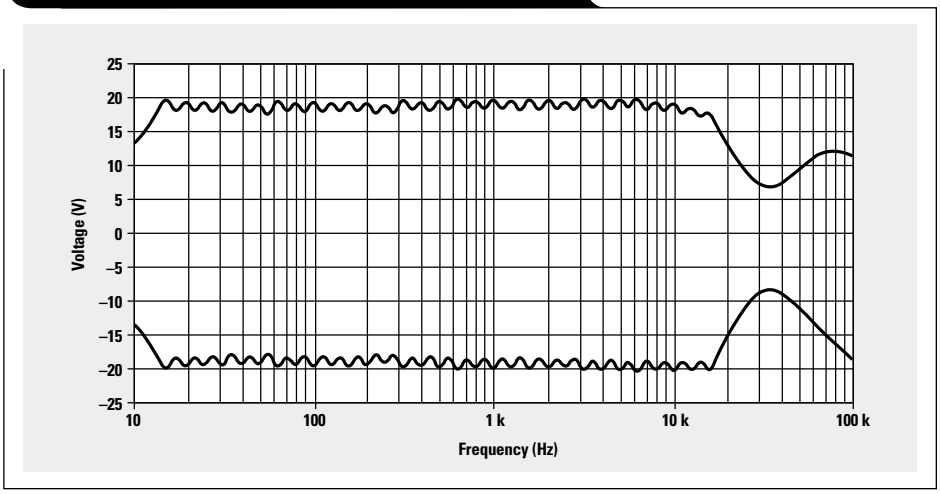


Figure 11. Response of a ⅓-octave equalizer



Appendix A. Component values for graphic equalizers

Use standard E-24 capacitor values nearest to the value calculated in the table.

Some ⅓-octave equalizers omit the 16- and 20-Hz bands; others omit the 20-kHz band. The frequencies are so close that 1% resistors are mandatory for this design.

Table 1. Component values for a 2-octave equalizer

FREQ	R5	R4	Q	L	C1	C2
60	100000	510	0.85	1.150	2.3E-08	6.1E-06
250	100000	470	0.85	0.254	5.4E-09	1.6E-06
1000	100000	470	0.85	0.064	1.4E-09	4.0E-07
4000	100000	470	0.85	0.016	3.4E-10	1.0E-07
16000	100000	470	0.85	0.004	8.5E-11	2.5E-08

Table 2. Component values for a pseudo 2-octave equalizer

FREQ	R5	R4	Q	L	C1	C2
100	100000	470	1	0.748	1.6E-08	3.4E-06
300	100000	470	1	0.249	5.3E-09	1.1E-06
1000	100000	470	1	0.075	1.6E-09	3.4E-07
3000	100000	470	1	0.025	5.3E-10	1.1E-07
10000	100000	470	1	0.007	1.6E-10	3.4E-08

Table 3. Component values for a 1-octave equalizer

FREQ	R5	R4	Q	L	C1	C2
16	110000	470	1.7	7.948	1.5E-07	1.2E-05
31	110000	470	1.7	4.102	8.0E-08	6.4E-06
63	100000	470	1.7	2.018	4.3E-08	3.2E-06
125	100000	470	1.7	1.017	2.2E-08	1.6E-06
250	100000	470	1.7	0.509	1.1E-08	8.0E-07
500	100000	470	1.7	0.254	5.4E-09	4.0E-07
1000	100000	470	1.7	0.127	2.7E-09	2.0E-07
2000	100000	470	1.7	0.064	1.4E-09	1.0E-07
4000	100000	470	1.7	0.032	6.8E-10	5.0E-08
8000	100000	470	1.7	0.016	3.4E-10	2.5E-08
16000	100000	470	1.7	0.008	1.7E-10	1.2E-08

Table 4. Component values for a ⅓-octave equalizer

FREQ	R5	R4	Q	L	C1	C2
16	100000	499	5.1	25.315	5.1E-07	3.9E-06
20	105000	475	5.1	19.278	3.9E-07	3.3E-06
25	100000	511	5.1	16.591	3.3E-07	2.4E-06
31	97600	499	5.1	13.066	2.7E-07	2.0E-06
40	100000	499	5.1	10.126	2.0E-07	1.6E-06
50	100000	499	5.1	8.101	1.6E-07	1.3E-06
63	100000	487	5.1	6.274	1.3E-07	1.0E-06
80	100000	511	5.1	5.185	1.0E-07	7.6E-07
100	100000	499	5.1	4.050	8.2E-08	6.3E-07
125	105000	487	5.1	3.162	6.2E-08	5.1E-07
160	100000	499	5.1	2.531	5.1E-08	3.9E-07
200	105000	475	5.1	1.928	3.9E-08	3.3E-07
250	100000	511	5.1	1.659	3.3E-08	2.4E-07
315	97600	499	5.1	1.286	2.7E-08	2.0E-07
400	100000	499	5.1	1.013	2.0E-08	1.6E-07
500	100000	499	5.1	0.810	1.6E-08	1.3E-07
630	100000	487	5.1	0.627	1.3E-08	1.0E-07
800	100000	475	5.1	0.482	1.0E-08	8.2E-08
1000	100000	499	5.1	0.405	8.2E-09	6.3E-08
1200	100000	511	5.1	0.346	6.8E-09	5.1E-08
1600	100000	499	5.1	0.253	5.1E-09	3.9E-08
2000	105000	475	5.1	0.193	3.9E-09	3.3E-08
2500	100000	511	5.1	0.166	3.3E-09	2.4E-08
3200	105000	499	5.1	0.127	2.4E-09	2.0E-08
4000	100000	499	5.1	0.101	2.0E-09	1.6E-08
5000	100000	499	5.1	0.081	1.6E-09	1.3E-08
6300	100000	487	5.1	0.063	1.3E-09	1.0E-08
8000	100000	475	5.1	0.048	1.0E-09	8.2E-09
10000	100000	499	5.1	0.041	8.2E-10	6.3E-09
12000	100000	511	5.1	0.035	6.8E-10	5.1E-09
16000	100000	499	5.1	0.025	5.1E-10	3.9E-09
20000	105000	475	5.1	0.019	3.9E-10	3.3E-09

Audio power amplifier measurements

By Richard Palmer
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Introduction

Characterization is an important step when a part is released to production. The data sheet is the medium through which the manufacturer relates this information to the customer. It is of paramount importance that the information on the data sheet be relevant and clear. It is sometimes beneficial for the customer to re-create these characterization measurements in order to evaluate a device in his system.

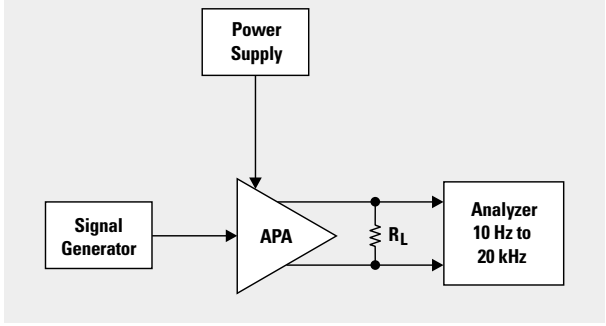
The primary goal of audio characterization measurement is to determine the performance of a device in the audible spectrum—20 Hz to 20 kHz. Although most people do not hear frequencies below 50 Hz nor above 15 kHz, the broader spectrum is an industry standard and allows more accurate comparison of devices. A method for measuring standard data sheet information is presented for several key parameters: total harmonic distortion plus noise (THD+N) versus output power (P_O) and frequency; gain and phase versus frequency; and crosstalk and noise versus frequency.

Basic measurement system

This article provides the guidelines for measuring the parameters of Texas Instruments audio power amplifiers (APAs). The measurements were made using off-the-shelf evaluation modules (EVMs) that are compatible with the TI Plug-n-Play platform. EVMs for the TPA2001D1 and TPA731 were used for all but the crosstalk measurement, which requires a stereo device. TPA2001D2 and TPA0212 EVMs were used for the crosstalk measurements.

Figure 1 shows the block diagram of a basic measurement system for class-AB amplifiers. These amplifiers are relatively easy to measure since they are linear—the output is a linear representation of the input. The input signal of the APA is provided by a low-output-impedance source. A sine wave is normally used as the input signal since it ideally has only the fundamental frequency (no harmonics are present). An analyzer is then connected to the APA output to measure the sine-wave output. The analyzer must measure from 20 Hz to 20 kHz. A regulated dc power supply is used to reduce the noise and distortion injected into the APA.

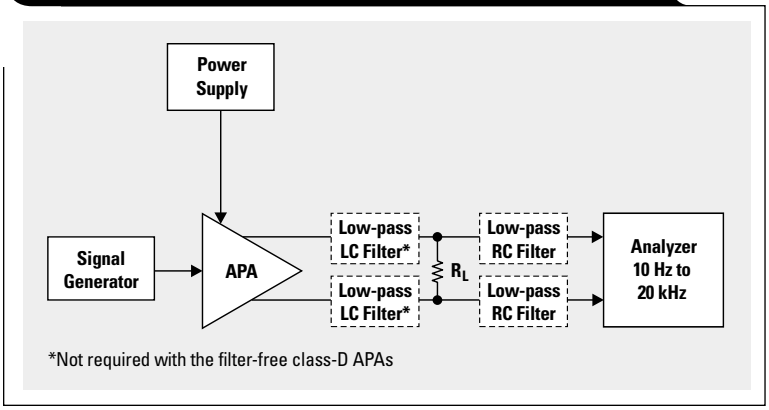
Figure 1. Class-AB basic audio system measurement



A block diagram of a class-D APA measurement system is shown in Figure 2. The system is the same as the class-AB system, except for the addition of the LC and RC low-pass filters. These filters reduce the level of the high-frequency output signal of the pulse-width-modulated class-D APA prior to the analyzer inputs. The rail-to-rail square-wave signal exceeds the common-mode voltage of the analyzer, making accurate distortion measurements impossible without some sort of filter.

The RC filter is required to measure any of the filter-free class-D APAs, which use an improved modulation scheme that greatly reduces the quiescent current and the need for the expensive, bulky LC filters used with the more contemporary class-D devices. These filters are mutually exclusive—when one is present, the other is not required. More information about the selection of the RC filter is provided later in this article. See Reference 1 for more information about the class-D LC filter.

Figure 2. Class-D basic audio system measurement



Interfacing with the APA inputs and outputs

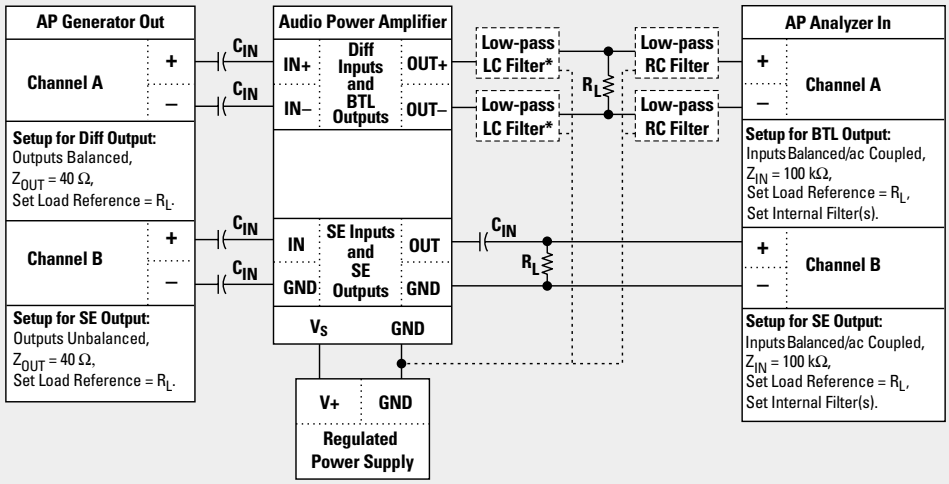
The APA inputs are either differential (Diff) or single-ended (SE), and the outputs are configured for either a bridge-tied load (BTL) (otherwise known as an H-bridge circuit) or a single-ended (SE) load. There are four possible configurations of these inputs and outputs for the APA:

Diff input and BTL output (Diff/BTL)
Diff input and SE output (Diff/SE)
SE input and BTL output (SE/BTL)
SE input and SE output (SE/SE)

Differential inputs have two pins per channel that amplify the difference in voltage between them. They reduce noise and distortion in the APA. BTL outputs have two pins that provide voltages 180° out of phase. The load is connected between these pins. This type of output is normally used when the APA and speaker are in the same enclosure. It has the benefits of quadrupling the output power to the load and eliminating a dc output coupling capacitor.

The SE inputs normally have one pin per channel and are used for line amplifiers (speakers) when a differential signal is unavailable from the source. SE inputs are commonly used with amplifiers that have SE outputs, such as headphone amplifiers. SE outputs have one pin that is tied directly to one end of the load; the other end of the load is tied to ground. This output configuration is normally used when the APA and speaker are in separate enclosures. A dc coupling capacitor is often required with this type of output.

Figure 3. Class-AB or class-D audio system measurement



*Not required when measuring filter-free class-D or class-AB APAs

There are class-AB devices for each configuration. Good examples include the TPA711 with SE inputs and either BTL or SE outputs, and the TPA0212 that can be configured into any of the four combinations. Most class-AB headphone amplifiers have SE outputs and normally have SE inputs. There are a few exceptions, like the TPA6112A2, which are Diff/SE. The class-D devices operate with differential inputs and BTL outputs.

An audio measurement circuit for class-AB or class-D is shown in Figure 3. The RC filters are included for simplicity but are not required for class-AB measurements. The circuit shows an audio precision (AP) measurement system that includes an analog signal generator with sweep capability and an analog analyzer optimized for audio signals. To emphasize the different input/output configurations, channel A (Ch A) is set up for differential inputs and BTL outputs, and channel B (Ch B) is set up for SE inputs and outputs. The remaining combinations (Diff/SE or SE/BTL) can be set up by referencing the appropriate input or output configuration in Figure 3. The BTL and SE settings for the AP generator and analyzer are shown below the appropriate channel. The input ac coupling capacitors, C_{IN}, are included on the device evaluation modules.

Twisted-pair wire should be used on all connections. The twisted pair reduces the loop area between the conductors, protecting against magnetic, or inductive, coupling. Shielding protects against electric, or capacitive, coupling and is used when the system environment is noisy or to reduce radiation from the APA circuit to other nearby circuits.

The signal source should have balanced outputs for APAs with differential inputs. The balanced output really means the outputs have the same impedance. The analyzer should have balanced inputs, particularly when APAs with BTL outputs are measured. The cable shielding (when used) should be terminated at the end where the impedance is high for Diff/BTL-type connections.[2] This will occur at the APA and analyzer inputs. The single point connection prevents return currents from flowing through the shield between connections that are at slightly different voltage potentials, thus minimizing ground loops.

When APAs with SE inputs are measured, the signal source should have unbalanced outputs to prevent any voltage drop from occurring due to ground-current flow. The analyzer should have balanced inputs to reduce the common-mode noise. The signal and ground wires of the twisted pair should be connected at both ends to allow return currents to flow. When the generator is grounded and cable shielding is used, the latter should be connected at both ends to provide an additional return current path, reducing the noise in the twisted-pair wire.[2] See Reference 2 for more details concerning grounding and cable connections.

RC low-pass measurement filter

The RC filter is designed to reduce the square-wave output of the filter-free class-D output so as not to interfere with the measurements. It is required by the analyzer inputs, which do not have the common-mode capability to handle the fast-switching class-D output waveform. The high frequency of the square wave is not a factor in the audio measurements because it is well above the audible frequency range, and the speaker cannot respond at such a fast rate.

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When the RC filter is used, it is connected as shown in Figure 4. C_{Filter} is grounded to the APA to form a path for return current and to minimize ground loops. The input resistance and capacitance of the analyzer are substituted for R_{IN} and C_{IN}. The equivalent circuit is shown in Figure 5. The equation for this circuit is

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left(\frac{R_{IN}}{R_{IN}+R_{Filter}}\right)}{1+j\left(\frac{\omega}{\omega_O}\right)}, \quad \textbf{(1)}$$

where $\omega_O = R_{EQ}C_{EQ}$, $R_{EQ} = R_{Filter} \parallel R_{IN}$, and $C_{EQ} = (C_{Filter} + C_{IN})$. The filter frequency should be set above the bandwidth of the highest measurement frequency, yet low enough to filter out most of the switching frequency so the AP analyzer can measure it.

$$f = 10^{\frac{20\times\log(f_{max})+3\ dB}{20}} \quad \textbf{(2)}$$

Equation 2 provides the cutoff frequency of the RC filter 3 dB above the highest-frequency component, f_{max}, of the spectrum being measured. The value chosen for R_{Filter} must then be large enough to avoid attenuating the output voltage, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by R_{IN} and R_{Filter}. These are conflicting criteria, and a balance must be sought. Once R_{Filter} is selected, C_{Filter} is calculated:

$$C_{Filter} = \frac{1}{2\pi \times f \times R_{Filter}}, \quad \textbf{(3)}$$

where f is the cutoff frequency of the filter. The values used for the measurements in the following discussion were R_{Filter} = 100 Ω and C_{Filter} = 47 nF. Some current will flow through the RC filter to ground, but it is generally not a consideration for these measurements.

THD+N versus power and frequency

The THD+N measurement combines the effects of white noise, distortion, and other undesirable signals into one measurement and relates it (usually as a percentage) directly to the fundamental frequency. Ideally only the fundamental frequency is present at the output, which in practice is never the case. Nonlinearity of the amplifier, internal noise sources, external noise sources, and layout and grounding issues are some of the contributors that distort the original input signal. The distortion shows up at the output as harmonics of the fundamental frequency.

The bandwidth is usually limited with filters in the analyzer to reduce the noise; yet this also reduces the relevant harmonics of the higher-frequency signals, and a tradeoff is made. A filter cutoff frequency of 80 kHz is used for class-AB APAs to allow measurement of the third harmonic. The filter cutoff frequency is set to 22 kHz for class-D APAs to remove the switching waveform from the measurements.

The AP measurement circuit is shown in Figure 6 for a mono-channel, BTL output APA. The measurements for the TPA2001D1 and TPA731 output power sweep are shown in Figure 7, and an output frequency sweep is shown in Figure 8. The maximum input voltage for producing maximum output power can be found by increasing the input until the output clips, then reducing it until it is just below clipping. Another method is to calculate the maximum peak-to-peak input voltage:

$$V_{IN(PP)} = \frac{2\sqrt{2\times P_{O(max)}\times R_L}}{A_V}, \quad \textbf{(4)}$$

where P_O(max) is the maximum-rated RMS output power, R_L is the load resistance, and A_V is the voltage gain of the APA.

Figure 4. RC filter for filter-free class-D

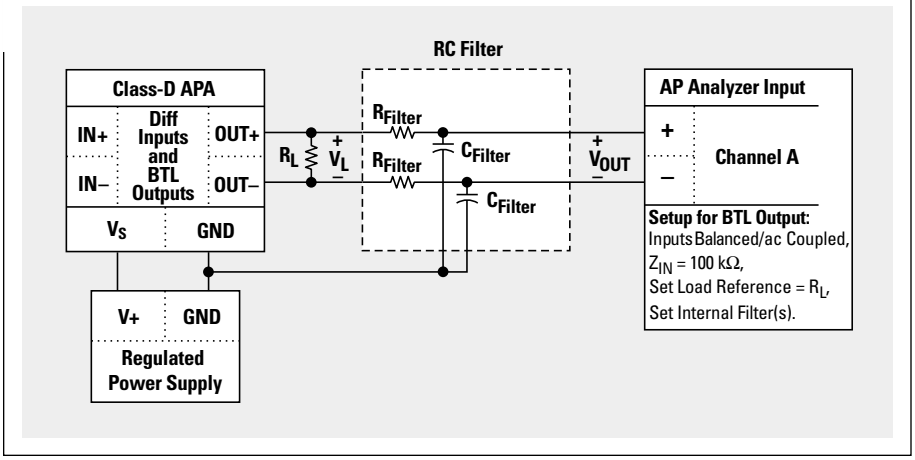


Figure 5. Equivalent filter circuit

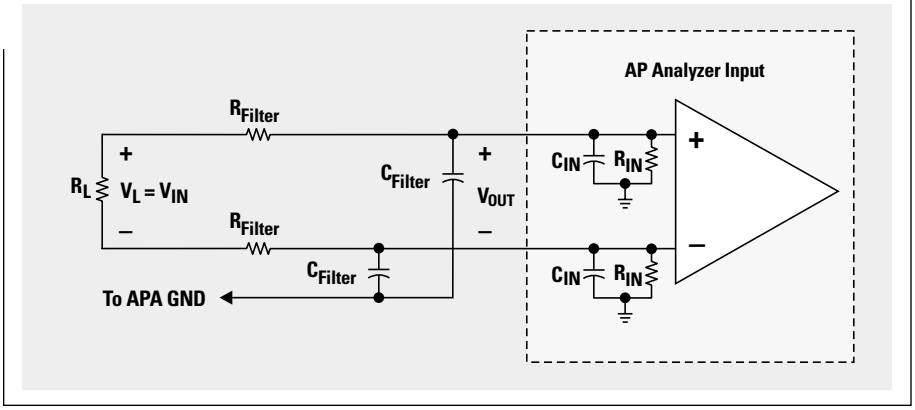
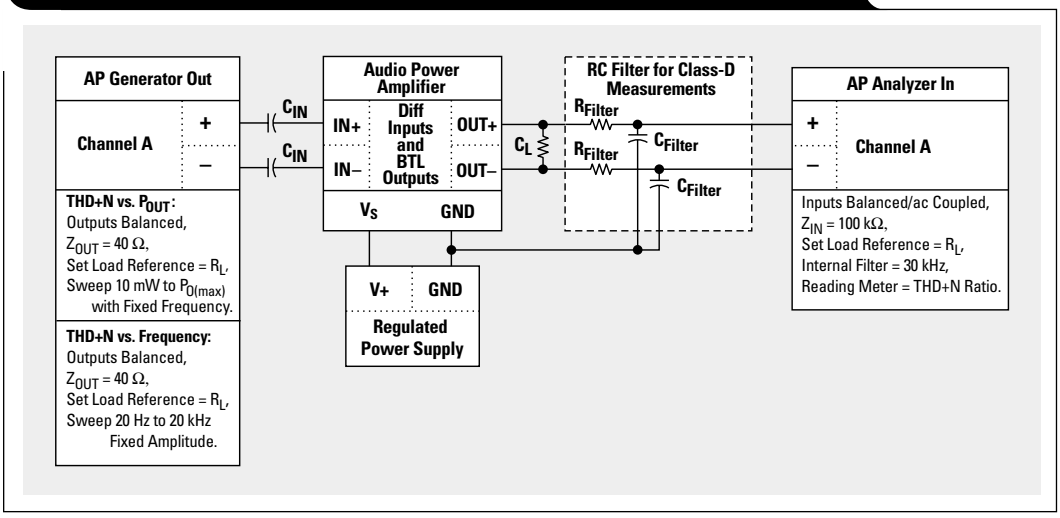


Figure 6. THD+N measurement circuit for a mono-channel BTL APA



When the THD+N versus output power is measured, the analog generator sweeps the input voltage from low to high at a fixed frequency. The output signal harmonics are then measured at specified voltage steps, and the output power is calculated for a given load-impedance value that is provided to the audio analyzer. This value is then divided by the amplitude of the fundamental frequency and graphed as a percentage of the fundamental. Figure 7 shows a typical THD+N-versus-power curve. The higher distortion at low values of P_{OUT} is due to the decrease in signal-to-noise ratio as the harmonics decrease in amplitude below the noise floor.[3] The sudden increase at the upper level of P_{OUT} is due to clipping of the output signal.

When the THD+N versus frequency is measured, the analog generator sweeps the frequency from 20 kHz to 20 Hz at a fixed voltage. The harmonics of the output are measured at specified frequency steps. Each step is divided by the amplitude of the fundamental frequency and graphed as a percentage of the fundamental. This graph provides a fundamental check when compared to the THD+N versus power—they should match at one specific frequency and power. The increase at low frequencies is primarily due to the 1/f noise. If the THD+N measured at low frequencies is considerably higher than the data sheet value, the APA input ac coupling capacitance may need to be reduced to limit the noise bandwidth.

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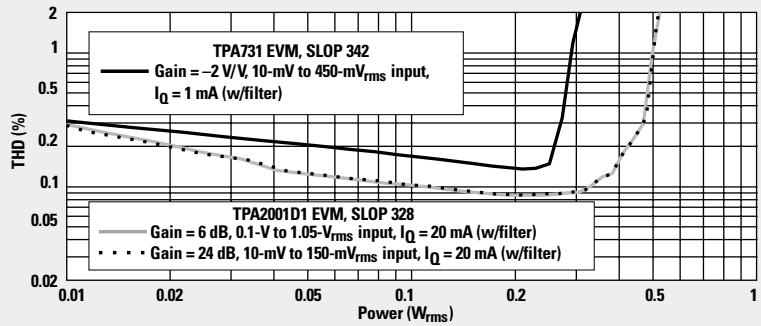
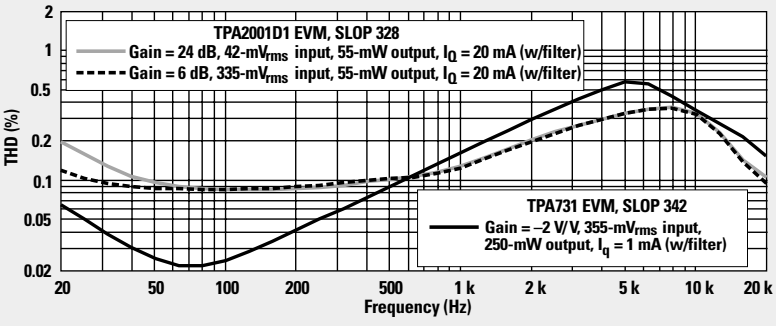
Figure 7. TPA2001D1 and TPA731 output power sweep



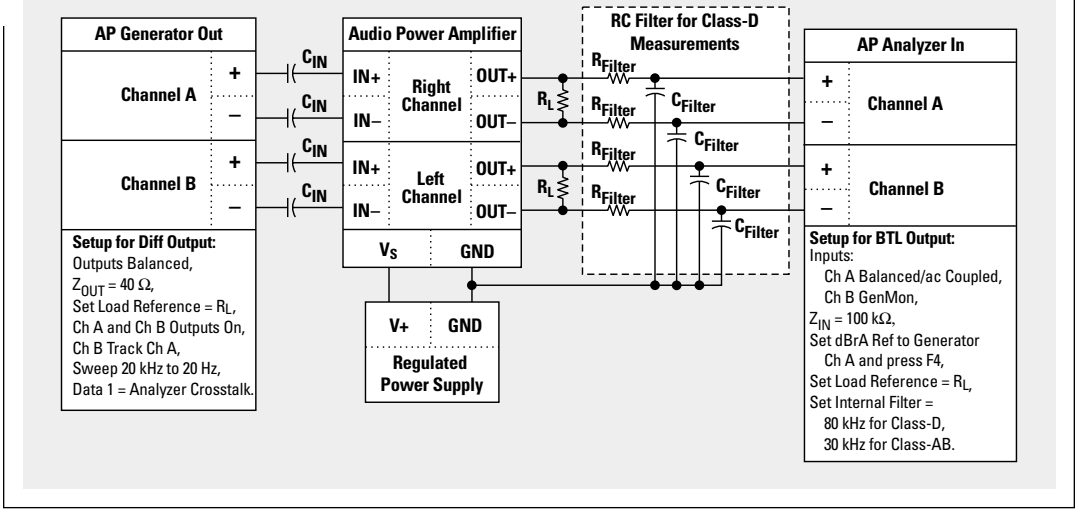
AP Setup: 30-kHz BW, gen out bal-float, analyzer in XLR-bal, PS chassis ground circuit: 8-Ω load, diff input/output, 1-kHz input, 30-kHz filter (R = 100 Ω, C = 47 nF), V_S = 3.3 V, twisted pair wires, mono-BTL

Figure 8. TPA2001D1 and TPA731 output frequency sweep



AP Setup: 30kHz BW, gen out bal-float, analyzer In XLR-bal, circuit: 8-Ω load, diff input/output, 30-kHz filter (R = 100 Ω, C = 47 nF), V_S = 3.3 V, twisted-pair wires all connections, PS chassis ground connected, AP Filter connected to PS ground, mono-BTL

Figure 9. Gain and phase measurement circuit for a mono-channel BTL APA



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The high-frequency increase is due to device nonlinearities. The rolloff at high frequencies is due to the attenuation of harmonics, as the band-limiting filter in the analyzer was set to 30 kHz. This is normally a characteristic of the class-D measurements due to the filters used to reduce the switching frequency. The graph would continue in a straight line if there were no filter present, as is typically the case with class-AB amplifiers. Output filters are not typically used with class-AB measurements.

The load resistance must be set properly to get the right output power, and the shielded cable must be grounded properly or the THD will increase dramatically at high power. If there is unusually high distortion at lower power, check the ground connections and be sure to use twisted-pair, shielded wires. Also check that the generator outputs are set correctly for SE or Diff APA inputs. These measurements will vary with C_{BYPASS} for devices that have a BYPASS pin, with THD increasing as C_{BYPASS} decreases.

Gain and phase

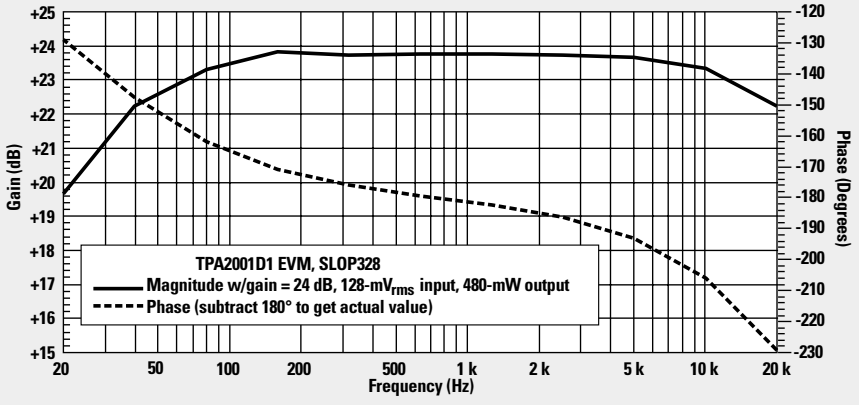
The AP measurement circuit is shown in Figure 9 for a mono-channel BTL APA. Measurements for the TPA731 and TPA2001D1 are shown in Figures 10 and 11. The gain and phase can also be measured at a single point with an oscilloscope by using Equation 5 for the gain and Equation 6 for the phase, where Δt is the interval time between voltages and f is the frequency of the input signal:

$$A_V(dB) = 20 \times \log\left(\frac{V_{OUT}}{V_{IN}}\right) \quad \textbf{(5)}$$

$$\theta = \Delta t \times f \times 360° \quad \textbf{(6)}$$

Both channels must be turned on at the generator panel in the software, and Ch B must be set to track Ch A. The analyzer Ch B is set to GenMon, which means it takes its input directly from the generator output internal to the AP and uses it as the input-phase reference. The reference dBrA value should be set equal to the channel being swept, which in this case is Ch A. It may be necessary to subtract 180° from the measurement to get the actual value. The APA input high-pass filters and the RC filter introduce some attenuation and phase shift at the measurement endpoints, as seen in the figures.

Figure 10. Gain-phase measurement for a TPA2001D1



AP Setup: 30-kHz BW, gen out bal-float, analyzer in XLR-Bal, circuit: 8-Ω load, diff input/output, 30-kHz filter (R = 100 Ω, C = 47 nF), V_S = 3.3 V, Mono-BTL

Crosstalk

Crosstalk is the measurement of the signal coupling between channels of a stereo device. The input to one channel is swept at a constant amplitude, and the outputs of both channels are then measured at specific frequencies using bandpass filters to limit the noise at that particular frequency. The value of the channel being measured is compared to the channel with the signal applied, and the log ratio is graphed versus frequency.

The crosstalk measurement circuit is shown in Figure 12 for an APA with Diff inputs and BTL outputs. This particular setup is referred to as right-to-left (R-L) channel. A graph of the crosstalk is shown in Figure 13 for the TPA2001D2 and the TPA0212.

Figure 11. Gain-phase measurement for a TPA731

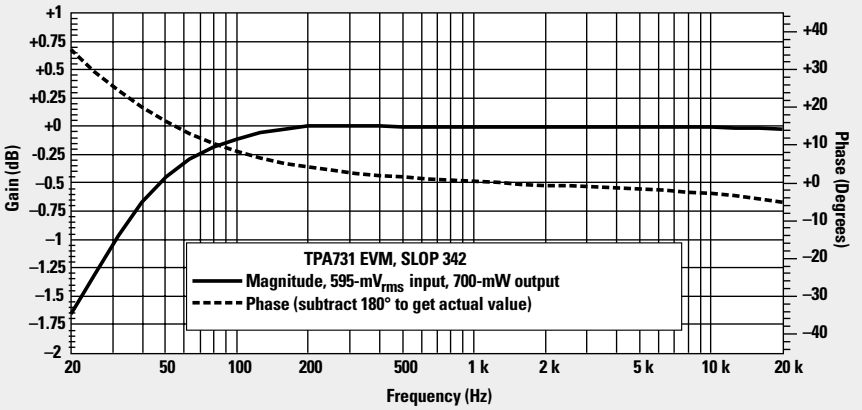
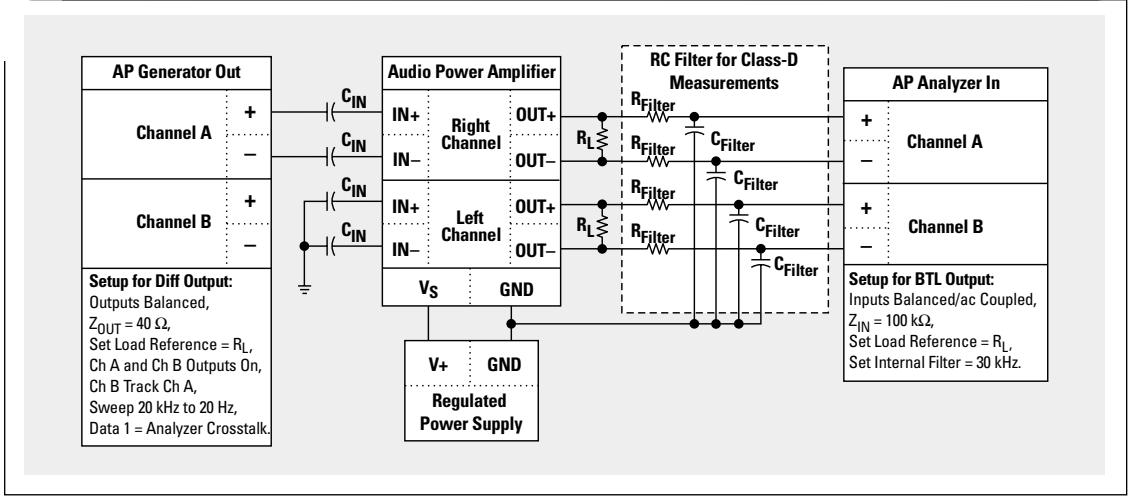


Figure 12. Crosstalk measurement system for an APA with Diff inputs and BTL outputs



It can be measured point-to-point by using Equation 7, which is correct for the graph in Figure 13:

$$\text{Crosstalk} = 20 \times \log\left(\frac{V_{\text{Ch B}}^{\text{OUT}}}{V_{\text{Ch A}}^{\text{OUT}}}\right) \qquad (7)$$

Both channels of the AP must be turned on at the generator panel in the software, and Ch B set to track Ch A. The input is swept over the audio frequency range at a constant amplitude—normally the maximum output power. The internal filter of the analyzer can be set to 30 kHz to limit noise but is otherwise not required. The output cables of the two channels should be

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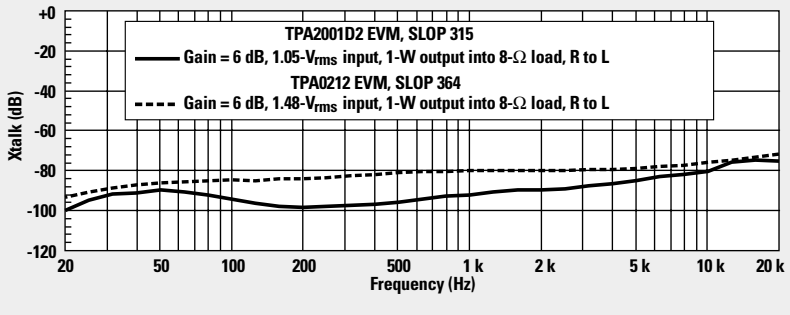
Figure 13. TPA2001D2 and TPA0212 crosstalk



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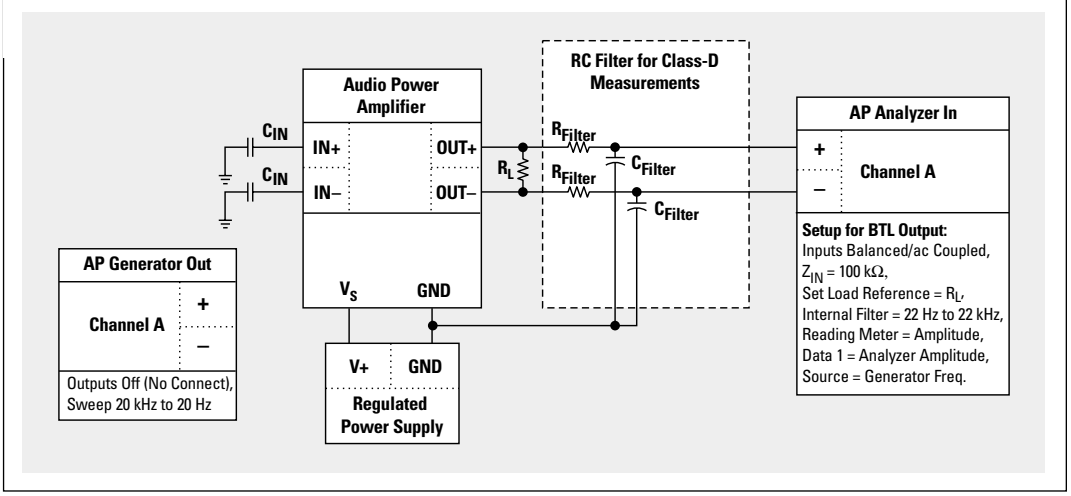
twisted together to minimize the loop between them, and the inputs of the channel being measured should be ac grounded. The setup is reversed to graph the L-R channel crosstalk. Normally the two channels will be different due to impedance variations between the channels.

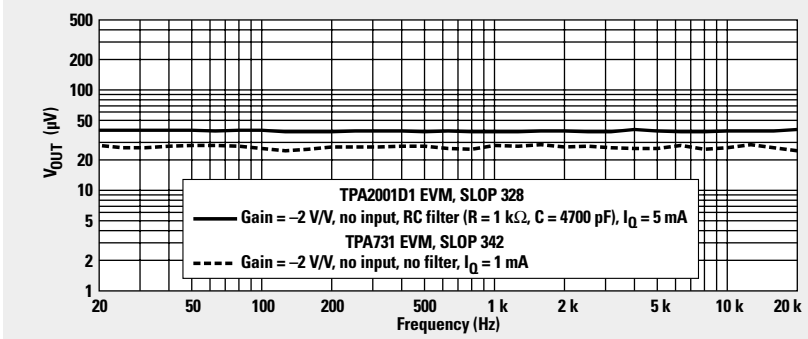
Figure 14. Measurement system for an APA with Diff inputs and BTL outputs



Output noise voltage

The output noise voltage is an integrated value that is measured over the audio frequency spectrum. The measurement circuit is shown in Figure 14 for an APA with Diff inputs and BTL outputs. A graph depicting the Diff/BTL output noise voltage of the TPA2001D1 and the TPA731 is shown in Figure 15. All of the inputs of the APA are ac coupled to ground. The AP generator outputs are not used in this measurement and should be turned off. The analyzer is active, with the reading meter function set to amplitude. The AP bandwidth should be limited to the audio frequency spectrum. The data is set to measure the analyzer amplitude; and the sweep source is the generator frequency, which is swept across the frequency spectrum from 20 kHz to 20 Hz. The output is in V_{rms} and must be divided by the gain to get the input-referred noise voltage.

Figure 15. TPA2001D1 and TPA731 Diff/BTL output noise voltage



AP Setup: 22-Hz to 22-kHz BW, gen out bal-float, analyzer in XLR-Bal, 100-kΩ Z_{IN}, circuit: 8-Ω load, diff input ac-grounded, BTL ouput, V_S = 3.3 V

Conclusion

A method for measuring audio power amplifier characteristics with an audio analyer has been presented. All measurements were taken with off-the-shelf TI APA evaluation modules. These values correspond closely to the data sheet values, which were measured by using characterization boards that are optimized for measuring the device. This shows that reasonable measurements can be made quickly and efficiently with audio circuits by using basic test equipment and pre-fabricated evaluation modules that save time and money spent on layout during initial evaluation of a device.

I want to thank the following people for their assistance: Mike Score, APA Systems Engineer and Member, Group Technical Staff; and Dave Skinner, APA Systems Engineer.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Michael D. Score, "Reducing and Eliminating the Class-D Output Filter," Application Report	sloa023
2. Henry W. Ott, *Noise Reduction Techniques in Electronic Systems* (Wiley Interscience, 1976).	—
3. Bob Metzler, *Audio Measurement Handbook* (Audio Precision, 1993).	—

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