ADS82x ADC with non-uniform sampling clock

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Introduction

The Texas Instruments (TI) high-speed analog-to-digital converter (ADC) ADS82x family includes ADS825/822, ADS826/823, and ADS828. These ADCs have 10-bit resolution with a maximum sampling speed of 40, 60, and 75 MHz, respectively. They are widely used in communications, video digitizing, test equipment, CCD imaging, and medical ultrasound imaging. In some applications the ADCs are driven by a continuous sampling clock with constant frequency. However, in other applications such as medical ultrasound imaging or where the ADCs are parallel with interleaved configuration, they must operate with a sampling clock that has variable frequency, phase, or duty cycle. In other words, these ADCs must operate with a non-uniform sampling clock. Can TI's ADS82x handle this? A lab bench test has shown good results, and the answer is *yes*. This article presents the measurement system and fast Fourier transform (FFT) analysis method used along with the test results for only the ADS826 EVM. However, these test results are applicable to all other ADCs in the ADS82x family, since these ADCs all have pipeline architecture and are designed with the same basic features, such as 10-bit resolution, internal or external reference, single-ended or differential analog input, input range selection, single 5-V power supply, power-down mode, low power dissipation, three-state output, and CMOS- or TTL-output compatibility.

Figure 1. ADS82x bench test system

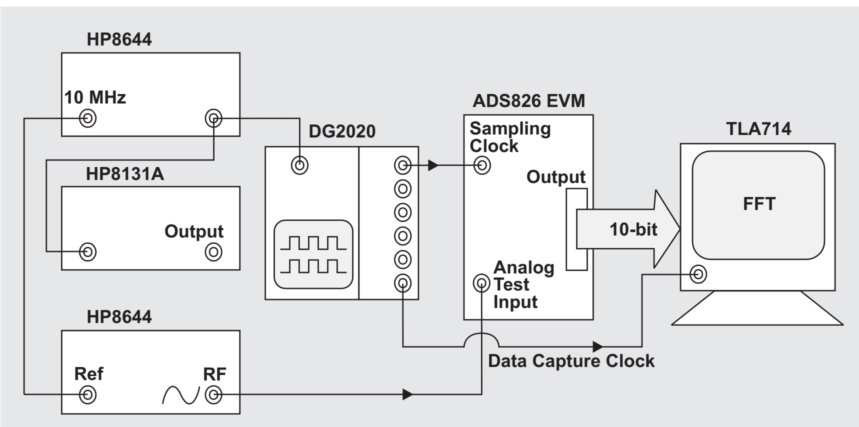
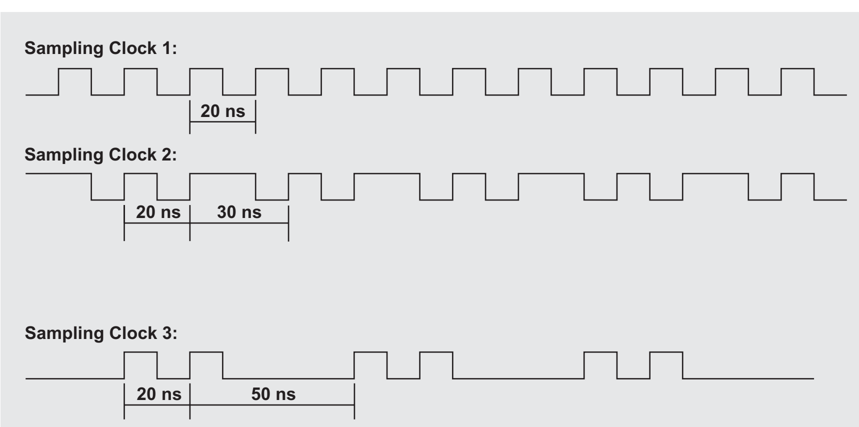


Figure 2. Pattern clocks for ADS826 test



Test system

The ADS826 bench test system includes a pulse generator (HP8131A), data generator (DG2020), waveform generator (HP8644), and Tektronix logic analyzer (TLA714) (see Figure 1). This system is used to generate an analog signal, pattern clock, and data capture clock. The analog signal, a sine wave that can be varied in frequency and amplitude, is an input test signal to the ADS826; and the pattern clock, which can be varied in frequency, phase, or duty cycle, is the sampling clock to the ADS826. The data capture clock can be flexible with a proper frequency and duty cycle for the TLA714 to capture data from the ADS826 EVM and perform FFT analysis. The clock source is phase locked with the test signal source by the 10-MHz reference output of the HP8644, so all the signals generated from the system are synchronized. The HP8131A is used to calibrate DG2020.

Pattern clocks

Three different pattern clocks, plotted in Figure 2, are generated from this system. They are used to test the non-uniform sampling performance of the ADS826. Sampling Clock 1 (Case 1) is a uniform clock with a frequency of 50 MHz and a duty cycle of 50%. Sampling Clock 2 (Case 2) is a non-uniform clock with frequency (varied cycle by cycle) alternating from 50 MHz with a 50% duty cycle to 33.3 MHz with a 66.7% duty cycle. Sampling Clock 3 (Case 3) is a non-uniform clock with frequency varying (cycle by cycle) from 50 MHz with a 50% duty cycle to 20 MHz with a 20% duty cycle. These clocks are simulated from real applications.

ADS826 input/output configuration

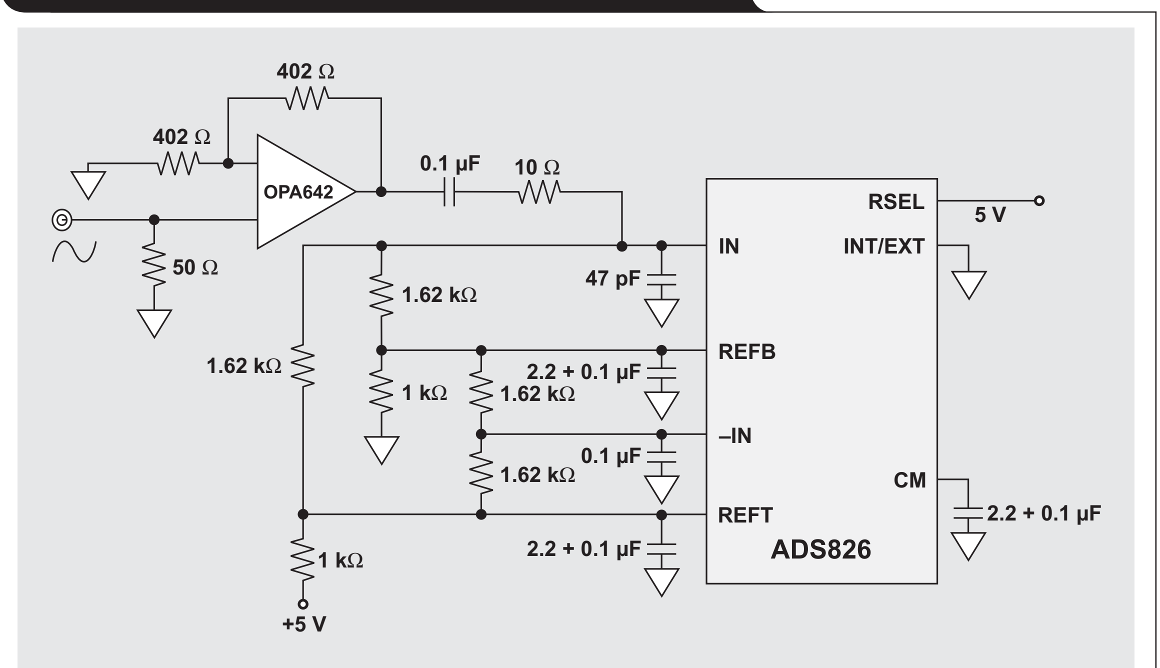
The single-ended analog input circuit used in this test is shown in Figure 3. Here an OPA642 with an inverting gain of 2 is used. This circuit mainly provides two conditions for the ADS826. One is an ac-coupled signal path with a power amplifier with proper gain and driving capability; another is the common-mode dc voltage for the ADS826 analog input bias. The ADS826 is configured with an internal reference and a full-scale input range of 2 V_{p-p}. The common-mode pin (CM) is not used here except for bypassing. Based on the configuration, a 2-V_{p-p} analog sine wave is applied to +IN, and a 2.35-V common-mode dc voltage is added to both +IN and –IN of the ADS826 analog input. This common-mode voltage is generated by REFT, REFB, and an external 5-V power supply through a balanced resistor network. The input clock of ADS826 from DG2020 is one of the three sampling clocks mentioned earlier. The digital output of the ADS826 is connected to the TLA714 through a data bus driver such as TI's SN74x family. The digital configuration of ADS826 is straightforward and is therefore not shown in Figure 3. Details about the ADS826 digital output circuit can be found in Reference 1.

Data measurement and analysis

A TLA714 is used to collect the output data from the ADS826, and the performance of the device is evaluated using FFT analysis. For this approach, the sampling clock of the ADS826 and the input clock of the TLA714 need to be synchronized with the analog input test signal. When the signal is synchronized, the data is ready to be measured. In the beginning, the analog sine wave is sampled by the ADS826 at the rising edge of the sampling clock, and the sample is converted into digital form in the pipeline stage. Five sampling clocks later, a digital number (straight offset binary code) of the sample is output to the data bus of the ADS826 with additional small-signal propagation. The digital data is sent to the data bus by the ADS826 at the rising edge of the input sampling clock. It stays on the bus for one clock period and is then updated at the next rising edge of the input sampling clock by new sample data. When the data is valid on the data bus, it is captured by the logic analyzer with a synchronized clock. The data is then processed and analyzed using FFT analysis.

The three different sampling cases mentioned earlier are evaluated here. In Case 1 the sampling clock frequency of ADS826 is constant at 50 MHz; in Case 2 the sampling clock frequency of ADS826 is not constant and is regularly varied 20 ns or 30 ns on a cycle-by-cycle basis; and in Case 3 the sampling clock period of the ADS826 is regularly varied by 20 ns or 50 ns. Sampling Clocks 2 and 3 are non-uniform sampling clocks, and their phases change with time. This is clearly demonstrated by Sampling Clock 3, where the clock phase is delayed for 30 ns after each two 50-MHz clock cycles. Such sampling phase variation is apparent

Figure 3. Single-ended input circuit for ADS826 bench test



from the output data of the ADS826. In Case 1, the ADS826 samples the analog sine wave and constantly outputs the digitized samples at 50 MSPS. In Cases 2 and 3, the analog sine wave is sampled by the ADS826 at variable speed so that the digitized samples are sent out in non-uniform time intervals. This is shown in Figures 4–6. Further analysis of the non-uniform sampling performance of the ADS826 is presented later under "Test results."

Does the ADS826 operate as well with a non-uniform sampling clock as it

Figure 4. Non-uniform sampling time intervals

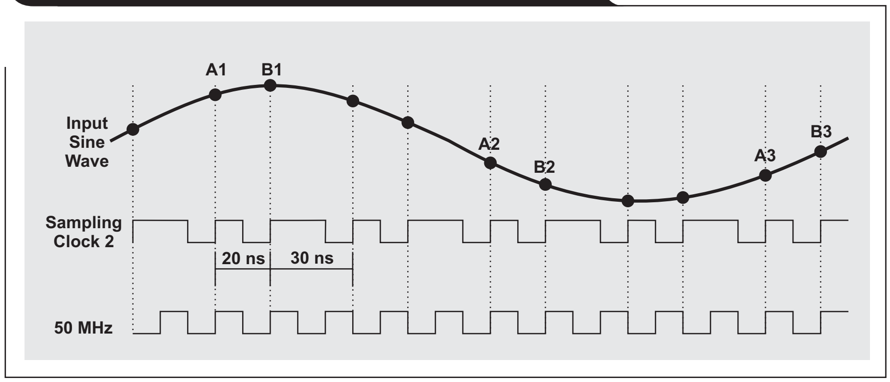


Figure 5. ADS826 non-uniform sampling performance analysis for Case 2

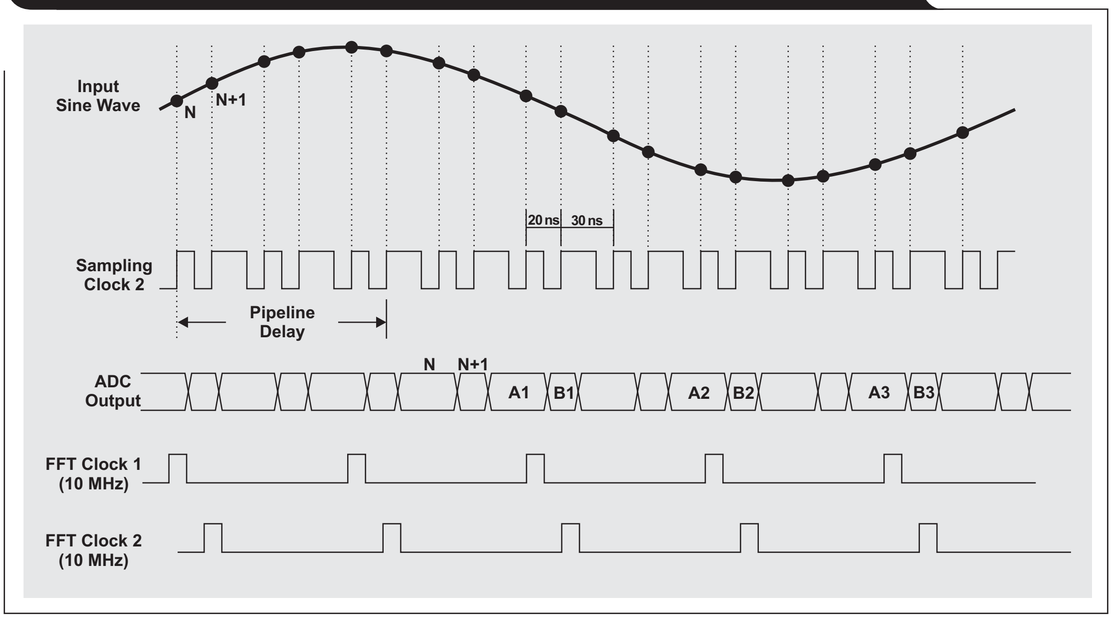
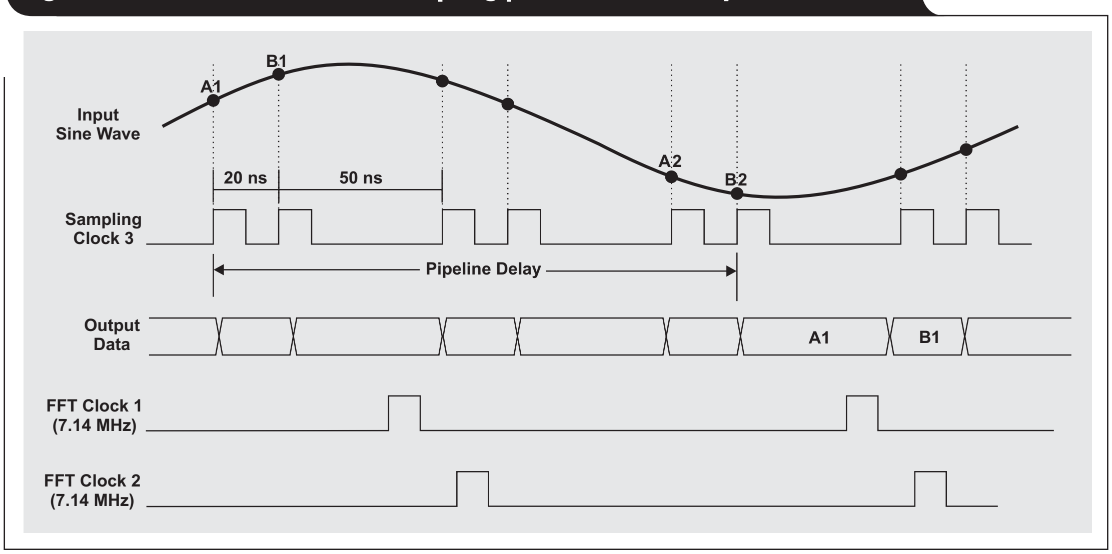


Figure 6. ADS826 non-uniform sampling performance analysis for Case 3

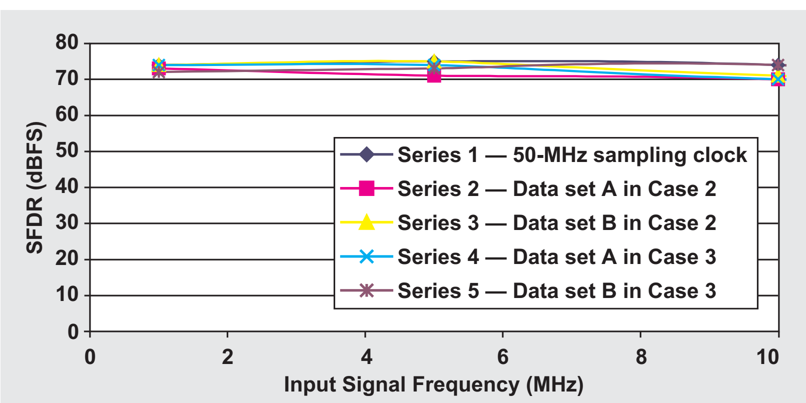


does with a uniform sampling clock? Yes, and this can be explained by the downsampling technique and the FFT analysis. In FFT analysis, the sample size is kept at 4096; and the FFT sampling frequency is kept more than five times higher than the signal frequency for all three cases. In Case 1 with Sampling Clock 1, the output data of the ADS826 can be used directly as the FFT input because of the uniform samples; and the FFT result is the specification in the data sheet. In Cases 2 and 3 with a non-uniform sampling clock, the output data of the ADS826 cannot be used directly as the FFT input due to non-uniform samples. To perform the FFT analysis for Cases 2 and 3, we need to find a set of uniform samples from non-uniform ADC sampling data. The implementation of this idea is shown in Figure 4, where the ADS826 samples an analog sine wave at the rising edge of Sampling Clock 2 and the sample locations on the sine wave have non-uniform time intervals. With FFT downsampling techniques, however, these locations can be classified into uniform time-interval sets. For example, by using a 50-MHz clock as a uniform time reference, we can find data set A (A1, A2, A3...) and data set B (B1, B2, B3...) in which the data is uniformly spaced. Furthermore, data set A results from fast-sampling Clock 2 (50 MHz), and data set B results from slow-sampling Clock 2 (33.3 MHz). The data in each set is uniformly time-spaced by the 10-MSPS FFT sampling frequency, which downsamples the original data. This frequency can be used as a clock frequency of the logic analyzer that is used to extract data set A or B from the data bus of the ADS826.

The completed data acquisition from the ADS826 with a non-uniform sampling clock is shown in Figure 5, where sample N on the sine wave is collected by the ADS826 at the rising edge of the input clock and is output after a period of five input clocks. The input clock consists of fast and slow clocks, while the ADS826 output data consists of long and short periods. Because of the five-clock delay, sample N from the fast input clock appears on the output data bus for a long period, and sample N+1 from the slow input clock appears on the output data bus for a short period. For FFT analysis, FFT Clock 1 (10 MHz) is used to capture data set A, while FFT Clock 2 (10 MHz with a 20-ns clock delay) is used to capture data set B. The output results of data sets A and B represent the dynamic performance of the ADS826 with non-uniform Sampling Clock 2, as shown later under "Test results."

The same principle is applied in Case 3, which is shown in Figure 6. In this case the frequency of FFT Clocks 1 and 2 is 7.14 MHz. With a different sampling clock pattern, the downsampling clock frequency for FFT will vary and may be difficult to determine. The test results show that the ADS826 functions well with a non-uniform sampling clock as long as the clock high and low pulse width is at least half the period of the highest sampling clock specified in the data sheet; for example, a pulse width of at least 8.3 ns for the ADS826 (maximum speed is 60 MHz). The sampling clock speed also has to meet the minimum limit in the data sheet.

Figure 7. SFDR of ADS826 with uniform and non-uniform sampling clocks



Test results

Input analog signal frequencies of up to 30 MHz for all three cases were tested, and the results are shown in Table 1 and Figure 7. Table 1 shows that there is no change in the signal-to-noise ratio (SNR) whether the ADS826 is driven by a uniform or non-uniform sampling clock. Figure 7 shows that there is also no significant difference in spurious-free dynamic range (SFDR) performance between uniform and non-uniform sampling. In addition, for

Table 1. SNR (dBFS) of ADS826

	SAMPLING CLOCK (MHz)	FFT CLOCK (MHz)	SNR (dBFS)			
			1-MHz Signal Frequency	5-MHz Signal Frequency	10-MHz Signal Frequency	30-MHz Signal Frequency
Case 1	50 (uniform)	50	60	60	60	58
Case 2	50 and 33.3 mixed (non-uniform)	10 (FFT Clock 1)	60	60	60	58
	50 and 33.3 mixed (non-uniform)	10 (FFT Clock 2)	60	60	60	58
Case 3	50 and 20 mixed (non-uniform)	7.14 (FFT Clock 1)	60	60	60	58
	50 and 20 mixed (non-uniform)	7.14 (FFT Clock 2)	60	60	60	58

non-uniform sampling, the SFDR increases when the sampling clock or input signal amplitude decreases.

The FFT test result is shown in Figures 8–10. Figure 8 shows the FFT output of Case 1 and the performance of ADS826 with a 50-MHz sampling clock and a 1-MHz input sine wave at maximum amplitude. The SNR is 60 dBFS, and the SFDR is 74 dBFS. The FFT output of Case 2 is shown in Figure 9, in which the non-uniform ADC samples are downsampled by a 10-MHz FFT clock. Figure 9a shows the FFT output of data set A, and Figure 9b shows the FFT output of data set B. The SNR is 60 dBFS for both data sets A and B; the SFDR is 73 dBFS for data set A and 74 dBFS for data set B. The FFT output of Case 3 is shown in Figure 10, in which the non-uniform ADC samples are downsampled by a 7.143-MHz FFT clock. The SNR is 60 dBFS for both data sets A and B; the SFDR is 74 dBFS for data set A and 72 dBFS for data set B.

Conclusion

The test results presented in this article strongly support non-uniform sampling applications of the ADS82x family. The test results show that the same SNR is achieved with both uniform and non-uniform sampling using the ADS826. Good SFDR is also achieved with both uniform and non-uniform sampling. The test data and analysis conclude that the ADS826 functions well with a non-uniform sampling clock as long as the clock high and low pulse width is at least half the period of the highest sampling clock specified in the data sheet. The test result proves that the ADS82x family has a very stable and solid SNR of 10 bits of resolution in both uniform and non-uniform high-speed sampling and converting operations, making it appropriate for wide use in future applications.

Figure 8. FFT output with 50-MHz uniform sampling (Case 1)

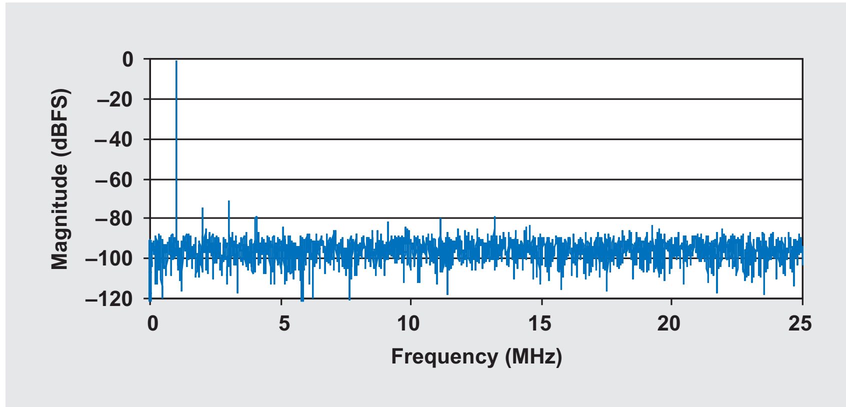


Figure 9. Case 2 FFT outputs with 10-MHz downsampling frequency

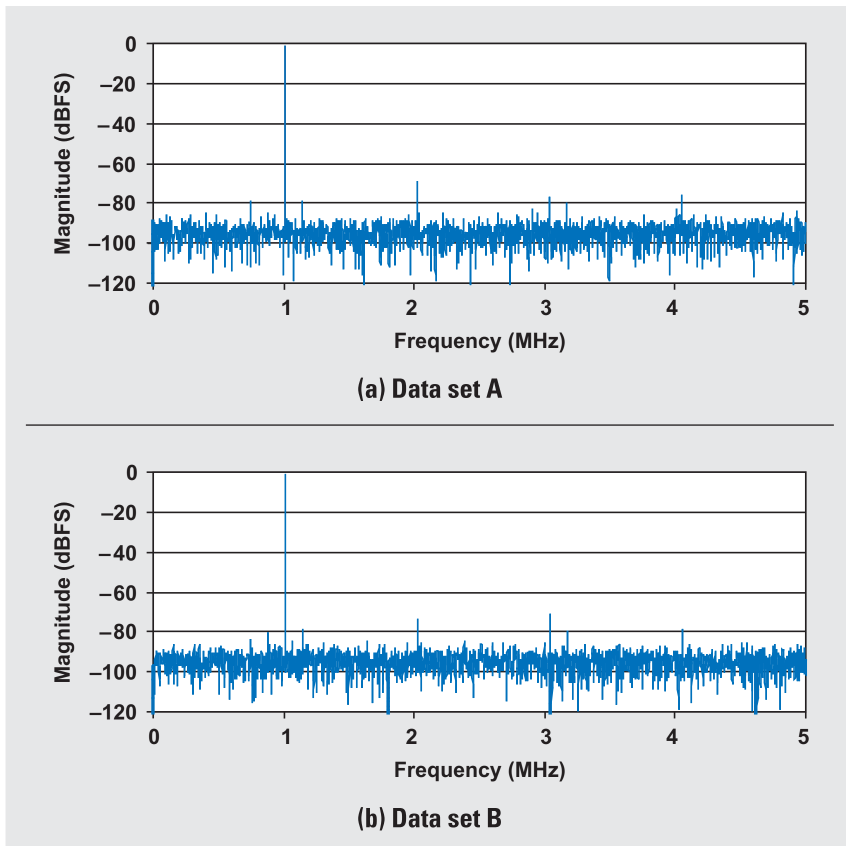
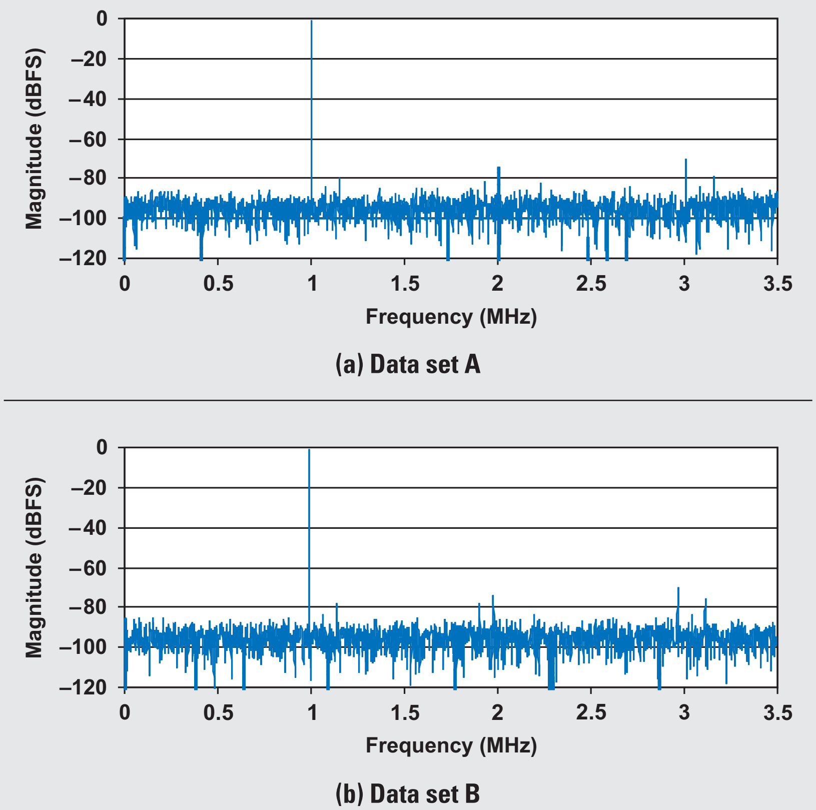


Figure 10. Case 3 FFT outputs with 7.14-MHz downsampling frequency



References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. "DEM-ADS82xE Evaluation Fixture," User Guide	sbau036
2. "10-Bit, 60MHz Sampling Analog-to-Digital Converter," Data Sheet	sbas070
3. Alan V. Oppenheim and Ronald W. Schafer, *Discrete-Time Signal Processing* (Prentice-Hall, Inc., 1989).	—

Acknowledgments

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Related Web sites

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