

# Power conservation options with dynamic voltage scaling in portable DSP designs

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*Low Power DC/DC Applications, High Performance Analog*

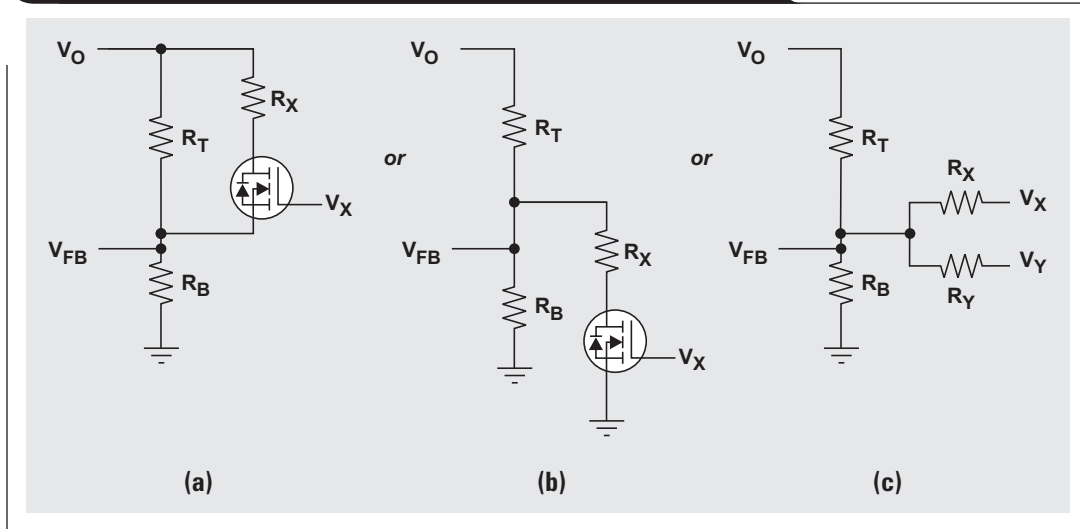
Extending the useful life of the battery in portable electronics with a DSP core is a challenge for portable electronics manufacturers. The relationship  $P_C \sim (V_C)^2 f$  describes the power consumption of a DSP core, where  $P_C$  is the core power consumption,  $V_C$  is the core voltage, and  $f$  is the core clock frequency.

Thus, power consumption can be reduced by lowering the internal clock frequency and/or even more by lowering the core supply voltage. Dynamic voltage scaling (DVS) is

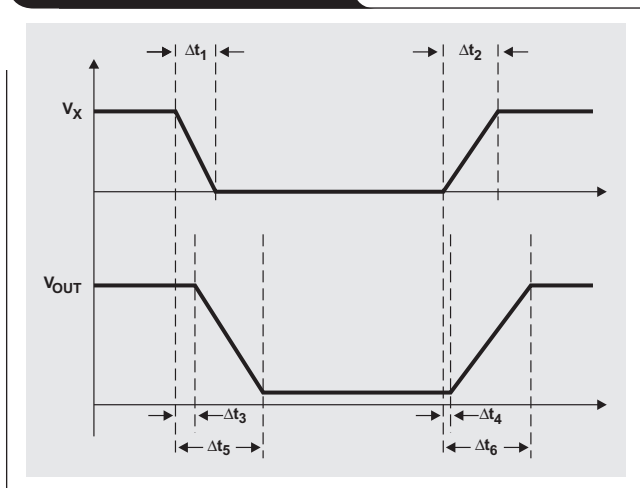
the term used to describe methods of adjusting core supply voltage to minimize power consumption. This article explains two generic methods of implementing DVS and highlights the advantages and disadvantages of each method.

Both methods require the use of a power IC with an adjustable output voltage and an externally applied control signal ( $V_X$ ). As shown in Figures 1a and 1b, the first method uses FET switches and resistors in parallel with either the top or bottom feedback resistors to alter the feedback

**Figure 1. Methods of implementing dynamic voltage scaling**



**Figure 2. Timing diagram**



network. The second method, in Figure 1c, uses the control signal or signals and an additional resistor to alter the feedback network.

Figure 2 shows the timing of the control signals and of the output voltage. Table 1 explains the different delays and their respective causes.

**Table 1. Timing delays and their causes**

	DESCRIPTION	INFLUENCING FACTORS
$\Delta t_1$	Fall time of $V_X$	Source of control signal
$\Delta t_2$	Rise time of $V_X$	
$\Delta t_3$	Response delay	Rise/fall time of $V_X$ , IC response time, feedback network settling time
$\Delta t_4$	Response delay	
$\Delta t_5$	$V_{OUT}$ fall time	Load current, output capacitance, IC response time
$\Delta t_6$	$V_{OUT}$ rise time	

Each method in Figure 1 will be examined in detail. Although most adjustable power ICs can be used to implement DVS, the author chose the TPS62200 300-mA, synchronous buck converter because it maintains high efficiency over a wide load range by switching from PFM at light loads to PWM at heavy loads.

### Switched bottom-side feedback resistor

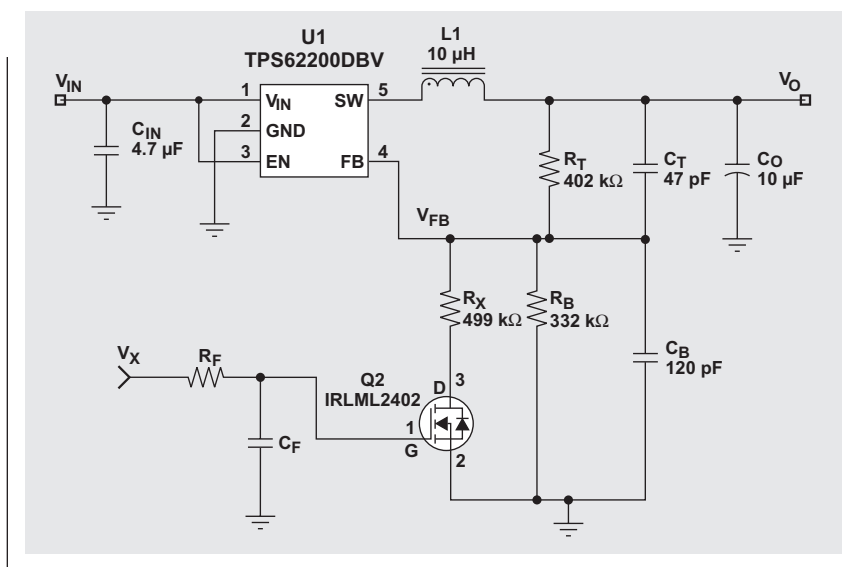
The polarity of the control signal determines the placement of the FET switch. If a low signal triggers the step-down of the core voltage, then an NMOS FET switch and additional resistor can be placed in parallel with the bottom feedback resistor. An example application is shown in Figure 3.

Figure 4 shows an example of DVS using the circuit of Figure 3, where the input capacitance of Q2 is 110 pF. The input voltage is 3.3 V, and the output voltage switches between 1.5 V and 1.1 V with a 10-Ω load. The rise and fall times of  $V_X$  are 10 μs.

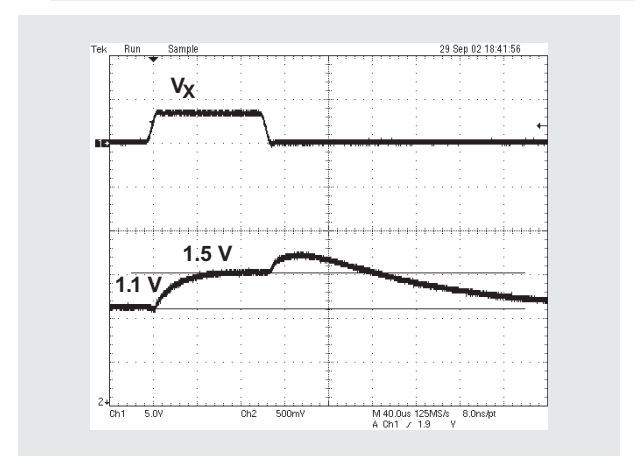
The overshoot during the transition from high to low voltage is due to the negative edge of the control signal being injected into the feedback pin, FB, by the gate-drain capacitance of the FET. Pulling FB low causes  $V_O$  to go high. Using lower-valued feedback resistors and higher-valued capacitive divider capacitors reduces the overshoot. Also, using a FET with lower input capacitance reduces the overshoot. Figure 5 shows an example of DVS using the circuit of Figure 3, where  $R_T = 200$  kΩ,  $R_B = 165$  kΩ,  $C_T = 100$  pF,  $C_B = 220$  pF, and Q1 is a BSS123 with input capacitance of 30 pF.

If the control signal's ramp rate ( $\Delta t_1$  and  $\Delta t_2$  of Figure 1) can be slowed either at the source or by an RC filter, like the one created by  $R_F$  and  $C_F$  in Figure 3, the overshoot can be further minimized. Slowing the fall time of  $V_X$  to 150 μs removes the overshoot entirely, as shown in Figure 6.

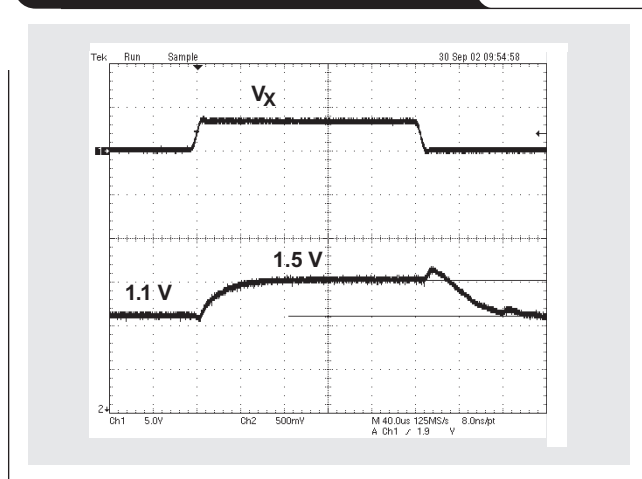
**Figure 3. Schematic with bottom resistor and high-cap FET**



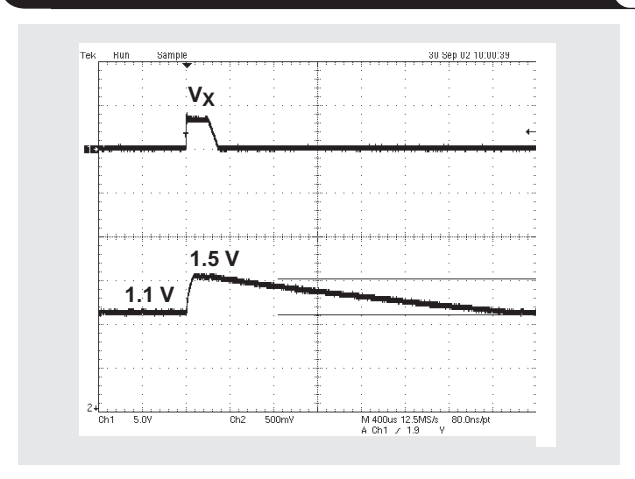
**Figure 4. Bottom FET solution with overshoot**



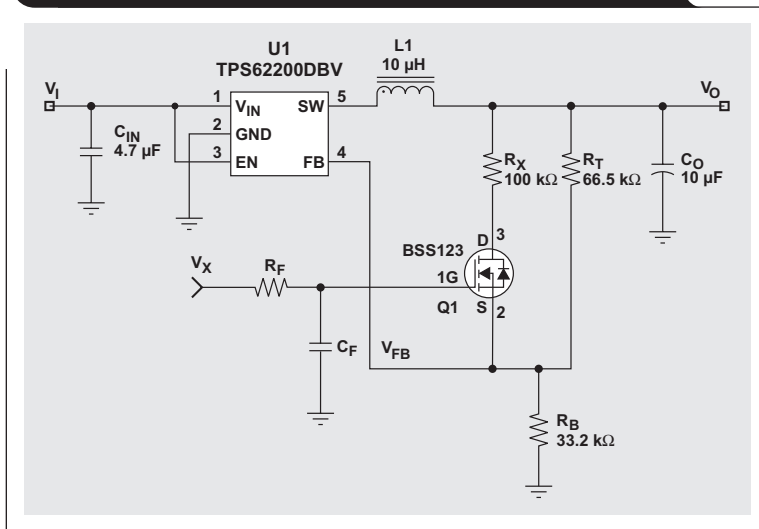
**Figure 5. Bottom FET solution with reduced overshoot**



**Figure 6. Bottom FET solution with no overshoot**



**Figure 7. Schematic with top-side, low-cap FET and low-value feedback resistors**



**Switched top-side feedback resistor**

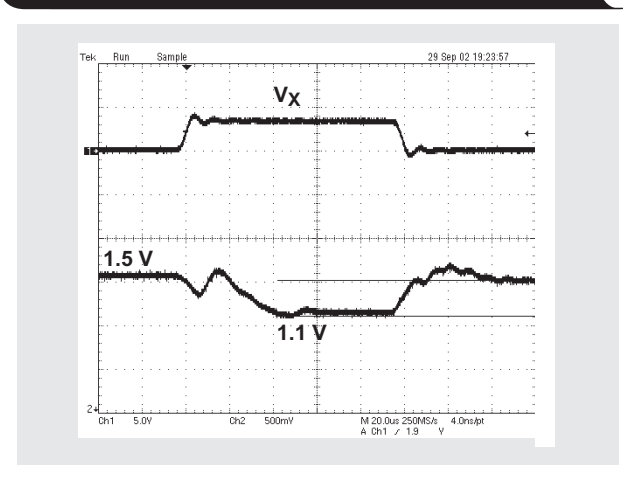
If a high control signal triggers a step-down of the output voltage, then the NMOS FET must be placed in series with the high-side feedback resistor, as shown in Figure 7. The FET must be carefully selected to ensure that (1)  $V_X$  is higher than  $V_{FB}$  by at least the FET's threshold voltage and (2) the input capacitance is low to minimize injection of  $V_X$  onto  $V_{FB}$ . Unlike the low-side FET switch in Figure 2, the high-side FET's source pin connects directly to the converter's feedback pin. Since the FET's gate-source capacitance shorts  $V_X$  to  $V_{FB}$  during its transition, the output is susceptible to overshoot and undershoot; however, lower feedback resistors reduce both.

Figure 8 shows an example of DVS using the circuit of Figure 7, with  $V_{IN} = 3.3$  V, a 10-Ω load, and control signal rise and fall times of 5 μs.

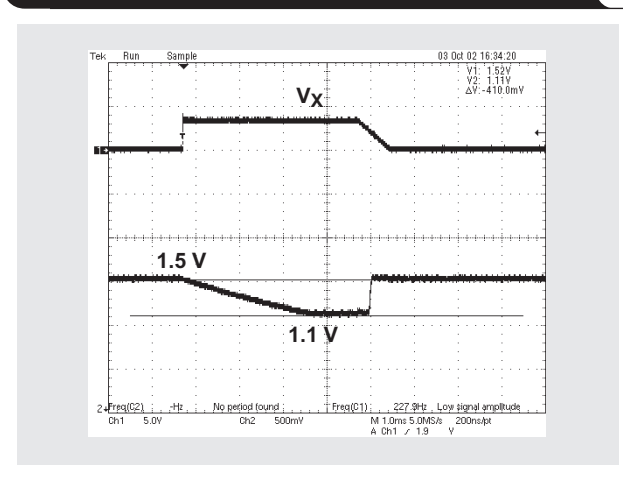
At output currents below 60 mA, the TPS62200 switches from PWM mode to PFM mode, and the observed undershoot and overshoot change. If  $V_X$ 's ramp rate ( $\Delta t_1$  and  $\Delta t_2$  of Figure 1) can be slowed either from the source or by an RC filter, like the one created by  $R_F$  and  $C_F$  in Figure 7, the overshoot is further minimized. Figure 9 shows results from using the same circuit as in Figure 7 but with a 1-kΩ load and control signal rise and fall times of 3 μs and 500 μs, respectively.

Although exact values for the feedback components and rise and fall times of the control signal are dependent on the specific application, the following generalizations can be made. Lower-valued feedback components reduce noise susceptibility at the feedback node and therefore reduce potential overshoot and undershoot caused by the switching transistor. However, these lower-valued feedback components consume power and reduce efficiency at light load. The rise and fall times of the control signal affect overshoot and undershoot. The optimal rise and fall times should be determined experimentally for the specific application, especially for the load current and dc/dc converter operating mode.

**Figure 8. Top-side FET solution with overshoot**



**Figure 9. Top-side FET solution at low current and reduced overshoot**



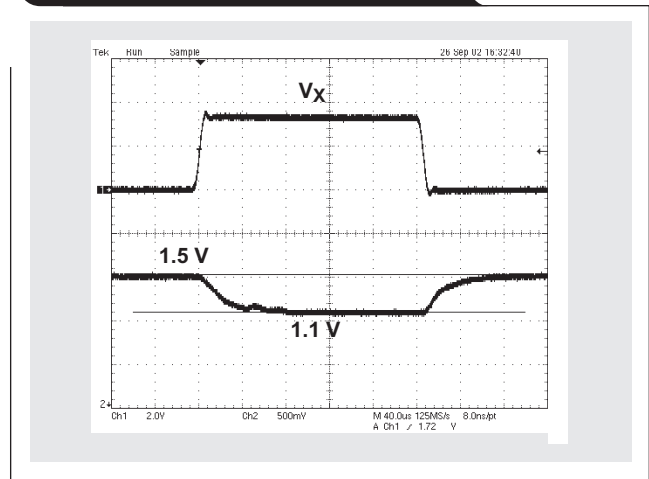
## Two voltages with one additional resistor

A simpler alternative for generating multiple voltages is to use  $V_X$  to inject current into the feedback network through an additional resistor, thereby changing the output voltage. Figure 10 shows the circuit in Figure 11 transitioning between  $V_{O1} = 1.5\text{ V}$  and  $V_{O2} = 1.1\text{ V}$ , with only one additional resistor,  $R_X$ .

For the following discussion, refer to Equations 1–4 at the bottom of this page. Equations 1 and 2 were written by summing the currents at the feedback node,  $V_{FB}$ . Simultaneously solving Equations 1 and 2, then substituting back and solving for  $R_B$ , yields Equations 3 and 4. These equations show how to compute the values of the injection resistor,  $R_X$ , and bottom feedback resistor,  $R_B$ , in Figure 11, given  $R_T = 402\text{ k}\Omega$ ,  $V_{O1} = 1.5\text{ V}$ ,  $V_{O2} = 1.1\text{ V}$ ,  $V_{X\_HI} = 3.3\text{ V}$ ,  $V_{X\_LO} = 0\text{ V}$ , and  $V_{FB} = 0.5\text{ V}$ .

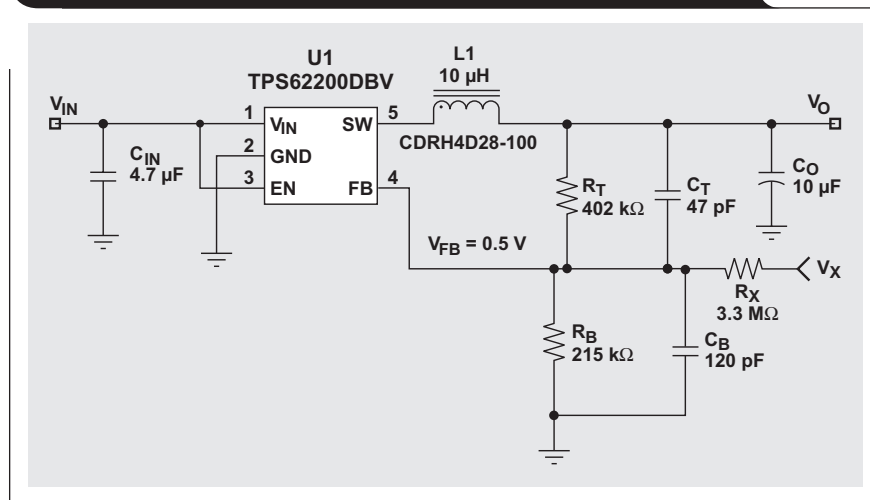
Pulsing  $V_X$  with varying duty cycles varies its average dc level. This allows a single control voltage and one additional resistor,  $R_X$ , to generate multiple output voltages. Equations 1 and 2 can be solved to find  $R_X$  and  $R_B$  for the lowest desired output voltage and highest  $V_X$ . Then, solving Equation 4 for  $V_O$  and substituting in progressively lower values for  $V_{X\_HI}$  results in progressively higher values of  $V_O$ . Figure 12 on the next page shows such an implementation.

**Figure 10. Transition between two output voltages**



Choosing  $R_F$  in Figure 12 two orders of magnitude below  $R_X$  eliminates the need to include it in the computation of  $R_X$ . Choosing  $C_F$  to form a low-pass filter with  $-3\text{-dB}$  roll-off at least two orders of magnitude below the frequency of  $V_X$  makes the ripple being injected into  $V_{FB}$  negligible.

**Figure 11. Schematic for switching between two voltages**



$$\frac{V_{FB}}{R_B} + \frac{V_{FB} - V_{O1}}{R_T} + \frac{V_{FB} - V_{X\_LO}}{R_X} = 0 \quad (1)$$

$$\frac{V_{FB}}{R_B} + \frac{V_{FB} - V_{O2}}{R_T} + \frac{V_{FB} - V_{X\_HI}}{R_X} = 0 \quad (2)$$

$$R_B = -V_{FB} R_T \times \frac{-V_{X\_HI} + V_{X\_LO}}{(-V_{O1} + V_{O2} + V_{X\_LO} - V_{X\_HI}) \times V_{FB} - V_{X\_LO} V_{O2} + V_{X\_HI} V_{O1}} \quad (3)$$

$$R_X = R_B \times R_T \times \frac{-V_{FB} + V_{X\_HI}}{V_{FB} R_B + V_{FB} R_T - V_{O2} R_B} \quad (4)$$

### Three voltages from two additional resistors

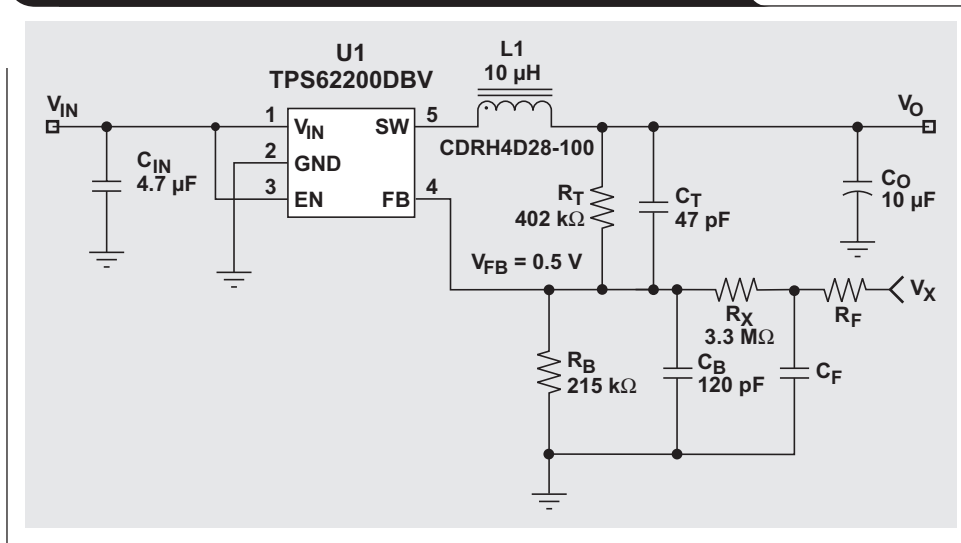
If varying the duty cycle of  $V_X$  is not an option but additional control voltages (e.g.,  $V_Y$ ) are available, the converter can still be configured to switch between multiple voltages. In addition to the two feedback resistors,  $R_T$  and  $R_B$ , this solution requires one less resistor than the number of required output voltages. For example, if the application requires switching between three different voltages, the solution requires two injection resistors,  $R_X$  and  $R_Y$ , as shown in Figure 13.

As Table 2 shows, there are four logic states that can be derived from the two logic signals,  $V_X$  and  $V_Y$ ; however, only three logic states are used.

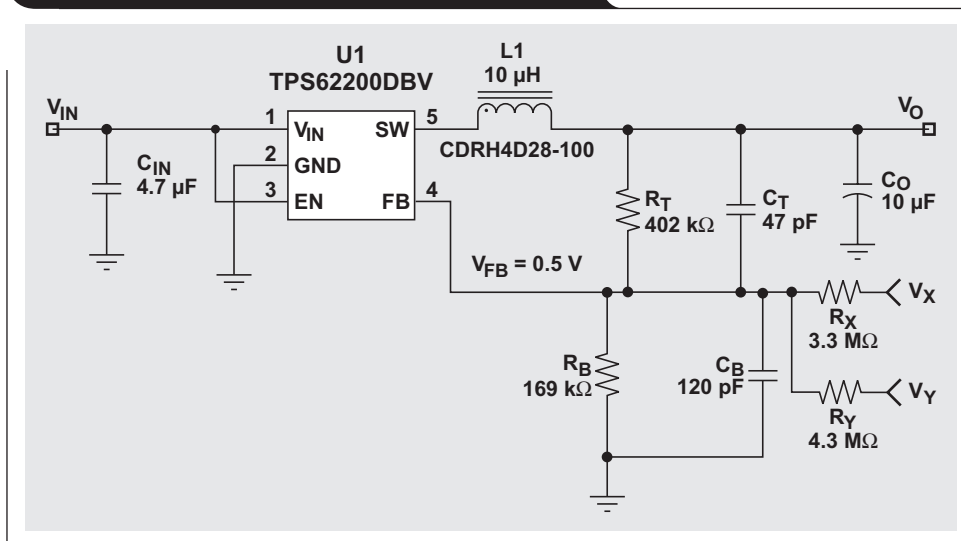
**Table 2. Control signal vs. output voltage**

	$V_X$	$V_Y$	DESIRED $V_O$ (V)	ACTUAL $V_O$ (V)
$V_{O1}$	LO	LO	1.80	1.80
$V_{O2}$	LO	HI	1.50	1.50
$V_{O3}$	HI	LO	Don't care	1.40
$V_{O4}$	HI	HI	1.10	1.10

**Figure 12. Filter for switching between multiple voltages**



**Figure 13. Switching between three voltages**



Similar to the computations for Figure 11, the circuit operation of Figure 13 can be evaluated with four nodal equations (one for each logic state), which can be solved for  $R_X$ ,  $R_Y$ , and  $R_B$  in Equations 5, 6, and 7.

$$R_X = R_T \times \frac{V_{X\_LO} - V_{X\_HI}}{-V_{O2} + V_{O4}} \quad (5)$$

$$R_Y = R_T \times \frac{-V_{Y\_LO} + V_{Y\_HI}}{V_{O1} - V_{O2}} \quad (6)$$

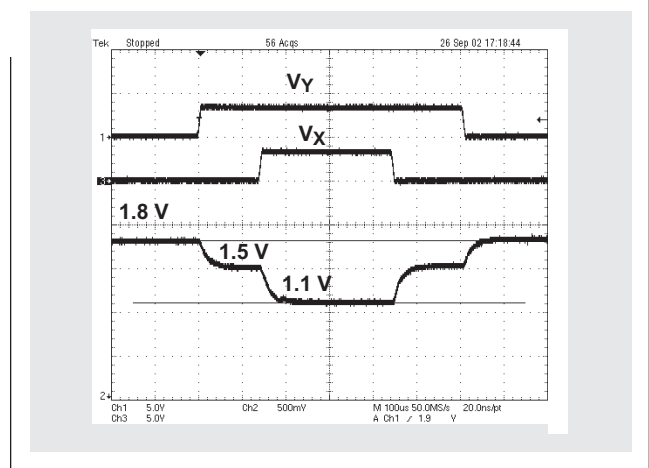
$$R_B = \left( \frac{V_{O1}/V_{FB} - 1}{R_T} - \frac{1}{R_X} - \frac{1}{R_Y} \right)^{-1} \quad (7)$$

$V_{O3}$  is not included in the equations, indicating that one of the four voltages is not independent of the others. The exact state/voltage that is not independent is determined by the method used to derive Equations 5, 6, and 7 but is one of the states during which the control signals are opposites (the second or third state in Table 2). In this case, the third state with  $V_{X\_HI}$  and  $V_{Y\_LO}$  is the dependent state and produces 1.40 V. Equations 5, 6, and 7 were used to find values for resistors  $R_X$ ,  $R_Y$ , and  $R_B$  in Figure 13, given  $R_T = 402 \text{ k}\Omega$ ,  $V_{O1} = 1.8 \text{ V}$ ,  $V_{O2} = 1.5 \text{ V}$ ,  $V_{O4} = 1.1 \text{ V}$ ,  $V_{X\_HI} = 3.3 \text{ V}$ ,  $V_{X\_LO} = 0 \text{ V}$ ,  $V_{Y\_HI} = 3.3 \text{ V}$ ,  $V_{Y\_LO} = 0 \text{ V}$ , and  $V_{FB} = 0.5 \text{ V}$ . Figure 14 shows the transition between the levels when  $V_{IN} = 3.3 \text{ V}$  and  $R_{LOAD} = 10 \Omega$ , using the circuit in Figure 13.

When injection resistors are used instead of FET switches, the transitions between voltages are much smoother.

Dynamic voltage scaling is a means of conserving power and therefore of extending battery life in portable electronics. There are two basic methods of implementing

**Figure 14. Transition between three voltages**



DVS using any adjustable power IC and an external control signal. If the control signal has a poor tolerance or can drive only capacitive loads, then the first method, consisting of FET switches in series with additional feedback resistors, is recommended. If the control signal has an acceptable tolerance and can drive a small resistive load, then the second method, using the control signal to inject current into the feedback network, is a simpler option and offers smoother transitions between voltages.

### Related Web sites

[analog.ti.com](http://analog.ti.com)

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