SHDSL AFE1230 application

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Introduction

Symmetric high-bit-rate digital subscriber line (SHDSL) was defined by the new ITU international standard G.991.2 in February 2001. This digital subscriber line uses advanced line coding and error correction technology, baseband Trellis-coded pulse amplitude modulation (TC-PAM), and symmetric power spectral density (PSD) to achieve symmetrical bit rates up to 2.3 Mbps at distances of over 12,000 ft. It provides full-duplex transmissions with multiple rates from 192 kbps to 2.3 Mbps over a single twisted-pair copper wire with extended transmission reach. SHDSL was developed to replace older DSL technologies such as HDSL, SDSL, ISDN, and IDSL. It is often used to provide symmetrical T1 and E1 service.

The implementation of SHDSL technology is based on a VLSI chipset including a digital signal processor (DSP) and an SHDSL analog front end (AFE). The DSP performs the functions of framer, encoder, decoder, and PAM engine under the control of an on-chip or off-chip microprocessor. The AFE provides the necessary interface between the DSP and the telephone line, which includes A/D converter, D/A converter, shaping filter, gain control, and line driver. With the chipset, a minimal but necessary external circuit is needed to provide the best speed, power, linearity, and signal-to-noise ratio (SNR) for the system. In this article a new Texas Instruments SHDSL analog front end, the AFE1230, and its basic application design are described to enable users to take full advantage of AFE1230 for DSL applications. This article includes details of both the external digital interface configuration and the analog interface circuit design.

AFE1230 function

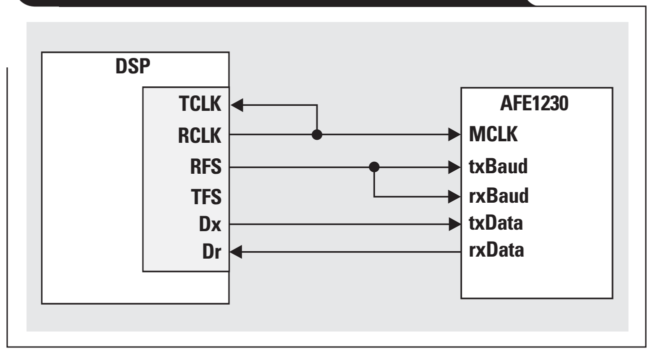
The AFE1230 provides upstream and downstream data conversion over a wide range of speeds from 64 kbps to 2.5 Mbps, so that it covers a range of bit rates beyond that of standard SHDSL. As a transceiver, it consists of a transmitter and receiver. The transmitter section includes a digital interpolation filter; a 16-bit ΣΔ D/A converter; a user-selectable fifth- or seventh-order, switched-capacitor (SC) low-pass filter; and a differential output line driver. The receiver section includes a digitally programmable gain amplifier, a 16-bit ΣΔ A/D converter, and a digital decimation filter. Via the digital serial interface, the AFE1230 receives a 24-bit word including a 16-bit data word and an 8-bit control byte. The received 16-bit word is upsampled by 2 through a digital interpolation filter to remove out-of-band images in the signal; it is then oversampled by the ΣΔ modulator with a factor of 12 and processed by the multi-level DAC section to facilitate the D/A conversion. The quantization noise from the ΣΔ D/A is then filtered by the on-board tx filter (the fifth- or seventh-order, SC Butterworth low-pass filter). At the same time, the signal is shaped by the tx filter to meet the SHDSL PSD requirements. Depending on the particular response desired, the tx filter can be programmed for three different corner frequencies as well as two filter (fifth- or seventh-order) configurations. The subsequent analog signal is sent to the on-chip line driver with an appropriate line transformer to provide up to 14.5-dBm power to a 135-Ω line for SHDSL. In addition, the on-chip line driver can be used as an output buffer to generate 17 dBm into a 135-Ω line via an external line driver such as the OPA2677 or OPA2607 for HDSL2 and DMT signal. The transmit power is controlled by the digital input.

In the receiver section, a differential input amplifier sums the signals from the line and hybrid path to perform first-order analog echo cancellation and programmable gain control. A fourth-order cascaded ΣΔ A/D converter with an oversampling ratio of 24 digitizes the resultant signal. The subsequent signal is processed by a fifth-order sinc filter and a programmable IIR filter for additional quantization noise reduction and downsampling as well as droop compensation. The resulting digital signal is then sent to the digital serial interface for processing by the DSP. The receiver section also can be set in Line Receiver Only mode (hybrid input is internally connected to common-mode voltage) or Hybrid Receiver Only mode (line input is internally connected to common-mode voltage) for different applications.

Digital interface configuration

The AFE1230 uses a standard four- or five-line digital serial interface operating in the slave mode. It can easily communicate with DSPs specifically designed for DSL applications or with general-purpose DSPs, such as TI's TMS320C5x™ or TMS320C6x™ series or analog devices SHARC series. Figure 1 shows a digital interface configuration of the AFE1230 connected to the serial port of a general-purpose DSP.

Figure 1. AFE1230 digital interface with general-purpose DSP



The AFE1230 has five digital interface lines: MCLK (master clock), txBaud (transmit baud clock), txData (input data), rxBaud (receive baud clock), and rxData (output data). The AFE1230 pins—MCLK, txBaud/rxBaud (txBaud is connected with rxBaud), txData, and rxData—are connected to the DSP pins—RCLK (receive clock), RFS (receive frame sync signal), Dx (transmit data), and Dr (receive data), respectively. The 32-bit DSP is set in multichannel mode to achieve 48-bit word serial communication required from the AFE1230. The DSP generates clocks of RCLK and RFS. The RCLK drives both TCLK (transmit clock) in the DSP and MCLK in the AFE1230. The RFS drives both txBaud and rxBaud in the AFE1230. The TFS (transmit frame sync signal) is open due to multichannel-mode configuration in the DSP. Following is a description of the five lines used for serial communication. Their timing is shown in Figure 2.

MCLK

The master clock of AFE1230, generated by the DSP, can vary from 1.28 MHz to 40.8 MHz (37.12 MHz for E1), with a 50/50 duty cycle required. It runs at 48 times the txBaud rate.

txBaud

The transmit data baud clock, generated by the DSP, can vary from 26.7 kHz to 850 kHz (517.33 kHz for T1 and 773.33 kHz for E1). One period of txBaud consists of 48 periods of MCLK. The pulse width of txBaud, t_W, should not be smaller than one period of MCLK. The txBaud is a frame sync signal that indicates the beginning of each serial word transfer. When txBaud is high, the rising edge of MCLK detects this signal; and the next rising edge of MCLK will sample the first bit of the serial word. After the txBaud is asserted, it is not checked again until the entire word has been received. The falling edge of txBaud can occur any time, t_f, during the txBaud period. txBaud and rxBaud must be the same frequency and synchronous with MCLK; however, the phase of these two signals may be different. For example, the DSP can generate both RFS and TFS separately to interface to the AFE1230. In the case of a phase jump (i.e., when the rxBaud or txBaud symbol clocks move one MCLK period forward or backward, resulting in 49 or 47 MCLK cycles per rxBaud), the receive data will be invalid for six symbol periods while the data settles to final value.

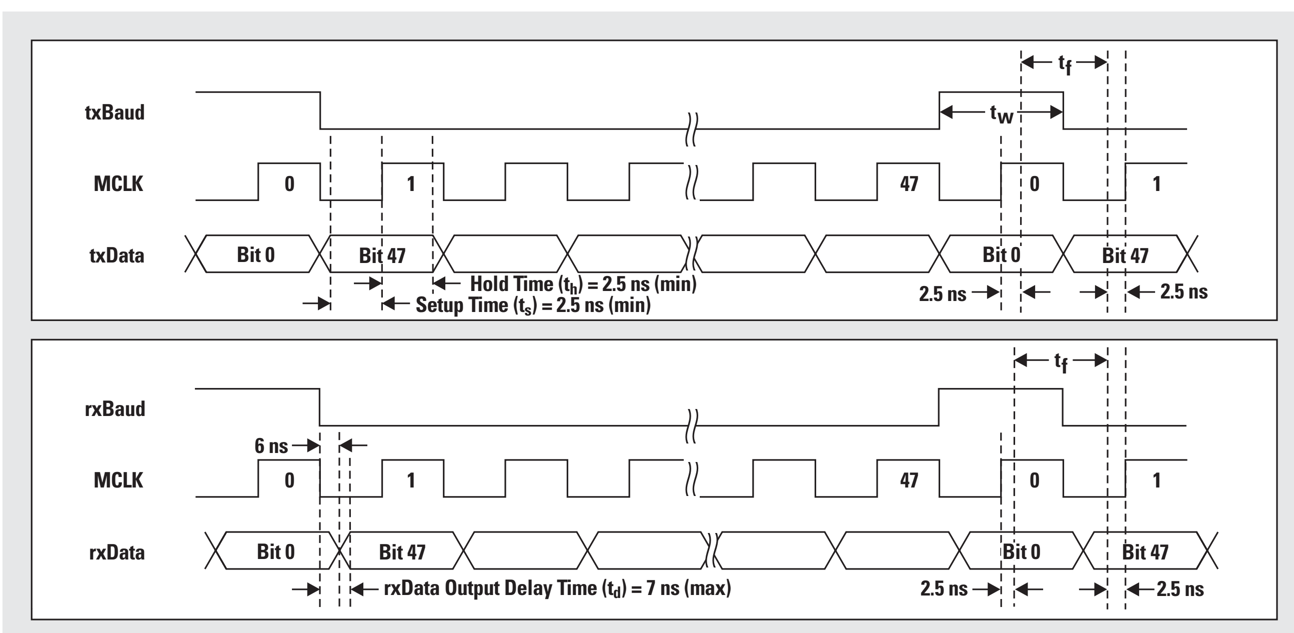
txData

The input digital data of AFE1230 comes from an external DSP with 48 bits per txBaud period. The 48 bits include two 16-bit words of DAC input data and two 8-bit control bytes. The DAC is updated two times per symbol period, and data is latched by AFE1230 on the rising edge of MCLK. txData must be stable at least 2.5 ns before and after the rising edge of MCLK (see Figure 2). The data is coded in two's complement with 16 bits.

rxBaud

The receive data baud clock, generated by the DSP, can vary the same as txBaud, from 26.7 kHz to 850 kHz (517.33 kHz for T1 and 773.33 kHz for E1). A period of rxBaud consists of 48 periods of MCLK. The pulse width of rxBaud, t_W, should not be smaller than one period of MCLK. The rxBaud is a frame sync signal that indicates the beginning of each serial word transfer. When rxBaud is high, the rising edge of MCLK detects this signal; and the next rising edge of MCLK will sample the first bit of the serial word. After the rxBaud is asserted, it is not checked again until the entire word has been transmitted. The falling edge of txBaud can occur any time, t_f, during the rxBaud period. The rxBaud and txBaud lines can be activated independently or at the same time.

Figure 2. AFE1230 digital interface timing



rxData

The output digital data of AFE1230 is sent to the external DSP as 48 bits per rxBaud period. The 48 bits include two 16-bit ADC data words and two 8-bit control data words (reserved). The ADC is read two times per rxBaud period, and rxData is updated by AFE1230 at the falling edge of MCLK. The maximum delay of the rxData is 7 ns (see Figure 2). The data is coded in two's complement with 16 bits.

Digital loop-back

AFE1230 provides a digital loop-back function that tests the DSP signal and the AFE digital interface. With bits 2 and 1 set as "01" in the digital input frame, the AFE1230's txData will connect with rxData internally to form digital loop-back.

Analog interface circuit

Two basic application analog circuits of AFE1230 are introduced here. The first circuit is for SHDSL as shown in Figure 3. This circuit has an on-chip line driver capable of providing 14.5-dBm power directly to the 135-Ω line. The other circuit is for HDSL2, shown in Figure 4 (next page). It has an off-chip external line driver, the OPA2677, to provide 17-dBm power to the 135-Ω line. Some of the design issues involved in these external analog circuits are transmitter power, power spectral density, output noise, input noise, input dynamic range, echo cancellation, and power dissipation. These issues are important and necessary to address here.

Figure 3. AFE1230 on-chip driving circuit for SHDSL

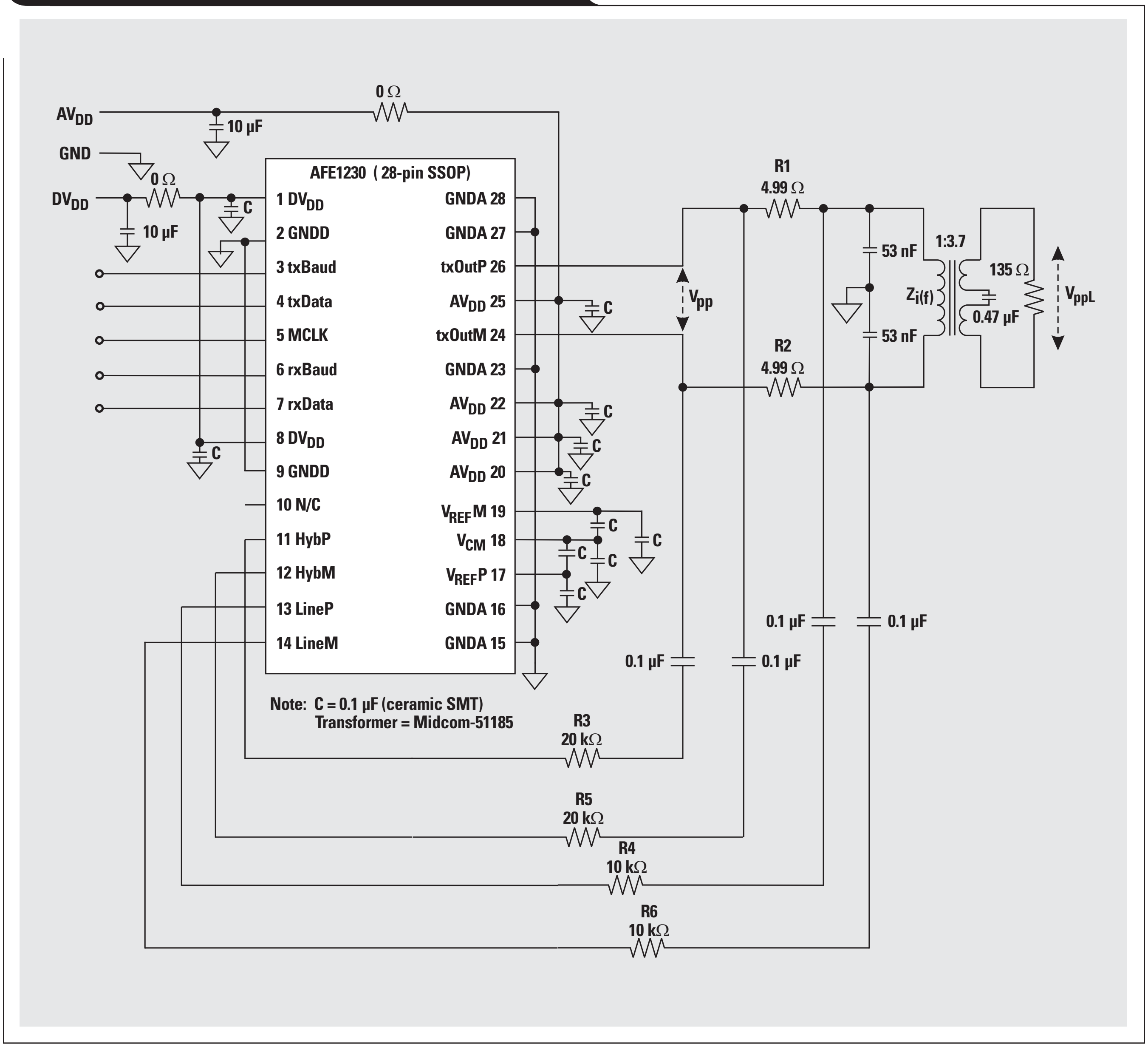
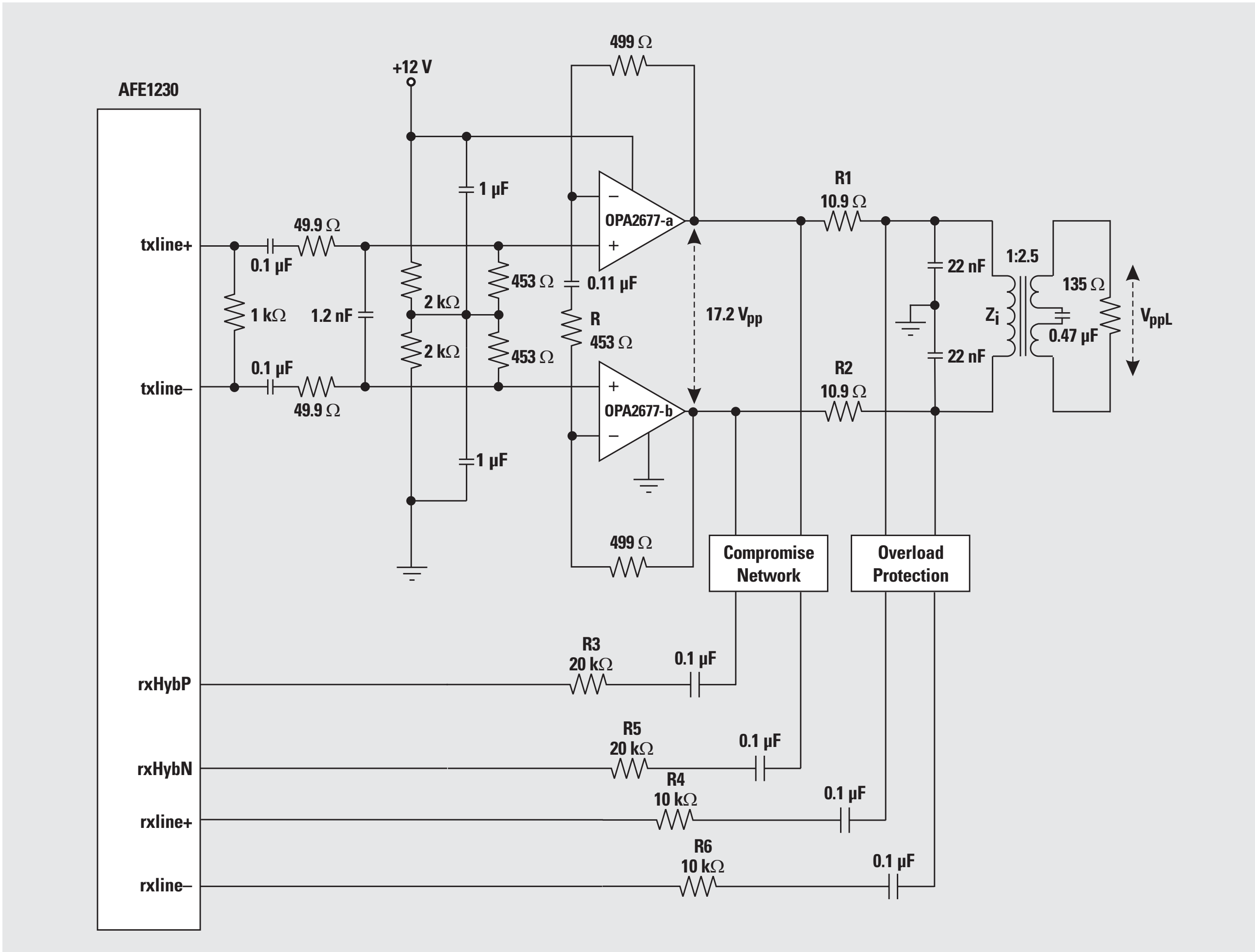


Figure 4. AFE1230 off-chip driving circuit for HDSL2



Transmitter power

To provide the power required by the specific line, it is necessary to consider the critical factors of output voltage swing of the AFE, maximum peak current of the on-chip driver, turns ratio of the transformer, peak-to-average power ratio (PAR) of the signal, and line impedance. These factors are directly related to circuit components; for example, the matching resistances R1 and R2 in Figure 3 and the transformer turns (device/line) ratio, n, directly affect the voltage on the line impedance and the load current to the driver. R1 and R2 are used to control far-end reflection and maximize the energy exchange between the AFE and the line. The turns ratio, n, is used to step up the voltage required by the line; however, if n is too high, it will create too much load for the driver and step down too much received signal voltage.

According to the SHDSL standard, the total power and power spectral density are measured with a load impedance of 135 Ω within a specific frequency range. If in Figure 3 we assume that the total power is 14.5 dBm, the PAR is 3.0, and the differential peak-to-peak output voltage from the AFE1230 is 6.2 V, then n is 3.7, and R1 and R2 are each 4.99 Ω. Such a design requires peak current of 158 mA, which is well within the AFE1230 on-chip driver's peak current capability of 230 mA.

The calculations for these values are determined by the following equations.

$$P_{dBm} = 10 \times \log(1000 P_w),$$

where P_{dBm} is the line power in dBm and P_w is the line power in watts.

$$P_w = V_{rms}^2 / R_L,$$

where V_{rms} is the voltage on the line and R_L is the impedance of the line (load impedance).

$$V_{ppL} = 2 \times PAR \times V_{rms},$$

where V_{ppL} is the peak-to-peak voltage on the line and PAR is the peak-to-average ratio of the power. PAR is 3.0 for SHDSL and 4.0 for HDSL2.

$$n = 2V_{ppL} / V_{pp}$$

(for matching line impedance), where V_{pp} is the output peak-to-peak voltage of AFE1230.

$$R1 = R2 = 135/(2n^2).$$

If these equations are used for the higher power of HDSL2, the matching resistances R1 and R2 in Figure 4 are 10.9 Ω each, and the transformer turns ratio, n, is 2.5. The external line driver must provide differential output peak-to-peak voltage of 17.2 V and peak current of 199 mA to deliver 17.3-dBm power to the HDSL2 line. TI's OPA2677 is suggested as the external line driver with a single +12-V power supply. Since the AFE1230 output differential, peak-to-peak voltage is 6.2 V, the ac gain of the external driver should be 2.8 V/V. With a 12-V supply, the dc offset (common-mode voltage) is 6 V. The ac gain, G, is estimated by the equation

$$G = 1 + (2R_F / R),$$

where R_F is the feedback resistance on OPA2677. In Figure 4, R_F is 499 Ω and R is 453 Ω.

Output noise

The AFE1230 has an on-chip, digital-interpolation, low-pass filter and a fifth- or seventh-order SC low-pass filter to remove the images from the digital input signal and D/A quantization noise. However, other sampling images appear at frequencies of multiple MCLK in the transmit output PSD due to the internal sample and hold function of the SC filter. The power of these images is relative to signal power, speed, and external low-pass filter cutoff frequency.

During normal operation, the output matching resistors and capacitor form a low-pass filter that reduces the power of these images to well below the PSD requirements of the SHDSL and HDSL2 standards. However, if the sampling rate (MCLK) is reduced while the low-pass filter cutoff frequency remains high, the first image will, of course, appear at a correspondingly lower frequency that may be within the SHDSL or HDSL2 signal band. At some point, lower sampling rates will produce an image, which can violate the appropriate PSD requirements. To reduce the power of these images, it is necessary to increase the sampling rate or improve the external analog low-pass filter.

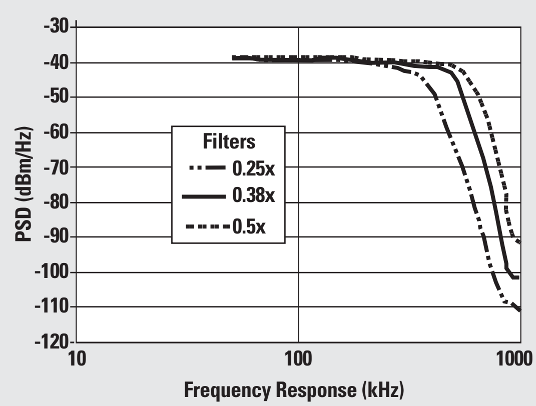
As an example, in Figure 3, the matching resistance and a capacitance of 53 nF contribute such a low-pass filter with cutoff frequency at about 650 kHz; in addition, the transformer acts as another first-order low-pass filter with cutoff frequency at about 2 MHz. These filters will greatly reduce the images. As a result, when the MCLK is 3 MHz, the power of the first image on the 135-Ω load can be reduced below –110 dBm/Hz; and, when the sampling rate of AFE1230 is fairly high, the power of the first image on the 135-Ω load can be limited below –120 dBm/Hz. These filters can also reduce high-frequency noise. The test shows that with a sampling rate of 1.25 MHz, 0.38× tx filter, and a full-scale, single-tone input with a 135-Ω load through the transformer, the circuit in Figure 3 can provide a transmit SNR of about 80 dB within the Nyquist band. If no signal is transmitted on the 135-Ω load, a transmit noise floor measured by HP spectrum analyzer is below –112 dBm/Hz in wide-frequency range.

Power spectral density

The transmit PSD provided by AFE1230, of course, should not exceed the PSD masks for all data rates; and total power into a 135-Ω line should fall within the range specified in the G.991.2 ITU standard for SHDSL. The spectral shaping is performed by appropriate DSP processing and by the transmit filter in AFE1230. However, the external filter and transformer will affect the spectral shape and are important factors in spectral shaping design.

With the circuit shown in Figure 3 and the input of a white noise generated in DSP, a transmit PSD can be measured. Figure 5 describes a PSD with white noise at a MCLK sampling rate of 30 MHz. These curves show the spectral shaping from the three user-selectable on-chip transmit filters (0.25×, 0.38×, or 0.5×) and external passive filters. If an appropriate FIR filter is applied to the white noise in the DSP before it is sent to the AFE1230, then the resulting PSD complies with the standard for the SHDSL PSD mask.

Figure 5. AFE1230 transmit PSD with white noise at MCLK of 30 MHz



Transformer

The key parameters of a line transformer are its turns ratio, primary inductance, leakage inductance, dc resistance, and total harmonic distortion. These parameters affect overall performance of the system. In practice, the transformer acts like a bandpass filter. The high-pass cutoff frequency is determined by the primary inductance, and the low-pass cutoff frequency is determined by the leakage inductance.

If the primary inductance is too high, the low-frequency components included in the signal will create a long tail in the impulse response of the echo path, which the equalizer in the DSP cannot remove. However, if the primary inductance is too low, it will reduce the signal bandwidth with a subsequent loss of information. This is particularly important in the case of low data rates. On the other hand, higher data rates require lower leakage inductance and better total harmonic distortion. A recommended transformer for AFE1230 G.SHDSL applications is the Midcom 51185, which provides a turns ratio of 3.7, primary inductance of 2 mH, leakage inductance of 26 µH, dc resistance of 1.6 Ω, and total harmonic distortion of 80 dB.

Receiving signal and noise

Because SHDSL is a full-duplex data transmission system with overlapping spectra, the AFE1230 receives both line receive signal and transmit signal at the same time and in the same bandwidth. In Figure 3, the received line signal is reduced by a factor of 3.7 by the transformer and has a dynamic range of about 35 dB due to different line attenuation. The line signal includes delay distortion due to the limitation of the channel bandwidth. The received transmit signal is the transmit signal reduced through the voltage-dividing effect of the matching resistance and the line impedance. Since the line impedance changes with frequency, the voltage divider changes with frequency. This means that the total received signal is also a function of the frequency.

The AFE1230 also receives noise from a number of sources, which include thermal noise from random electron motion, impulse noise from power spikes, echo signals from terminal impedance mismatch, reflections from bridged taps, and crosstalk from inductive and capacitive coupling between two wires in the same cable. If not controlled, this noise can cause the failure of signal detection in some cases. To limit the noise, a band-limited low-pass filter is necessary even though there is an on-chip anti-alias (AA) filter included on the AFE1230.

In Figure 3, an FFT measurement of this circuit for the AFE1230 operating at a 30-MHz sampling rate (MCLK) shows that for a full-scale, single-tone signal through the filter, the SNR of the digital output is about 86 dB with a PGA gain of 0 dB, and 76 dB with a PGA gain of 21 dB within the Nyquist band.

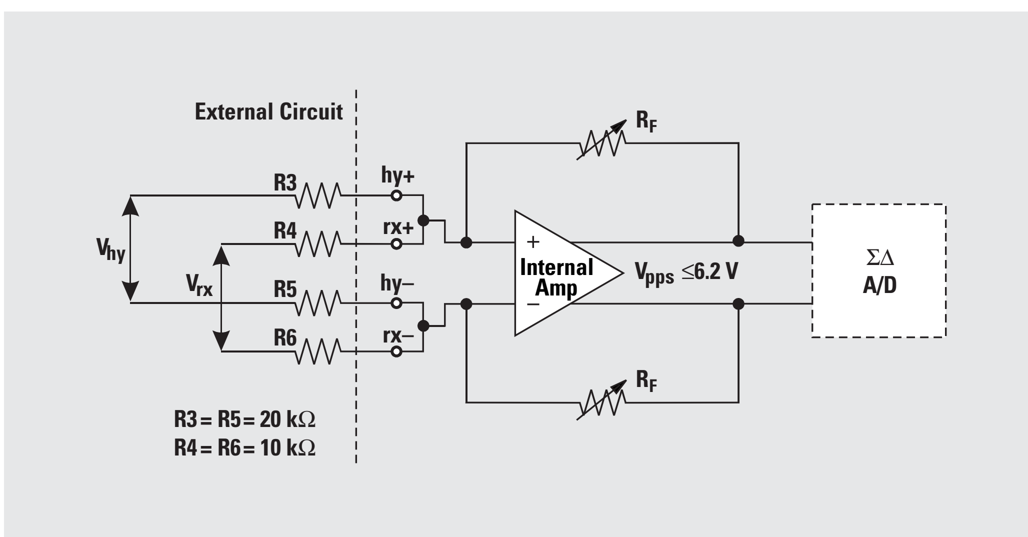
Echo cancellation

Echo cancellation is used in full-duplex data transmission systems to remove the transmit signal from the receiver signal. This is typically realized partially in an analog hybrid circuit and partially in the DSP. The hybrid circuit is actually an electrical bridge, formed by the line impedance, transmit matching resistance, receiver input impedance, and hybrid input impedance. When the bridge is perfectly balanced, the far-end reflection, near-end reflection, and trans-hybrid reflection will be zero. However, since the line impedance changes with frequency and line condition as well as with limitations of the hardware, an unbalance in this analog electrical bridge always exists.

In general, analog echo cancellation between the line transformer and the receiver input is the first step to remove the majority of the echo signal and reduce the dynamic range requirements of the receive channel A/D converter. Digital echo cancellation in the DSP is the final, precision step to remove the rest of the echo.

Figure 3 shows a basic hybrid circuit configuration with a resistor-only network. If line impedance is assumed to be a constant of 135 Ω, only resistors need to be inserted in the transmit path, receiver path, and hybrid path. A resistance of 10 kΩ is required for each receiver input, and 20 kΩ for each hybrid input. These four resistors are connected to the virtual ground inputs of the on-chip differential input amplifier to form a differential summing amplifier. This is shown in Figure 6. Since the receiver and hybrid paths have a phase difference of 180° from each other, the input amplifier subtracts their voltages to create

Figure 6. Echo cancellation with R network and internal receive amplifier



a first-order analog echo canceller. The output voltage of the summing amplifier, V_{pps}, is then digitized by the A/D converter. The analog echo cancellation can be determined by the following equations.

$$V_{pps} = (R_F / R4)V_{rx} - (R_F / R3)V_{hy},$$

$$V_{rx} = V_{line} + (1/2)V_{tx}, \text{ and}$$

$$V_{hy} = V_{tx},$$

where V_{line} is the signal from the line and V_{hy} or V_{tx} is the transmit signal from the AFE1230. The common-mode voltage of the receiver amplifier is half of the analog power supply and is set internally.

Unfortunately, in practice, the line impedance is not constant and changes with line condition and frequency. This change can be modeled by an RC or RLC network. A common way to match the line impedance is to insert an RC or RLC compromise network into the hybrid path to track the line impedance change (Figure 4). The RC components for different loops can be determined with line simulation models that include a line transformer equivalent circuit. When the compromise network is inserted in the hybrid path of the external circuit, the resistors R3 and R5 on the hybrid path and the dc block capacitors (0.1 µF) on both the hybrid and receive paths will be determined by the compromise network.

Conclusion

TI's analog front end, the AFE1230, provides an SHDSL transceiver interface function between a DSP and the local loop. With an appropriate external circuit, it will handle upstream and downstream data transmission over the telephone line. The AFE1230's standard 5-wire serial digital interface supports full-duplex communication with the serial port of a DSP. A 6-pin analog interface with simple passive external filters, a transformer, and a hybrid circuit insures power delivery and reception as well as echo cancellation in the DSL application. The fundamental external circuit design procedure, using either an on-chip line driver for SHDSL or an off-chip driver for HDSL2, is also described in this article. The main factors for the design are signal PAR, line power, driver, transformer, receiver dynamic range, PGA, and analog echo cancellation. For optimum system performance with good PSD and SNR, the transformer effect, receiver band-limited filter, and line impedance matching need to be considered in the external circuit design.

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4. Alan V. Oppenheim, *Discrete-Time Signal Processing* (Prentice-Hall, Inc., 1989).

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Replace *partnumber* with AFE1230, OPA2607 or OPA2677

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