Powering electronics from the USB port

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Introduction

The USB interface can provide power to low-power peripherals but must adhere to the USB 2.0 specification (Reference 1). Table 1 provides an overview of the requirements placed on the peripheral equipment. The host equipment provides a 5-V supply capable of, in the worst case, only 2.25 W of power. In some cases, this is clearly not enough for the peripheral, and an alternate power source such as a wall adapter or off-line power supply is used. In other cases, 2.25 W is much more than is needed; and low-cost, linear regulators can be used to generate the supply voltages for the peripherals. However, in many cases this power limit necessitates the use of higher-efficiency power-supply designs and complicates the system trade-offs of cost, efficiency, and size. This article discusses these issues.

Table 1. USB power requirements at a glance

PARAMETER		REQUIREMENT
Voltage	Low-power device	4.4 to 5.25 V
	High-power device	4.75 to 5.25 V at upstream connector
Maximum quiescent current	Low-power device	500 µA
Maximum low-power current		100 mA
Maximum high-power current		500 mA
Maximum power draw		2.25 W
Maximum input capacitor		10 µF
Maximum inrush		50 µC

Another unique requirement of the USB power interface is the different current draws allowed. When a device is first connected to the USB, its bypass capacitor could be charged abruptly and create a glitch on the host equipment supply. The USB specification resolves this problem by limiting the initial power surge in two ways. The peripheral device is allowed only a small (<10-µF) bypass capacitor, and the charge drawn from the bus is limited to 50 µC over a specified time. Larger capacitors can be used if inrush limiting is provided. Once the USB is connected, there are further limits on current draw. The host first recognizes the peripheral as low-power, allowing it to draw less than 100 mA of current. The peripheral can ask the host to recognize it as a high-power device in a process called "enumeration." Once enumeration is completed and permission is granted, the allowed peripheral current is increased to 500 mA. The USB spec also includes a suspend mode that supports remote wake-up. This mode limits quiescent current to a total of 500 µA for a low-power device and 2.5 mA for a high-power device. It often requires the use of switches to power down portions of the peripheral's electronics.

The USB 1.0 specification has been active since its release in November 1995. Products that were delivered to the 1.0 specification had no official logo associated with them. Many times the products did not fully meet the current-limit requirements, which usually was not a problem with the product connected to a PC. However, problems did arise when there were multiple products connected in a hub arrangement. With the release of the 2.0 specification, certified products will be marked with a logo. The certification promises to be more rigorous, and designers should expect to meet the requirements of the new specification.

Inrush limit and power segmentation

There are two possible configurations for USB products—a single peripheral connected directly to a host, or a set of peripherals connected through hubs to the host. For a single peripheral, the current-limiting requirements usually are not an issue unless a large input capacitor is placed across the power-supply voltage for hold-up. If hubs are used, current limiting will definitely be required due to the unknown nature of the peripherals that will be plugged into the hub.

The current limits can be implemented in two manners, one using discrete power devices with external control circuits, and the other with the switches integrated into the controllers. In higher-power applications, the discrete approach usually yields a lower-cost solution. However, in lower-power applications, an integrated approach is very attractive. With the low voltages and currents involved in the USB, a number of manufacturers are developing ICs specifically targeted for these markets. Figure 1 on the next page presents a typical circuit. The first output is an adjustable linear regulator that can be configured for 0.9- to 3.3-V output, which powers the hub controller and other electronics. The second is a switched output that powers the peripherals connected to the hub. The integrated approach provides a number of desirable features. The device is much more rugged than a discrete approach because a thermal limit monitors the pass-element temperature and shuts down if an over-temperature is detected. Two-level current limiting is provided in the switch to prevent glitching of the host power bus. Initial power-up current is limited to 100 mA until the output reaches 93% of the input voltage; then, once the USB controller is enumerated, the current limit is raised to 500 mA, typical of the high-power peripherals.

Figure 1. Internal switch power segmentation and limiting

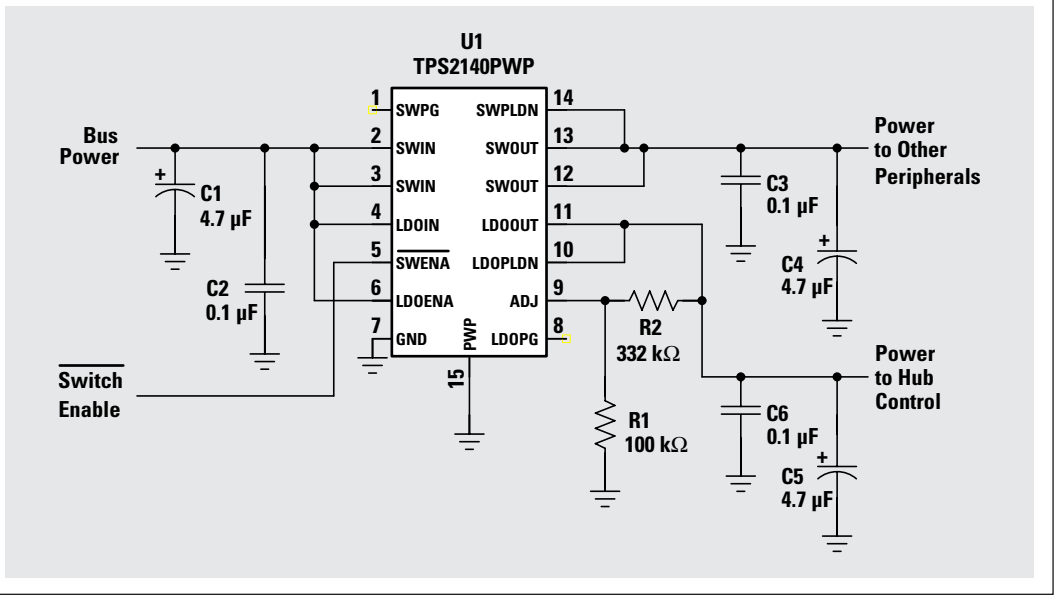


Table 2. Power-management options

POWER MANAGER IMPLEMENTATION	SWITCH RESISTANCE (mΩ)	CIRCUIT AREA (in^2)	OVER-TEMPERATURE PROTECTION	OVERALL RELATIVE COST (%)
Internal switch	100	0.30	Yes	80
External switch	50	0.5	No	100

Table 2 compares the two approaches, internal versus external switches or pass elements. The pass elements have higher resistance in the internal switch approach, which occupies less than 60% of the external switch approach. However, the silicon die area is more costly in the internal switch because more mask levels are involved in the IC's device structure than in a simple MOSFET. Typically, the IC will use over 20 mask levels compared with 8–10 levels of the MOSFET. The higher level of integration eliminates at least two semiconductor packages and the resulting poor interconnect efficiency. In addition, the higher level of integration provides a higher reliability as bond wires and solder joints are eliminated. Reliability is further enhanced with the over-temperature protection of the internal switch. With the external switch, there is no cost-effective method to measure MOSFET temperature to protect it from shorted loads. Current foldback and power cycling techniques can help but do not provide the robustness of the thermal shutdown. The last column of the table presents a cost comparison between the two approaches. The costs are almost the same and would bear a closer examination on a particular requirement. Generally, the reason the costs are so close is that the external switch approach uses multiple semiconductor packages compared with the single package of the integrated switch. Each of the packages has its own overhead of assembly and test, making the overall system-level costs about equivalent.

Powering low-voltage digital electronics

Generating low voltages, such as 3.3 V, from the USB can be done in several ways. Regardless of the configuration used, the output current for a 3.3-V output is limited to 0.65 A (assuming 95% efficiency) due to the 2.25-W input power limitation. The options to provide these lower voltages include linear regulators, switching power supplies, and charge pumps. Within switching power supplies, there are two further subgroups, synchronous and conventional. The synchronous is more efficient and costly and will be used to get as much power from the USB as possible.

The linear regulator is the lowest-cost and highest-density option for generating lower voltages from the 5-V USB. When there is no power issue, it will be the circuit of choice. However, when power becomes an issue, switching regulators can more efficiently power the

peripheral. Figure 2 shows one of the lowest-cost buck switching regulator options available. In this circuit, the switching of the FET, Q2, is controlled to "buck" the average voltage presented to the output filter, which then smooths the switching waveform. The drawback of this circuit is that the lack of controller integration requires an external FET and drive circuit, which makes the circuit relatively large. An external FET provides flexibility in the design, allowing lower on resistance devices to be used compared with integrated FET controllers, and possibly achieving greater efficiency.

In Figure 2, a large percentage of the overall power loss is dissipated in the freewheeling diode D2. In Figure 3 this diode is replaced with an N-channel FET, making this circuit a synchronous buck converter, which significantly improves the converter efficiency. Efficiency improvements

Figure 2. Low-cost, non-synchronous buck regulator

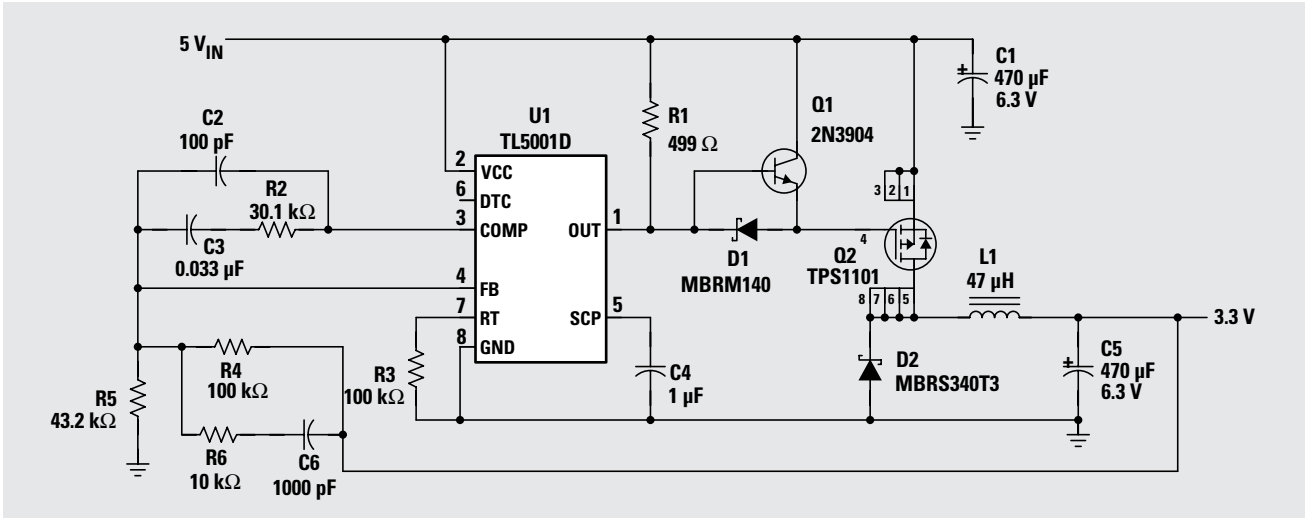


Figure 3. External-switch synchronous buck regulator

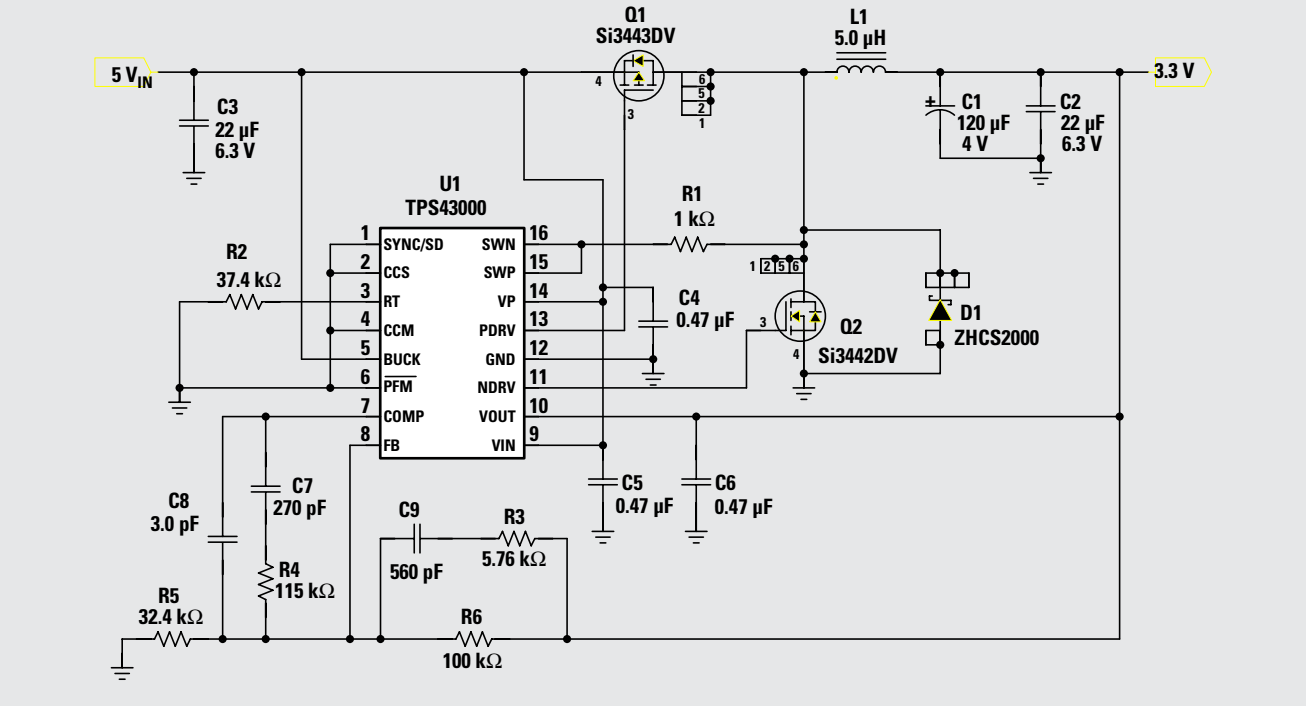


Figure 4. Step-down charge pump

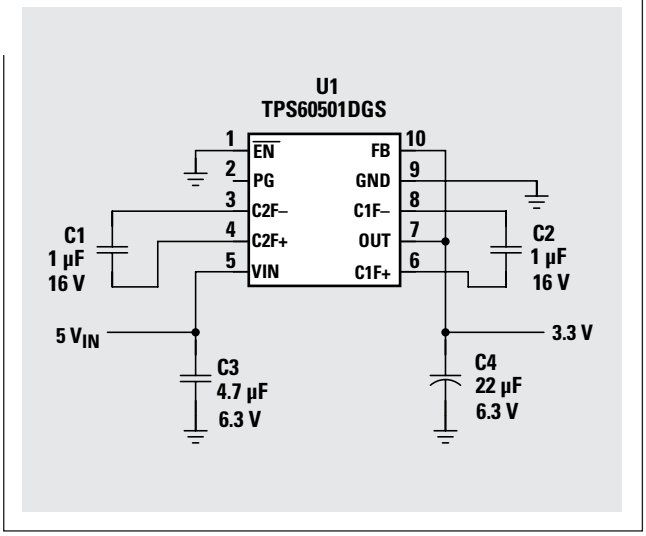
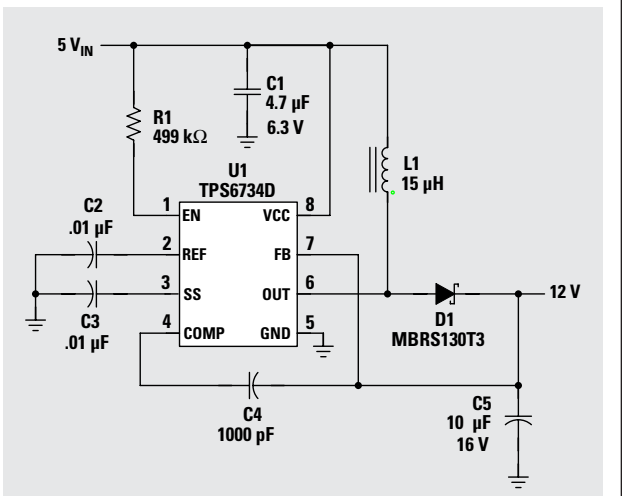


Figure 5. Boost regulator



can be realized over a wide load range with this circuit. At very light loads, pulse skipping can decrease gate-drive losses. When the output voltage drops 2% below the nominal voltage set point, the converter senses it and switches until the output reaches an upper threshold; it then puts itself in sleep mode until the load discharges the output capacitor to the lower threshold again. This circuit provides excellent efficiency but is more costly than the one in Figure 2. Its circuit area is also slightly smaller, mainly because the controller can operate at frequencies of up to 1 MHz, which allows the inductor and input/output capacitors to be noticeably smaller.

Integrating the top FET, bottom FET, drive circuit, and feedback compensation into the controller provides for a small, integrated, and efficient converter solution. This is becoming a very popular solution because it is generally simple to design and has a very short design cycle time. Software is available that aids in the design, making it possible for novices to design power supplies. Controllers such as the TPS5431x and TPS5461x SWIFT™ series provide such integration, but their cost is higher due to the added performance and features.

Circuit area is often a critical design parameter. The step-down charge pump in Figure 4 represents an extremely small solution. Four ceramic capacitors and the charge pump controller are the only components required for this solution. The controller utilizes internal FETs that connect two flying capacitors in various series or parallel configurations, dumping their energy to the output. The input voltage and the load are used to set the internal FET configuration automatically. At loads heavier than 150 mA, the controller acts as an LDO and stops using the switched capacitors altogether. Output current is limited to a maximum of 0.25 A, which limits this circuit to low-power applications. Efficiency is between 80 and 90% for light loads between 1 mA and 50 mA, but drops off to approximately 65% above that when operating in LDO mode. The cost of Figure 4 is one of the lowest, due to the low cost of the ceramic capacitors.

Table 3 provides a summary of the low-voltage step-down options discussed. Efficiency, cost, and circuit area are also listed for reference. So what's the right choice? Linear regulators, when you can afford the losses. Then take a look at charge pumps and determine their losses based on conversion ratios. Finally, evaluate non-synchronous and then synchronous regulators. In each case, the system cost and size increase, but more power is available for the load. A second trade-off in the switching power supplies involves deciding between internal and external FETs. The cost is usually lowest with external FETs; while the design time, component count, and size will be smaller with internal FETs.

Table 3. Low-voltage (5-V to 3.3-V) regulator options

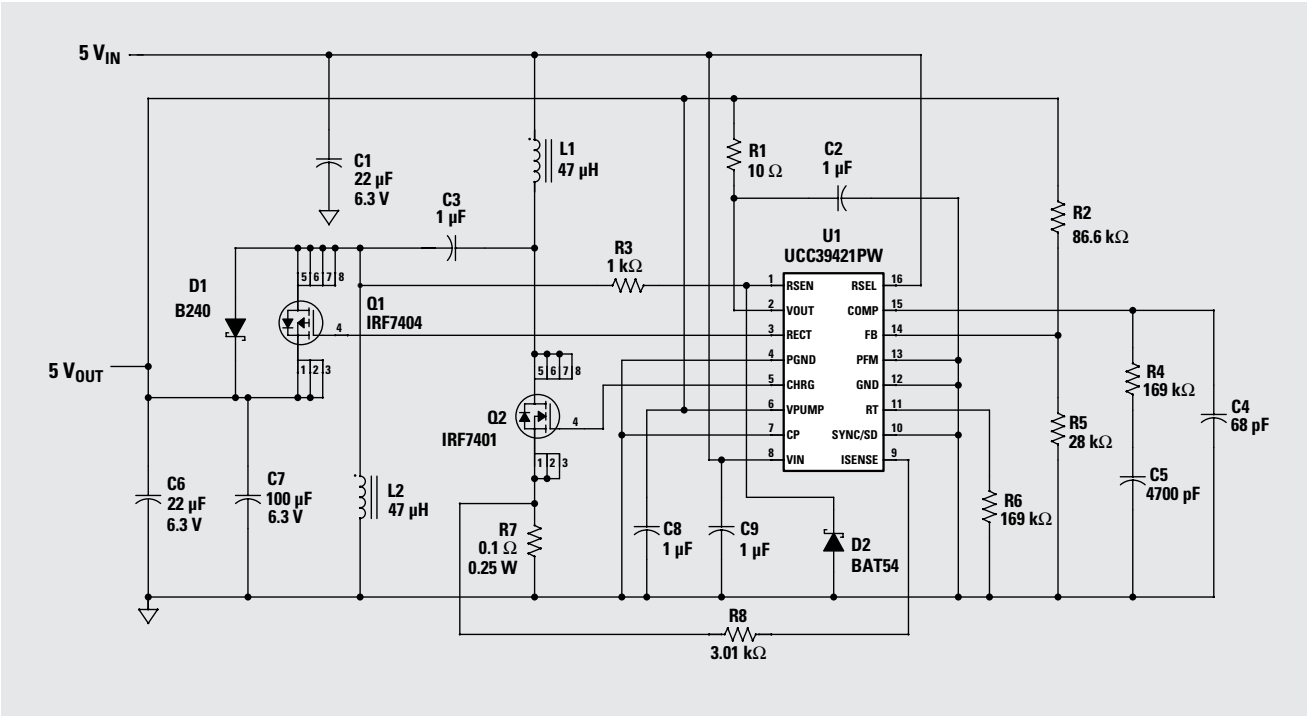
TOPOLOGY	INTERNAL SWITCH	TYPICAL EFFICIENCY (%)	OVERALL RELATIVE COST (%)	AREA (in^2)
Linear	Y	66	40	0.1
Non-synchronous buck	N	87	100	1.2
Non-synchronous buck	Y	85	150	1.1
Synchronous buck	N	96	200	1.0
Synchronous buck	Y	95	250	0.7
Charge pump*	Y	60 to 90	70	0.15

*Current is limited to 0.25 A, and efficiency is largely dependent on input voltage.

Powering higher-voltage analog

Higher-legacy voltages, such as 5 V and 12 V, are often required to power analog circuits. The loading on these outputs is typically not as heavy as on their digital voltage counterparts—usually less than 100 mA. The circuit in Figure 5 is a boost regulator that provides 12 V and will provide up to 120 mA while operating over the 5-V USB output voltage range. In this

Figure 6. Synchronous SEPIC converter



design, the FET is integrated into the controller along with the feedback resistor network, reducing total parts count to a minimum. A drawback to this approach is that the circuit block provides no current limit. If the 12-V output is shorted to ground, there is nothing in the V_{IN}, L1, D1 path to limit current.

An alternative topology, the SEPIC, can overcome this shortcoming. Also, the SEPIC conversion ratio extends above and below the input voltage as compared with the boost, whose ratio just includes voltage greater than V_{IN}. Since the USB voltage can range from 4.5 V to 5.5 V, the SEPIC converter in Figure 6 makes an excellent choice for a 5-V output. This SEPIC uses a synchronous rectifier Q1 to reduce the losses in the output diode and improve efficiency by several percent. Diode D1 conducts only during the on/off transitions of Q1 to prevent the intrinsic diode of Q1 from conducting. Additional benefits include low-input ripple currents and inherent current limiting. On the negative side, the addition of the dc blocking capacitor C3 is required. Since the blocking capacitor and output capacitors must handle large pulsing currents, they require a high RMS ripple-current rating and a low ESR to minimize the output ripple voltage. Ceramic capacitors are usually chosen due to their high ripple-current rating and low cost.

Figure 7. Synchronous buck converter with auxiliary output winding

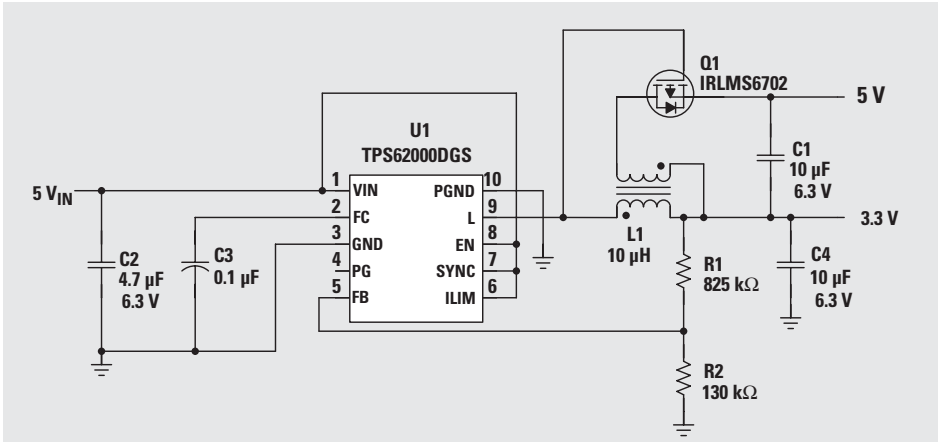


Figure 7 shows an option for providing dual-output voltages from a single synchronous buck converter. When the bottom-side FET (internal to TPS62000) conducts, FET Q1 turns on, and output cap C1 charges with an additional voltage developed across the secondary of L1. The level of the auxiliary voltage is determined by the turns ratio

Table 4. Higher-voltage regulator options

TOPOLOGY	INTERNAL SWITCH	CURRENT LIMIT	TYPICAL EFFICIENCY (%)	OVERALL RELATIVE COST (%)	AREA (in^2)
5-V to 12-V boost	N	N	86	280	0.7
5-V to 12-V boost	Y	N	85	320	0.6
5-V to 5-V SEPIC*	N	Y	89	560	1.0
5-V to 5-V SEPIC	Y	Y	85	550	0.9
3.3-V to 5-V charge pump**	Y	Y	65 to 75	200	0.2
Sync buck w/aux winding†	Y-Sync buck N-Aux	Y	95	100	0.3

* Synchronous operation
** TPS60133 charge pump controller, 0.3-A maximum output current
† Cost and area of auxiliary output only

between the two windings of L1. The voltage across C1 is stacked on the 3.3-V regulated output; so, for a 5-V auxiliary output, an additional 1.7 V needs to be developed across L1's secondary. A turns ratio of 2:1 will work well in this application. For low current levels, the voltage drops developed across the internal bottom FET and Q1 (which turn on in phase with each other) are small and often cancel each other out. These FET drops may not significantly add to the output-voltage tolerance error, and good regulation can be achieved.

Table 4 presents a comparison of some of the options for generating higher voltages for analog loads. Here again, the decision involves a trade-off between cost, performance, and loss. If power is not a problem, the first choice to consider is a charge pump. When loss becomes an issue, a switching regulator may become warranted. The first circuit to consider, particularly if a buck regulator is being used, is the auxiliary winding scheme of Figure 7. It adds minimal cost and degrades efficiency the least. Next come the SEPIC and boost regulator. The need for short-circuit protection will determine which approach will be favored. Usually a boost will be chosen for its higher efficiency if current limiting is not needed or can be accommodated elsewhere in the system. There are also trade-offs in synchronous and non-synchronous operation, as well as in an internal versus external switch, as in the buck regulator.

USB-powered DSL modem power supply example

The circuit in Figure 8 (next page) is an example of a complete USB power supply with 3.3-V, 5-V, and 12-V outputs. With the 3.3-V powered at 0.32 A, the 5-V at 0.05 A, and the 12-V at 0.05 A, the overall efficiency is 89.5%, which allows the input power to remain below the 2.25-W maximum limit. In operation, only the 3.3-V output is allowed to power up at turn-on, with the 5-V and 12-V enable pins being held low by the bus controller. No more than 100 mA is drawn off the 3.3-V output during power-up in low-power mode. Enumeration then comes from the bus controller to allow the 5-V and 12-V to power up. A boost topology was used for both the 5-V and 12-V outputs, with the 5-V power stage input powered from the 3.3-V output. The controller chosen for both boost regulators was the low-cost TL1451A dual controller. The approach taken for this design example is geared toward low cost and high efficiency rather than small area. Figure 9 shows a photograph of the completed hardware, which measures 1.5" × 2".

Figure 9. DSL modem power supply

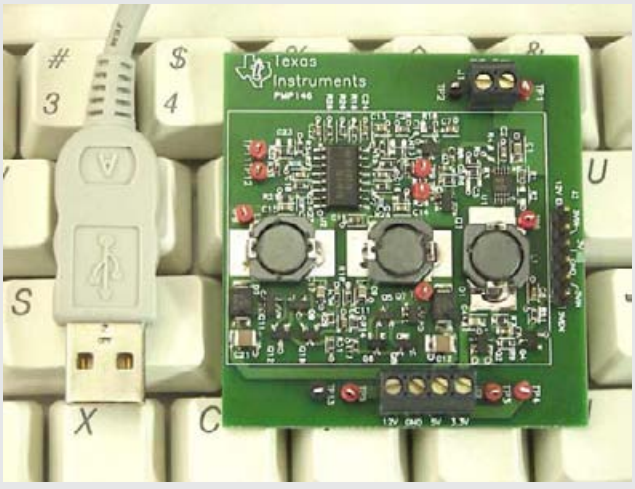
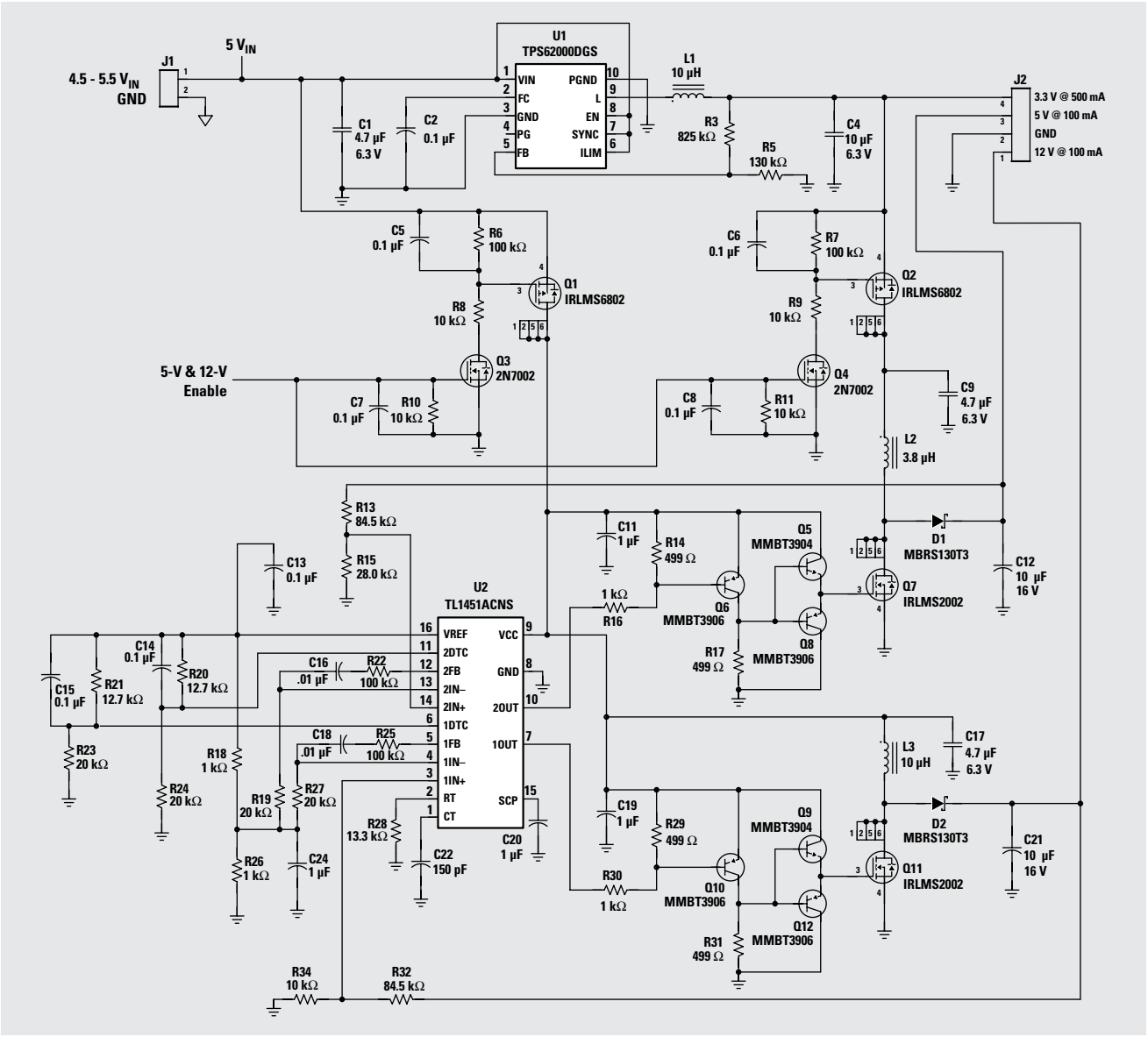


Figure 8. USB-powered DSL modem power supply



Conclusion

The design of a power supply powered from the USB port is heavily driven by the 2.25 W of available input power and the peripheral load requirements. The design process should involve a very careful analysis of load currents followed by a program to minimize them. Once the loads have been determined, the power-supply engineer should develop multiple block diagrams with the topologies described in this article to develop the lowest-cost, most power- and area-compliant approach. The array of integrated circuits to support these designs is very diverse; the designer has the options of striving for maximum integration, minimum cost, and ease of use.

Reference

1. USB Implementers Forum Inc., "Universal Serial Bus Specification Revision 2.0," www.usb.org

Related Web sites

www.ti.com/sc/device/*partnumber*
Replace *partnumber* with TL1451A, TL5001, TPS2140, TPS6734, TPS43000, TPS54310, TPS54610, TPS54611, TPS60130, TPS60500, TPS62000 or UCC39421
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